DATA HANDBOOK

I²C Peripherals for Microcontrollers

Signetics

Philips Semiconductors

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Preface

I²C Peripherals for Microcontrollers

Signetics supplies over 100 devices with an embedded I²C serial interface. I²C, Inter-Integrated Circuit, is a simple, two-wire serial bus developed by Philips. This powerful and widely-adapted serial bus has been successfully designed in a broad range of applications, from simple consumer products to complex military and computer applications.

This data handbook covers those I²C devices that are commonly used with Philips' line of microcontrollers. Additional I²C devices, depending on application and use, are covered in separate books. 80C51 microcontrollers that contain the I²C interface are covered in the *80C51 and Derivative Microcontrollers* data handbook (IC20). 84CXXX microcontrollers with the I²C interface are also covered in a separate data handbook.

Signetics supplies a wide range of microcontrollers based on mainstream architectures, spanning 8-, 16-, and 32-bit product lines. By offering a large variety of product derivatives, Signetics can meet a broad range of specific or unique application requirements. All of our microcontrollers are based on mainstream architectures to allow the user to take advantage of existing software and a vast array of third-party support.

Signetics 8-bit microcontrollers are based on the popular 80C51 and 80C49 architectures. We offer most of the industry standard products in these architectures as well as a large selection of powerful derivative products. These derivatives offer a wide assortment of features, including: memory from 2K to 32K, Analog-to-Digital, PWM, additional timers, embedded EEPROM I²C and CAN serial bus, extended I/O, low power/voltage (1.8 volts, etc.). OTP and EPROM versions are available for virtually every derivative. Philips has the most 80C51 derivatives in the world.

Signetics 16-bit microcontroller family is based on the powerful 68000 architecture. While these are called 16-bit microcontrollers, the 68000 CPU core architecture is 32-bit. This offers the user a great deal more processing power, when the need arises in a design to move from an 8-bit to a 16-bit microcontroller. Signetics 16-bit microcontrollers are software compatible with existing 68000 code. As with our popular 8-bit microcontrollers, EPROM and OTP versions of our 16-bit products are available. The 16-bit microcontrollers are also covered in a separate data handbook.

Signetics is developing a family of 32-bit microcontrollers based on the SPARC RISC architecture. This family of microcontrollers will offer the ultimate in processing power for those applications that are computation intensive in an embedded control environment.

Signetics offers uncompromising quality, service, and support with all of its microcontroller products. For a complete family and the best in microcontroller products, look to Signetics.

Product Status

I²C Peripherals for Micrcontrollers

DEFINITIONS		
Data Sheet Identification	**Product Status**	**Definition**
Objective Specification	**Formative or In Design**	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
Preliminary Specification	**Preproduction Product**	This data sheet contains preliminary data and supplementary data will be published at a later date. Signetics reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product Specification	**Full Production**	This data sheet contains Final Specifications. Signetics reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

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I²C bus addresses

ASSIGNED I²C BUS ADDRESSES

PART NUMBER	FUNCTION	I²C ADDRESS						
		A6	A5	A4	A3	A2	A1	A0
—	General call address	0	0	0	0	0	0	0
—	Reserved addresses	0	0	0	0	X	X	X
PCD3311/12	Tone generator DTMF/modem/musical	0	1	0	0	1	0	A
PCF8200	Voice synthesizer (male or female)	0	0	1	0	0	0	0
PCF8566	96-segment LCD driver 1:1–1:4 Mux	0	1	1	1	1	1	A
PCF8568	LCD row driver for dot matrix displays	0	1	1	1	1	0	A
PCF8569	Column driver for dot matrix displays	0	1	1	1	1	0	A
PCF8570/71	256 × 8, 128 x 8 static RAM	1	0	1	0	A	A	A
PCF8570C	256 × 8 static RAM	1	0	1	1	A	A	A
PCF8573	Clock/calendar	1	1	0	1	0	A	A
PCF8574	I²C bus to 8-bit bus converter	0	1	0	0	A	A	A
PCF8574A	I²C bus to 8-bit bus converter	0	1	1	1	A	A	A
PCF8576	160-segment LCD driver 1:1–1:4 Mux	0	1	1	1	0	0	A
PCF8577	64-segment LCD driver 1:1–1:2 Mux	0	1	1	1	0	1	0
PCF8577A	64-segment LCD driver 1:1–1:2 Mux	0	1	1	1	0	1	1
PCF8578	Row/column LCD dot-matrix driver	0	1	1	1	1	0	A
PCF8579	Row/column LCD dot-matrix driver	0	1	1	1	1	0	A
PCF8581	128-byte EEPROM	1	0	1	0	A	A	A
PCF8582	256 × 8 EEPROM	1	0	1	0	A	A	A
PCF8583	256 × 8 RAM with clock/calendar	1	0	1	0	0	0	A
PCF8591	4-channel, 8-bit A/D plus 8-bit D/A	1	0	0	1	A	A	A
PCF8594	512-byte EEPROM	1	0	1	0	A	A	A
SAA1064	4-digit LED driver	0	1	1	1	0	A	A
SAA1136	PCM-Audio indent-word interface	0	0	1	1	1	1	0
SAA1300	5-bit high current driver	0	1	0	0	0	A	A
SAA5243/45	Enhanced teletext circuit	0	0	1	0	0	0	1
SAA7191	S-VHS digital multistandard decoder "square pixel"	1	0	0	0	1	A	1
SAA7192	Digital color space converter	1	1	1	0	0	0	A
SAA7199	Digital encoder	1	0	1	1	0	0	0
SAA9020	Field memory controller	0	0	1	0	1	A	A
SAA9051	Digital multi-standard TV decoder	1	0	0	0	1	0	1
SAA9068	(PIPCO) Picture-in-picture controller	0	0	1	0	0	1	A
SAB3035/36/37	(CITAC) CPU interface for tuning and control	1	1	0	0	0	A	A
SAF1135	Data line decoder	0	0	1	0	0	A	A
TDA4670	Picture signal improvement circuit	1	0	0	0	1	0	0
TDA4680	Video processor	1	0	0	0	1	0	0
TDA8421	Hi-fi stereo audio processor	1	0	0	0	0	0	A
TDA8425	Audio processor w/loudspeaker channel	1	0	0	0	0	0	1
TDA8440	Switch for CTV receivers	1	0	0	1	A	A	A
TDA8442	Interface for color decoders	1	0	0	0	1	0	0
TDA8443	YUV/RGB interface circuit	1	1	0	1	A	A	A
TDA8444	Octuple 6-bit DAC	0	1	0	0	A	A	A
TDA8461	PAL/NTSC color decoder	1	0	0	0	1	0	A
TEA6100	FM/IF and tuning interface	1	1	0	0	0	0	1
TEA6300/6310T	Sound fader control circuit	1	0	0	0	0	0	0
TSA5511/12/14	PLL frequency synthesizer for TV	1	1	0	0	0	A	A
TSA6057	Radio tuning PLL frequency synthesizer	1	1	0	0	0	1	A
UMF1009	Frequency synthesizer	1	1	0	0	0	A	A
—	Reserved addresses	1	1	1	1	X	X	X

X = Don't care.
A = Can be connected high or low by the user.

I²C address allocation table

I²C ADDRESS ALLOCATION TABLE

A6–A3	A2–A0							
	0	1	2	3	4	5	6	7
0	General call address	Reserved—	———	———	———	———	———	⟶
1								
2	PCF8200*	SAA5243*			SAA9020*	———	———	⟶
	SAF1135:—	———	———	⟶				
		SAA5245*	SAA9068!—	⟶				
3							SAA1136!	
4	SAA1300!—	———	———	⟶				
	TDA8444!—	———	———	———	———	———	———	⟶
	PCF8574!—	———	———	———	———	———	———	⟶
					PCD3311/A!—	⟶	SA3028	
					PCD3312!—	⟶		
5								
6								
7			PCF8577!	PCF8577A!	PCF8578*	⟶	PCF8566	⟶
					PCF8579*	⟶	!—	
	PCF8576!—	⟶						
	PCF8574*—	———	———	———	———	———		⟶
	SAA1064!—	———	———	⟶			———	
8	TDA8420!—	⟶	TDA8045*		TDA8422!	SAA9050*	SAA9062*	
	TDA8421!—	⟶			TDA8461!—	⟶	SAA9063*	
	TEA6300/T!—	TDA8425!				SAA9051*	SAA9064*	
	TEA6310T!—							
9	TDA8440!—	———	———	———	———	———	———	⟶
	PCF8591*—	———	———	———	———	———	———	⟶
A	PCF8583*—	⟶						
	PCF8570*—	———	———	———	———	———	———	⟶
	PCF8571*—	———	———	———	———	———	———	⟶
	PCF8572*—	———	———	———	———	———	———	⟶
	PCF8582A!—	———	———	———	———	———	———	⟶
B	PCF8570*—	———	———	———	———	———	———	⟶
C	TSA5511*—	———	———	⟶				
	SAB3035*—	———	———	⟶				
	SAB3036*—	———	———	⟶				
	SAB3037*—	———	———	⟶				
		TEA6000*—	TSA6057!—	⟶				
		TEA6100*—						
	TDA8400!—	———	———	⟶				
D	TDA8433!—	———	———	———	———	———	———	⟶
	TDA8443A!—	———	———	———	———	———	———	⟶
	TDA8573*—	———	———	⟶				
E								
F	Reserved—	———	———	———	———	———	———	⟶

Address Format: | A6 | A5 | A4 | A3 | A2 | A1 | A0 | R/W |

Legend: * = R/W, ! = W, : = R

To find a part's address, the most significant 4 bits (A6, A5, A4, and A3) are read from the side of the table. The least significant 3 bits (A2, A1, and A0) are read from the top of the table. For example: SAA1136 is at 36H (0011 110), PCF8577 is at 72H (0111 010). Parts with arrows indicate that a portion of the address is user-configurable. For example: PCF8576 is at address 70H (0111 000) but the last bit (A0) can be set high or low by the user so it can also be at address 71H (0111 001).

80C51 micrcontroller family features guide

PART NO.			MEMORY		COUNTER/	I/O	SERIAL	EXTERNAL	
ROMless	ROM	EPROM	ROM	RAM	TIMER	PORT	INTERFACES	INTERRUPTS	SPECIAL FEATURES
–	83C751	87C751	2k	64	1 (16-bit)	2–3/8	I²C (Bit)	2	Low-cost 24-pin skinny-DIP
–	83C752	87C752	2k	64	1 (16-bit)	2–5/8	I²C (Bit)	2	5-Channel 8-bit A/D, PWM output
8031AH	8051AH	–	4k	128	2	4	UART	2	NMOS
80C31B	80C51B	87C51	4k	128	2	4	UART	2	CMOS
80CL410	83CL410	–	4k	128	2	4	I²C	10	Low voltage (1.8V–6V), low power
80C451	83C451	87C451	4k	128	2	7	UART	2	Extended I/O, Processor bus interface
80C550	83C550	87C550	4k	128	2 + Watchdog	4	UART	2	8-Channel 8-bit A/D
80C851	83C851	–	4k	128	2	4	UART	2	256 Bytes EEPROM, 8051 pin-for-pin compatible
8032AH	8052AH	–	8k	256	3	4	UART	2	NMOS
80C32	80C52	87C52	8k	256	3	4	UART	2	CMOS
80C552	83C552	87C552	8k	256	3 + Watchdog	6	UART, I²C	6	8-Channel 10-bit A/D, 2 PWM outputs
80C562	83C562	–	8k	256	3 + Watchdog	6	UART	6	8-Channel 8-bit A/D, 2 PWM outputs
80C652	83C652	87C652	8k	256	2	4	UART, I²C	2	8051 pin-for-pin compatible with twice the memory
–	83C053	–	8k	192	2 (16-bit)	3-4/8	–	3	On-screen display, 9 PWM outputs, 3 software A/D inputs
–	83C054	87C054	16k	192	2 (16-bit)	3-4/8	–	3	On-screen display, 9 PWM outputs, 3 software A/D inputs
–	83C654	87C654	16k	256	2	4	UART, I²C	2	8051 pin-for-pin compatible with four times the ROM and twice the RAM
80C528	83C528	87C528	32k	512	3 + Watchdog	4	UART, I²C (Bit)	2	The Ultimate Programming Machine
80CL51	83CL51	–	4k	128	2	4	UART	2	Low voltage (1.8V–6V), low power
80C575	83C575	87C575	8k	256	3 + PCA + Watchdog	4	Enhanced UART	2	4 analog comparators, Low Active Reset
80C592	83C592	87C592	16k	512	3+ Watchdog	6	CAN + UART	6	8-Channel 10-bit A/D, 2 PWM outputs, CAN bus interface

80C51 micrcontroller family features guide

	SPEED					TEMPERATURE °C			PACKAGE					
PART NO.	0.5–12	12	16	24	33	0 to 70	–40 to +85	–55 to +125	PDIP	CDIP	PLCC	CLCC	QFP	VSO
83/87C751	X	X	X			X	X	X (–40 to +125)	24	24	28			
83/87C752	X	X	X			X	X	X	28	28	28			
8031/51		X	X (15MHz)			X	X		40		44			
80C31/51/87C51	X	X	X	X	X	X	X	X	40	40	44	44	44	
80/83CL410			X (32kHz–16MHz)				X		40					40
80/83/87C451	X	X	X			X	X	X	64	64	68	68		
80/83/87C550		X	X			X	X	X	40	40	44	44		
80/83C851		X				X	X		40		44		44	
8032/52		X	X (15MHz)			X	X		40		44			
80C32/52/87C52			X	X		X	X	X	40	40	44	44	44	
80/83/87C552			X			X	X	X			68	68		
80/83C562			X			X		X (–40 to+125)			68			
80/83/87C652		X	X			X	X	X (–40 to +125)	40	40	44	44	44	
83C053		X				X			42 SDIP					
83/87C054		X				X			42 SDIP					
83/87C654		X	X			X	X	X (–40 to +125)	40	40	44	44	44	
80/83/87C528	X	X	X			X	X	X	40	40	44	44	44	
80/83CL51			X (32kHz–16MHz)				X		40					40
80/83/87C575			X	X		X	X		40	40	44	44	44	
80/83/87C592			X					X (–40 to +125)			68	68		

NOTE:
All combinations of part type, speed, temperature, and package may not be available.

CMOS and NMOS 8-bit microcontroller family

80C51 FAMILY CMOS

TYPE	ROM/ EPROM	RAM	SPEED (MHz)	PACKAGE	FUNCTIONS	REMARKS	PROBE SDS	METALINK EMULATOR	REMARKS
80C31 80C51 87C51	0 4k ROM 4k EPROM	128 128 128	33 33 33	DIL40, LCC44 QFP44	UART, 2 timers		OM1092 + OM1097 (16MHz)	SUI-8051SD	OM1092: Universal probe OM1095: Upgrade unit
80C32 80C52 87C52	0 8k ROM 8k EPROM	256 256 256	20 20 20	DIL40, LCC44 QFP44	UART, 3 timers		OM4111 + OM4110	SUI-8051SD	
80C451 83C451 87C451	0 4k ROM 4k EPROM	128 128 128	16 16 16	DIP64/LCC68	UART, 2 timers Extended I/O		OM4123	SMI-83C451SD SMI-80C451SD	OM4124: PLCC to DIL OM4125: DIL to PLCC
83C528 87C528	32k ROM 32k EPROM	512 512	16 16	DIL40/LCC44 (QFP44)	UART, 3 timers Watchdog timer Bit I²C		OM4111 + OM4110		OM4110: gen. probe OM4111: probe head OM4120-S for max. speed
83C550 87C550	4k ROM 4k EPROM	128 128	16 16	LCC44 DIL44	UART, 2 timers 8 8-bit ADC inputs, watchdog timer		OM5055		
80C552 83C552 87C552	0 8k ROM 8k EPROM	256 256 256	16 16 16	LCC68/QFP80	UART, 2 timers Timer with compare and capture, 2 PWM outputs, 8 10-bit ADC inputs, Byte I²C		OM1092 + OM1095	SMI-80C552SD	OM1092: Universal probe OM1095: Upgrade unit
80C562 83C562	0 8k ROM	256 256	16 16	LCC68/QFP80	UART, 2 timers Timer with compare and capture, 2 PWM outputs, 8 8-bit ADC inputs	Use 87C552 for development	OM1092 + OM1095	SMI-80C552SD	OM1092: Universal probe OM1095: Upgrade unit
80C575 83C575 87C575	0 8k 8k EPROM	256	16	DIL40, LCC44 QFP44	Enhanced UART, PCA, 4 analog comparators	80/83C575 Production: August '92			
80C592 83C592 87C592	0 16k ROM 16k EPROM	512 512 512	16 16 16	LCC68/QFP80	8XC552 + CAN interface No I²C	Samples: Q4 '91 Production: Q1 '92	OM4110 + OM4112		OM4110: gen. probe OM4112: probe head OM4120S: full speed
80C652 83C652 87C652	0 8k ROM 8k EPROM	256 256 256	12 12 12	DIL40/LCC44 QFP44	UART, 2 timers Byte I²C		OM1092 + OM1096	SMI-80C652SD	

CMOS and NMOS 8-bit microcontroller family

80C51 FAMILY CMOS (Continued)

TYPE	ROM/ EPROM	RAM	SPEED (MHz)	PACKAGE	FUNCTIONS	REMARKS	PROBE SDS	METALINK EMULATOR	REMARKS
83C654 87C654	16k ROM 16k EPROM	256 256	16 16	DIL40/LCC44 QFP44	UART, 2 timers Byte I²C		OM1092 + OM1096		OM1092: Universal probe OM1095: Upgrade unit
83C751 87C751	2k ROM 2k EPROM	64 64	16 16	DIP24 skinny LCC28 DIP24 skinny	1 timer Bit I²C		OM1094P	SMI-80C751SD	
83C752 83C752	2k ROM 2k EPROM	64 64	16 16	DIP28, LCC28 DIP 28, LCC28	1 timer, PWM output, 5 8-bit ADC inputs, Bit I²C		OM5072	SMI-83C752SD	
80C851 83C851 89C851	0 4k ROM	128 128 128	12 12 12	DIL40/LCC44 QFP44	UART, 2 timers 256 byte EEPROM	QFP44 In devel.	OM1092		
83C852	6k ROM	256	16		2k byte EEPROM smart card hardware	In devel.	OM4119		
83C053	8k ROM	192	12	DIP42 Shrunk	2 timers, 14-bit PWM, 8-6 bit PWM 128 char. OSD 3 4-bit A/D inp.		OM5054		
83C054 87C054	16k ROM 16k EPROM	192 192	12 12	DIP42 Shrunk DIP42 Shrunk	As 8XC053		OM5054		

* The following microcontollers have no external memory access: 8XC751, 8XC752, 8XC053, 87C054.

80CLXXX FAMILY CMOS

TYPE	ROM	RAM	SPEED (MHz)	PACKAGE	FUNCTIONS	REMARKS	PROBE SDS	REMARKS
85CL001	0	256	16	PLCC84	UART, 2 timers Byte I²C			
85CL000	0	256	16		UART, 2 timers Byte I²C		OM1079	Piggyback
83CL410	4k	128	16	DIL40 VSO40	2 timers Byte I²C		OM1079	
83CL710	16k	256	16	DIL40	UART, 2 timers Byte I²C	In devel.	OM1079	
80CL51	4k	128	16	DIL40	UART, 2 timers		OM1079	

CMOS and NMOS 8-bit microcontroller family

8051 FAMILY NMOS

TYPE	ROM	RAM	SPEED (MHz)	PACKAGE	FUNCTIONS	REMARKS	PROBE SDS	METALINK EMULATOR	REMARKS
8051 8031	4k 0	128 128	15 15	DIL40/PLCC44 DIL40/PLCC44	UART, 2 timers		OM1091 + OM1097	SUI-8051SD	
8052 8032	8k 0	256 256	15 15	DIL40/PLCC44 DIL40/PLCC44	UART, 3 timers UART, 3 timers		OM4111 + OM4110	SUI-8051SD	

8048 FAMILY NMOS

TYPE	ROM	RAM	SPEED (MHz)	PACKAGE
8048 8035	1k 0	64 64	11 11	DIL40/PLCC44 DIL40/PLCC44
8049 8039	2k 0	128 128	11 11	DIL40/PLCC44 DIL40/PLCC44
8050 8040	4k 0	256 256	11 11	DIL40/PLCC44 DIL40/PLCC44

8048 FAMILY CMOS

TYPE	ROM	RAM	SPEED (MHz)	PACKAGE
80C49 80C39	2k 0	128 128	15 15	DIL40/PLCC44 DIL40/PLCC44

CMOS and NMOS 8-bit microcontroller family

8400 FAMILY CMOS

TYPE	ROM	RAM	SPEED (MHz)	PACKAGE	FUNCTIONS	REMARKS	PROBE SDS	REMARKS
84C21 84C41 84C81 84C41C	2k 4k 8k 4k	64 128 256 128	10 10 10 12	DIL28/SO28 DIL28/SO28 DIL28/SO28 DIL28/SO28	20 I/O lines 8-bit timer Byte I²C		OM1083	
84C12 84C22 84C42 84C12A	1k 2k 4k 1k	64 64 64 64	10 10 10 16	DIL20/SO20 DIL20/SO20 DIL20/SO20 DIL20/SO20	13 I/O lines 8-bit timer		OM1083	
84C00B 84C00T	0 0	256 256	10 10	28 pins VSO-56	20 I/O lines 8-bit timer Byte I²C	Piggyback ROMless	OM1080	
84C121 84C121B	1k 0	64 64	10 10	DIL20/SO20	13 I/O lines 2 8-bit timers 8 bytes EEPROM	 Piggyback	OM1073	
84C122	1k	32	10	SO20/SO24	Controller for remote control			
84C230	2l	64	10	DIL40/VSO40	12 I/O lines 8-bit timer 16*4 LCD drive		OM1072	
84C430 84C430B	4k 0	128 128	10 10	QFP64	24 I/O lines 8-bit timer Byte I²C 24*4 LCD drive	 Piggyback for C230 and C430	OM1072	
84C633 84C633B	6k 0	256 256	16 16	VSO56	28 I/O lines 8-bit timer 16-bit up/down counter 16-bit timer with compare and capture 16*4 LCD drive		OM1086	
84C440 84C441 84C640 84C641 84C643 84C644 84C840 84C841 84C843 84C844	4k 4k 6k 6k 6k 6k 8k 8k 8k 8k	128 128 128 128 128 128 192 192 192 192	10 10 10 10 10 10 10 10 10 10	DIP42 shrunk	RC: 29 I/O lines LC: 28 I/O lines 8-bit timer 1 14-bit PWM 5 6-bit PWM 3-bit ADC OSD 2L-16	I²C, RC I²C, LC I²C, RC I²C, LC RC ,Q2 '90 LC ,Q2 '90 I²C, RC ,Q2 '90 I²C, LC ,Q2 '90 RC ,Q2 '90 LC ,Q2 '90	OM1074	For emulation of LC versions, use OM1074 + adapter_3
84C646 84C846	6k 8k	192 192	10 10	DIP42 shrunk	tbf	I²C, RC ,Q4 '90 I²C, RC ,Q4 '90	tbf	
84C647 84C847	6k 8k	192 192	10 10	DIP42 shrunk	tbf	I²C, LC ,Q4 '90 I²C, LC ,Q4 '90	tbf	

CMOS and NMOS 8-bit microcontroller family

8400 FAMILY CMOS (Continued)

TYPE	ROM	RAM	SPEED (MHz)	PACKAGE	FUNCTIONS	REMARKS	PROBE SDS	REMARKS
84C85	8k	256	10	DIL40/VSO40	32 I/O lines 8-bit timer Byte I²C		CM1070	
84C85B	0	256	10			Piggyback for C85		
84C853	8k	256	16	DIL40/VSO40	33 I/O lines 8-bit timer 16-bit up/down counter 16-bit timer with compare and capture		OM1081	Q3 '90
84C853B	0	256	16			Piggyback for C853		
84C270	2k	128	10	DIL40/VSO40	8 I/O lines 16*8 capture keyboard matrix 8-bit timer		OM1077	
84C470	4k	128	10	DIL40/VSO40				
84C270B	0	128	10			Piggyback for C270		
84C470B	0	128	10		470 also handles mech. keys	Piggyback for C470		
84C271	2k	128	10	DIL40	8 I/O lines 16*8 mech. keyboard matrix 8-bit timer		OM1078	

8400 FAMILY NMOS

TYPE	ROM	RAM	SPEED (MHz)	PACKAGE	FUNCTIONS	REMARKS	EMULATOR TOOLS	REMARKS
8411	1k	64	6	DIL28/SO28	20 I/O lines 8-bit timer Byte I²C		OM1084	
8421	2k	64	6	DIL28/SO28				
8441	4k	128	6	DIL28/SO28				
8461	6k	128	6	DIL28/SO28				
8422	2k	64	6	DIL20	13 I/O lines 8-bit timer Bit I²C		PM8327/20 + PM8447	On PMDS
8442	4k	128	6	DIL20				
8401B	0	128	6	28-pin PLCC68		Piggyback for 84X1 Bond out		
8401WP	0	128	6					

CMOS and NMOS 8-bit microcontroller family

3300 FAMILY CMOS

TYPE	ROM	RAM	SPEED (MHz)	PACKAGE	FUNCTIONS	REMARKS	PROBE SDS	REMARKS
3315	1.5k	160	10	DIL28/SO28	20 I/O lines 8-bit timer V_{DD} > 1.8V		OM1083	
3343	3k	224	10	DIL28/SO28	20 I/O lines 8-bit timer V_{DD} > 1.8V Byte I²C		OM1083	
3344	2k	224	3.58	DIL28/SO28	20 I/O lines 8-bit timer DTMF generator		OM1071	
3346	4k	128	10	DIL28/SO28	20 I/O lines 8-bit timer Byte I²C 256 bytes EEPROM V_{DD} < 1.8V		OM1076	
3347	1.5k	64	3.58	DIL20/SO20	12 I/O lines 8-bit timer DTMF generator		OM1071 + Adapter_2	
3348	8k	256	10	DIL28/SO28	20 I/O lines 8-bit timer Byte I²C V_{DD} < 1.8V		OM1083	
3349	4k	224	3.58	DIL28/SO28	20 I/O lines 8-bit timer DTMF generator		OM1071	
3350A	8k	128	3.58	VSO64	30 I/O lines 8-bit timer DTMF generator 256 bytes EEPROM	To be developed		
3351A	2k	64	3.58	DIL28/SO28	20 I/O lines 8-bit timer DTMF generator 128 bytes EEPROM		OM5000	
3352A	6k	128	3.58	DIL28/SO28	20 I/O lines 8-bit timer DTMF generator 128 byte EEPROM		OM5000	
3301B						Piggyback for 3315, 3343, 3348	OM1083	
3344B						Piggyback for 3344, 3347, 3349	OM1071	
3346B						Piggyback for 3346	OM1076	

CMOS 16-bit microcontroller family

16-BIT CONTROLLERS

TYPE	(EP)ROM	RAM	EEPROM	SPEED (MHz)	FUNCTIONS	REMARKS	DEVELOPMENT TOOLS
68070	–	–	–	17.5	2 DMA channels, MMU, UART, 16-bit timer, I²C, 68000 bus interface, 16Mb address range		OM4160 Microcore OM4161 (SBE68070) TRACE32-ICE68070 (Lauterbach) OM4222 90C Development system (planned)
93C101	34k	512		15	Derivative with low power modes	Low power micro-controller	
93C110 90C110 93C100 90C100 97C100	34k – 34k – 32k (EPROM)	512 512 512 512 512	256 256 – – –	15 15	UART, I²C, 3 16-bit timers, 80C51 interface, 68000 interface, 40 I/O lines, 2Mb address range		OM4160/3 Microcore 3 OM4201WP (SBE90C110) OM4220 90C Development system TRACE32 – ICE93C110 (Lauterbach)

16-BIT MICROCONTROLLER FAMILY[1]

PART NO.	ROM	RAM	EEPROM	16-BIT I/O PORTS	SERIAL I/O	DMA CHANNELS	COUNTER/ TIMER	EXTERNAL INTERRUPTS	SPEED MHz	PACKAGES	SPECIAL FEATURES
68070	–	–	–	–	UART, I²C	2	1[2]	6	10, 12, 15, 17.5	PLCC84 QFP120	Memory management unit 68000 bus interface
90C100	–	512	–	2 + 1/2	UART, I²C	–	1[2]	8	15	PLCC84 QFP80	80C51 bus interface 68000 bus interface
93C100	34k	512	–	2 + 1/2	UART, I²C	–	1[2]	8	15	PLCC84 QFP80	80C51 bus interface 68000 bus interface
97C100	32k EPROM	512	–	2 + 1/2	UART, I²C	–	1[2]	8	15	PLCC84 CLCC84 QFP80	80C51 bus interface 68000 bus interface

NOTES:
1. 68000 software compatible.
2. 16-bit timer with two match/count/capture registers.

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(408) 991-3459

Section 1
Inter-Integrated (I^2C) Circuit Bus

INDEX

I²C -bus specification (including fast-mode)

PREFACE

This specification is an updated version including the following latest modifications:

- Programming of a slave address by software has been omitted. The realization of this feature is rather complicated and has not been used.
- The 'low-speed mode' has been omitted. This mode is, in fact, a subset of the total I²C-bus specification and need not be specified explicitly.
- The 'fast-mode' is added. This allows a fourfold increase of bit rate up to 400 kbit/s. Fast-mode devices are downwards compatible i.e. they can be used in a 0 to 100 kbit/s I²C-bus system.
- 10-bit addressing is added. This allows 1024 additional slave addresses.
- Slope control and input filtering for fast-mode devices is specified to improve the EMC behaviour.

NOTE

Neither the 100 kbit/s I²C-bus system nor the 100 kbit/s devices have been changed.

I²C -bus specification (including fast-mode)

1.0 INTRODUCTION

For 8-bit applications, such as those requiring single-chip microcontrollers, certain design criteria can be established:

- A complete system usually consists of at least one microcontroller and other peripheral devices such as memories and I/O expanders.
- The cost of connecting the various devices within the system must be minimized.
- Such a system usually performs a control function and doesn't require high-speed data transfer.
- Overall efficiency depends on the devices chosen and the interconnecting bus structure.

In order to produce a system to satisfy these criteria, a serial bus structure is needed. Although serial buses don't have the throughput capability of parallel buses, they do require less wiring and fewer connecting pins. However, a bus is not merely an interconnecting wire, it embodies all the formats and procedures for communication within the system.

Devices communicating with each other on a serial bus must have some form of protocol which avoids all possibilities of confusion, data loss and blockage of information. Fast devices must be able to communicate with slow devices. The system must not be dependent on the devices connected to it, otherwise modifications or improvements would be impossible. A procedure has also to be devised to decide which device will be in control of the bus and when. And, if different devices with different clock speeds are connected to the bus, the bus clock source must be defined. All these criteria are involved in the specification of the I²C-bus.

2.0 THE I²C-BUS CONCEPT

Any IC fabrication process (NMOS, CMOS, bipolar) can be supported by the I²C-bus. Two wires, serial data (SDA) and serial clock (SCL), carry information between the devices connected to the bus. Each device is recognised by a unique address - whether it's a microcontroller, LCD driver, memory or keyboard interface - and can operate as either a transmitter or receiver, depending on the function of the device. Obviously an LCD driver is only a receiver, whereas a memory can both receive and transmit data. In addition to transmitters and receivers, devices can also be considered as masters or slaves when performing data transfers (see Table 1). A master is the device which initiates a data transfer on the bus and generates the clock signals to permit that transfer. At that time, any device addressed is considered a slave.

The I²C-bus is a multi-master bus. This means that more than one device capable of controlling the bus can be connected to it. As masters are usually micro-controllers, let's consider the case of a data transfer between two microcontrollers connected to the I²C-bus (Fig.1). This highlights the master-slave and receiver-transmitter relationships to be found on the I²C-bus. It should be noted that these relationships are

Table 1 Definition of I²C-bus terminology

Term	Description
Transmitter	The device which sends the data to the bus
Receiver	The device which receives the data from the bus
Master	The device which initiates a transfer, generates clock signals and terminates a transfer
Slave	The device addressed by a master
Multi-master	More than one master can attempt to control the bus at the same time without corrupting the message
Arbitration	Procedure to ensure that, if more than one master simultaneously tries to control the bus, only one is allowed to do so and the message is not corrupted
Synchronization	Procedure to synchronize the clock signals of two or more devices

I²C -bus specification (including fast-mode)

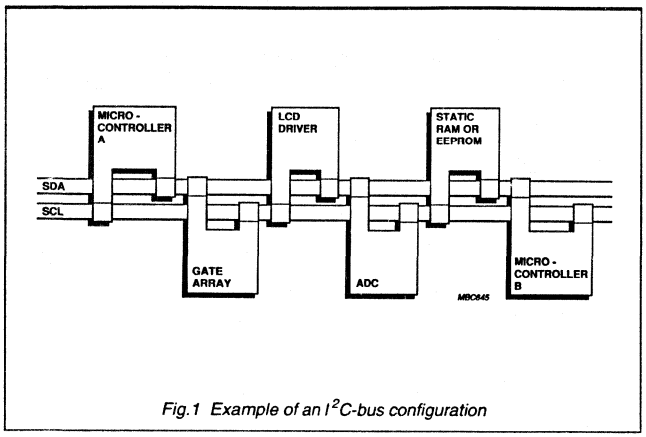


Fig.1 Example of an I²C-bus configuration

not permanent, but only depend on the direction of data transfer at that time. The transfer of data would proceed as follows:

1) Suppose microcontroller A wants to send information to microcontroller B:

- microcontroller A (master), addresses microcontroller B (slave)
- microcontroller A (master-transmitter), sends data to microcontroller B (slave-receiver)
- microcontroller A terminates the transfer.

2) If microcontroller A wants to receive information from microcontroller B:

- microcontroller A (master) addresses microcontroller B (slave)
- microcontroller A (master-receiver) receives data from microcontroller B (slave-transmitter)
- microcontroller A terminates the transfer.

Even in this case, the master (microcontroller A) generates the timing and terminates the transfer.

The possibility of connecting more than one microcontroller to the I²C-bus means that more than one master could try to initiate a data transfer at the same time. To avoid the chaos that might ensue from such an event - an arbitration procedure has been developed. This procedure relies on the wired-AND connection of all I²C interfaces to the I²C-bus.

If two or more masters try to put information onto the bus, the first to produce a 'one' when the other produces a 'zero' will lose the arbitration. The clock signals during arbitration are a synchronised combination of the clocks generated by the masters using the wired-AND connection to the SCL line (for more detailed information concerning arbitration see section 6.0).

Generation of clock signals on the I²C-bus is always the responsibility of master devices; each master generates its own clock signals when transferring data on the bus. Bus clock signals from a master can only be altered when they are stretched by a slow-slave device holding-down the clock line, or by another master when arbitration occurs.

3.0 GENERAL CHARACTERISTICS

Both SDA and SCL are bidirectional lines, connected to a positive supply voltage via a pull-up resistor (see Fig.2). When the bus is free, both lines are HIGH. The output stages of devices connected to the bus must have an open-drain or open-collector in order to perform the wired-AND function. Data on the I²C-bus can be transferred at a rate up to 100 kbit/s in the standard-mode, or up to 400 kbit/s in the fast-mode. The number of interfaces connected to the bus is solely dependent on the limiting bus capacitance of 400 pF.

4.0 BIT TRANSFER

Due to the variety of different technology devices (CMOS, NMOS, bipolar) which can be connected to the I²C-bus, the levels of the logical '0' (LOW) and '1' (HIGH) are not fixed and depend on the associated level of V_{DD} (see Section 15.0 for

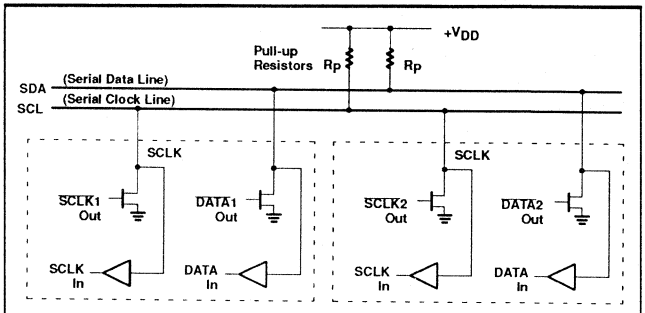


Fig.2 Connection of I²C-bus devices to the I²C-bus

I²C -bus specification (including fast-mode)

Electrical specifications). One clock pulse is generated for each data bit transferred.

4.1 Data validity

The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW (Fig.3).

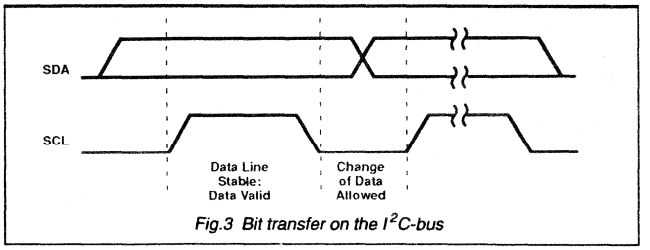


Fig.3 Bit transfer on the I²C-bus

4.2 START and STOP conditions

Within the procedure of the I²C-bus, unique situations arise which are defined as START and STOP conditions (see Fig.4).

A HIGH to LOW transition of the SDA line while SCL is HIGH is one such unique case. This situation indicates a START condition.

A LOW to HIGH transition of the SDA line while SCL is HIGH defines a STOP condition.

START and STOP conditions are always generated by the master. The bus is considered to be busy after the START condition. The bus is considered to be free again a certain time after the STOP condition. This bus free situation will be specified later (in Section 15.0).

Detection of START and STOP conditions by devices connected to the bus is easy if they incorporate the necessary interfacing hardware. However,

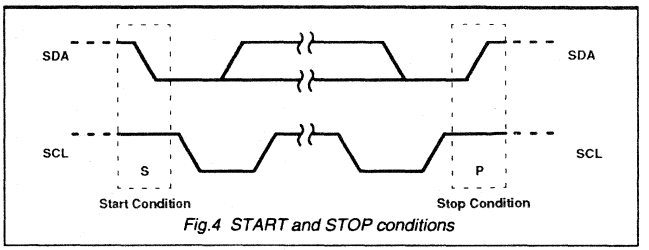


Fig.4 START and STOP conditions

microcontrollers with no such interface have to sample the SDA line at least twice per clock period in order to sense the transition.

5.0 TRANSFERRING DATA

5.1 Byte format

Every byte put on the SDA line must be 8-bits long. The number of bytes that can be transmitted per transfer is unrestricted. Each byte has to be followed by an acknowledge bit. Data is transferred with the most significant bit (MSB) first (Fig.5). If a receiver can't receive another complete byte of data until it has performed some other function, for example, servicing an internal interrupt, it can hold the clock line SCL LOW to force the transmitter into a wait state. Data transfer then continues when the receiver is ready for another byte of data and releases clock line SCL.

In some cases, it's permitted to use a different format from the I²C-bus format (for CBUS compatible devices for example). A message which starts with such an address can be terminated by generation of a STOP condition, even during the transmission of a byte. In this case, no acknowledge is generated (see section 8.1.3).

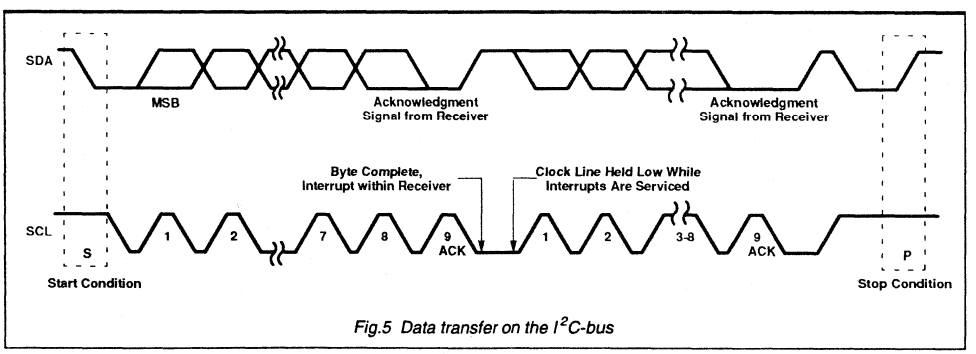


Fig.5 Data transfer on the I²C-bus

I²C -bus specification (including fast-mode)

5.2 Acknowledge

Data transfer with acknowledge is obligatory. The acknowledge-related clock pulse is generated by the master. The transmitter releases the SDA line (HIGH) during the acknowledge clock pulse.

The receiver has to pull down the SDA line during the acknowledge clock pulse so that it remains stable LOW during the high period of this clock pulse (Fig.6). Of course, set-up and hold times must also be taken into account and these will be described in Section 15.0.

Usually, a receiver which has been addressed is obliged to generate an acknowledge after each byte has been received (except when the message starts with a CBUS address - see section 8.1.3).

When a slave-receiver doesn't acknowledge on the slave address (for example, it's unable to receive because it's performing some real-time function), the data line has to be left HIGH by the slave. The master can then generate a STOP condition to abort the transfer.

If a slave-receiver does acknowledge the slave address but, some time later in the transfer cannot receive any more data bytes, the master must again abort the transfer. This is indicated by the slave generating the not acknowledge on the first byte to follow. The slave leaves the data line HIGH and the master generates the STOP condition.

If a master-receiver is involved in a transfer, it must signal the end of data to the slave-transmitter by not generating an acknowledge on the last byte that was clocked out of the slave. The slave-transmitter must release the data line to allow the master to generate the STOP condition.

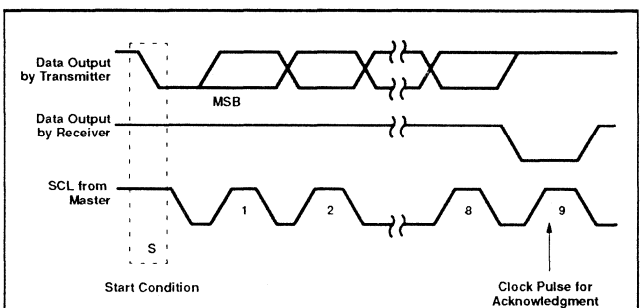


Fig.6 Acknowledge on the I²C-bus

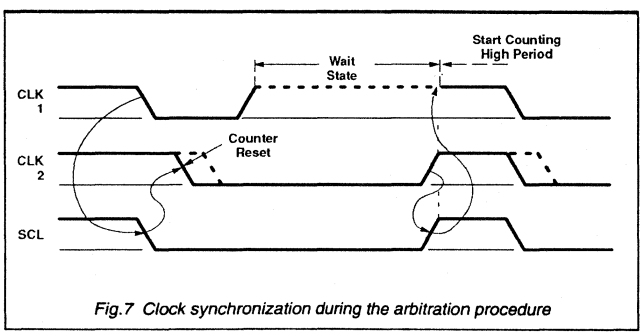


Fig.7 Clock synchronization during the arbitration procedure

6.0 ARBITRATION AND CLOCK GENERATION

6.1 Synchronization

All masters generate their own clock on the SCL line to transfer messages on the I²C-bus. Data is only valid during the clock HIGH period. A defined clock is therefore needed for the bit-by-bit arbitration procedure to take place.

Clock synchronization is performed using the wired-AND connection of I²C interfaces to the SCL line. This means that a HIGH to LOW transition on the SCL line will cause the devices concerned to start counting off their LOW period and, once a device clock has gone LOW, it will hold the SCL line in that state until the clock HIGH state is reached (Fig.7). However, the LOW to HIGH transition of this clock may not change the state of the SCL line if another clock is still within its LOW period. Therefore, the SCL line will be held LOW by the device with the longest LOW period. Devices with shorter LOW periods enter a HIGH wait-state during this time.

When all devices concerned have counted off their LOW period, the clock line will be released and go HIGH. There will then be no difference between the device clocks and the state of the SCL line and all the devices will start counting their HIGH periods. The first device to complete its HIGH period will again pull the SCL line LOW.

In this way, a synchronised SCL clock is generated with its LOW period determined by the device with the longest clock LOW period, and its HIGH period

I²C -bus specification (including fast-mode)

determined by the one with the shortest clock HIGH period.

6.2 Arbitration

A master may start a transfer only if the bus is free. Two or more masters may generate a START condition within the minimum hold time ($t_{HD;STA}$) of the START condition which results in a defined START condition to the bus.

Arbitration takes place on the SDA line, while the SCL line is at the HIGH level, in such a way that the master which transmits a HIGH level, while another master is transmitting a LOW level will switch off its DATA output stage because the level on the bus doesn't correspond to its own level.

Arbitration can continue for many bits. Its first stage is comparison of the address bits (addressing information is in Sections 8.0 and 12.0). If the masters are each trying to address the same device, arbitration continues with comparison of the data. Because address and data information on the I²C-bus is used for arbitration, no information is lost during this process.

A master which loses the arbitration can generate clock pulses until the end of the byte in which it loses the arbitration.

If a master also incorporates a slave function and it loses arbitration during the addressing stage, it's possible that the winning master is trying to address it. The losing master must therefore switch over immediately to its slave-receiver mode.

Figure 8 shows the arbitration procedure for two masters. Of course, more may be involved (depending on how many masters are connected to the bus). The moment there is a difference between the internal data level of the master generating DATA 1 and the actual level on the SDA line, its data output is switched off, which means that a HIGH output level is then connected to the bus. This will not affect the data transfer initiated by the winning master. Since control of the I²C-bus is decided solely on the address and data sent by competing masters, there is no central master, nor any order of priority on the bus.

Special attention must be paid if, during a serial transfer, the arbitration procedure is still in progress at the moment when a repeated START condition or a STOP condition is transmitted to the I²C-bus. If it's possible for such a situation to occur, the masters involved must send this repeated START condition or STOP condition at the same position in the format frame. In other words, arbitration isn't allowed between:

- A repeated START condition and a data bit
- A STOP condition and a data bit
- A repeated START condition and a STOP condition.

6.3 Use of the clock synchronising mechanism as a handshake

In addition to being used during the arbitration procedure, the clock synchronization mechanism can be used to enable receivers to cope with fast data transfers, on either a byte level or a bit level.

On the byte level, a device may be able to receive bytes of data at a fast rate, but needs more time to store a received byte or prepare another byte to be transmitted. Slaves can then hold the SCL line LOW after reception and acknowledgement of a byte to force the master into a wait state until the slave is ready for the next byte transfer in a type of handshake procedure.

On the bit level, a device such as a microcontroller without, or with only a limited hardware I²C interface on-chip can slow down the bus clock by extending each clock LOW period. In this way, the speed of any master is adapted to the internal operating rate of this device.

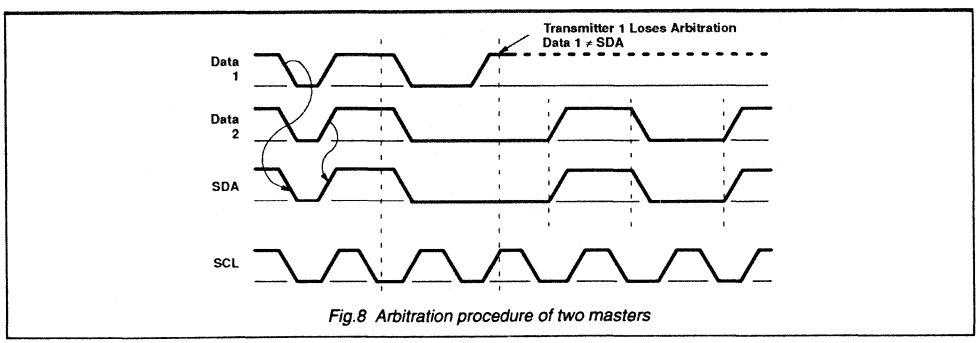


Fig.8 Arbitration procedure of two masters

I²C -bus specification (including fast-mode)

7.0 FORMATS WITH 7-BIT ADDRESSES

Data transfers follow the format shown in Fig.9. After the START condition (S), a slave address is sent. This address is 7 bits long followed by an eighth bit which is a data direction bit (R/$\overline{W}$) - a 'zero' indicates a transmission (WRITE), a 'one' indicates a request for data (READ). A data transfer is always terminated by a STOP condition (P) generated by the master. However, if a master still wishes to communicate on the bus, it can generate a repeated START condition (Sr) and address another slave without first generating a STOP condition. Various combinations of read/write formats are then possible within such a transfer.

Possible data transfer formats are:

- Master-transmitter transmits to slave-receiver. The transfer direction is not changed (Fig.10).

- Master reads slave immediately after first byte (Fig.11). At the moment of the first acknowledge, the master-transmitter becomes a master-receiver and the slave-receiver becomes a slave-transmitter. This acknowledge is still generated by the slave. The STOP condition is generated by the master.

- Combined format (Fig.12). During a change of direction within a transfer, the START condition and the slave address are both repeated, but with the R/$\overline{W}$ bit reversed.

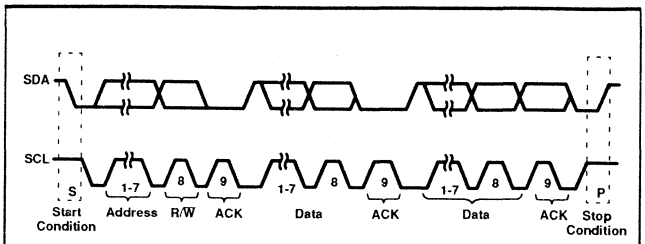


Fig.9 A complete data transfer

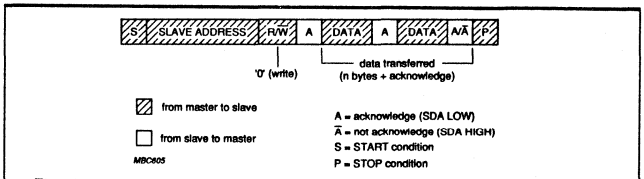


Fig.10 A master-transmitter addresses a slave-receiver with a 7-bit address. The transfer direction is not changed

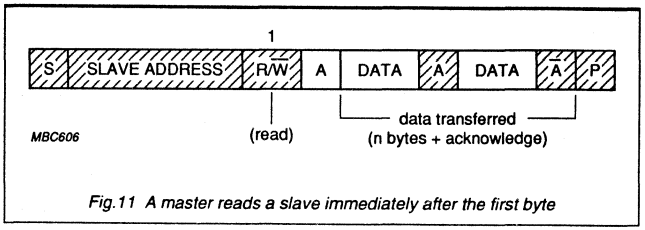


Fig.11 A master reads a slave immediately after the first byte

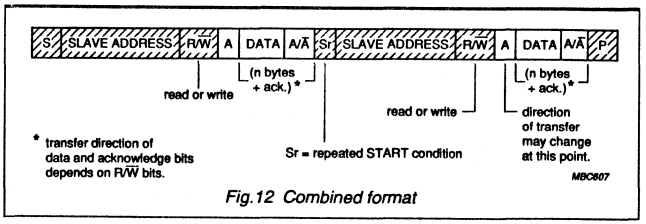


Fig.12 Combined format

NOTES:

1) Combined formats can be used, for example, to control a serial memory. During the first data byte, the internal memory location has to be written. After the START condition and slave address is repeated, data can be transferred.
2) All decisions on auto-increment or decrement of previously accessed memory locations etc. are taken by the designer of the device.
3) Each byte is followed by an acknowledgement bit as indicated by the A or Ā blocks in the sequence.
4) I²C-bus compatible devices must reset their bus logic on receipt of a START or repeated START condition such that they all anticipate the sending of a slave address.

I²C -bus specification (including fast-mode)

8.0 7-BIT ADDRESSING (see section 13 for 10-bit addressing)

The addressing procedure for the I²C-bus is such that the first byte after the START condition usually determines which slave will be selected by the master. The exception is the 'general call' address which can address all devices. When this address is used, all devices should, in theory, respond with an acknowledge. However, devices can be made to ignore this address. The second byte of the general call address then defines the action to be taken. This procedure is explained in more detail in Section 8.1.1.

8.1 Definition of bits in the first byte

The first seven bits of the first byte make up the slave address (Fig.13). The eighth bit is the LSB (least significant bit). It determines the direction of the message. A 'zero' in the least significant position of the first byte means that the master will write information to a selected slave. A 'one' in this position means that the master will read information from the slave.

When an address is sent, each device in a system compares the first 7 bits after the START condition with its address. If they match, the device considers itself addressed by the master as a slave-receiver or slave-transmitter, depending on the R/$\overline{W}$ bit.

A slave address can be made-up of a fixed and a programmable part. Since it's likely that there will be several identical devices in a system, the programmable part of the slave address enables the maximum possible number of such devices to be connected to the I²C-bus. The number of programmable address bits of a device depends on the number of pins available. For example, if a device has 4 fixed and 3 programmable address bits, a total of 8 identical devices can be connected to the same bus.

The I²C-bus committee coordinates allocation of I²C addresses. Further information can be obtained fom the Philips representatives listed on the back cover. Two groups of eight addresses (0000XXX and 1111XXX) are reserved for the purposes shown in Table 2. The bit combination 11110XX of the slave address is reserved for 10-bit addressing (see Section 13.0).

Table 2 Definition of bits in the first byte

Slave address	R/$\overline{W}$ bit	Description
0000 000	0	General call address
0000 000	1	START byte
0000 001	X	CBUS address
0000 010	X	Address reserved for different bus format
0000 011	X	Reserved for future purposes
0000 1XX	X	
1111 1XX	X	
1111 0XX	X	10-bit slave addressing

NOTES:

1) No device is allowed to acknowledge at the reception of the START byte.
2) The CBUS address has been reserved to enable the inter-mixing of CBUS compatible and I²C-bus compatible devices in the same system. I²C-bus compatible devices are not allowed to respond on reception of this address.
3) The address reserved for a different bus format is included to enable I²C and other protocols to be mixed. Only I²C-bus compatible devices that can work with such formats and protocols are allowed to respond to this address.

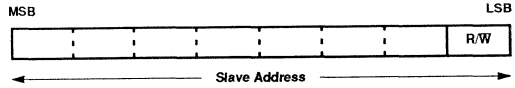


Fig.13 The first byte after the START procedure

I²C -bus specification (including fast-mode)

8.1.1 General call address

The general call address should be used to address every device connected to the I²C-bus. However, if a device doesn't need any of the data supplied within the general call structure, it can ignore this address by not acknowledging. If a device does require data from a general call address, it will acknowledge this address and behave as a slave-receiver. The second and following bytes will be acknowledged by every slave-receiver capable of handling this data. A slave which cannot process one of these bytes must ignore it by not acknowledging. The meaning of the general call address is always specified in the second byte (Fig.14).

There are two cases to consider:

- When the least significant bit B is a 'zero'.
- When the least significant bit B is a 'one'.

When B is a 'zero'; the second byte has the following definition:

- 00000110 (H'06'). Reset and write programmable part of slave address by hardware. On receiving this 2-byte sequence, all devices designed to respond to the general call address will reset and take in the programmable part of their address. Precautions have to be taken to ensure that a device is not pulling down the SDA or SCL line after applying the supply voltage, since these low levels would block the bus
- 00000100 (H'04'). Write programmable part of slave address by hardware. All devices which define the programmable part of their address by hardware (and which respond to the general call address) will latch this programmable part at the reception of this two byte sequence. The device will not reset.
- 00000000 (H'00'). This code is not allowed to be used as the second byte.

Sequences of programming procedure are published in the appropriate device data sheets.

The remaining codes have not been fixed and devices must ignore them.

When B is a 'one'; the 2-byte sequence is a 'hardware general call'. This means that the sequence is transmitted by a hardware master device, such as a keyboard scanner, which cannot be programmed to transmit a desired slave address. Since a hardware master doesn't know in advance to which device the message has to be transferred, it can only generate this hardware general call and its own address - identifying itself to the system (Fig.15).

The seven bits remaining in the second byte contain the address of the hardware master. This address is recognised by an intelligent device, such as a microcontroller, connected to the bus which will then direct the information from the hardware master. If the hardware master can also act as a slave, the slave address is identical to the master address.

In some systems, an alternative could be that the hardware master

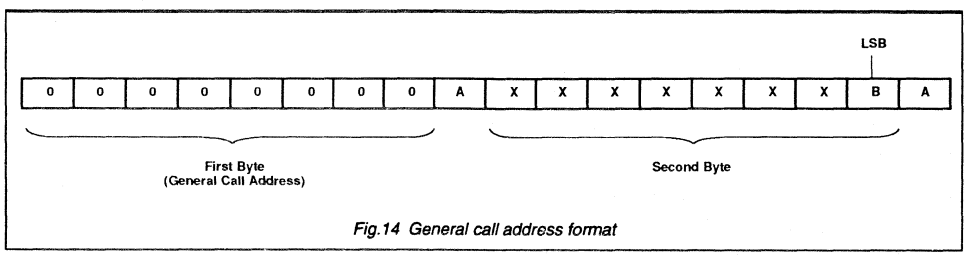


Fig.14 General call address format

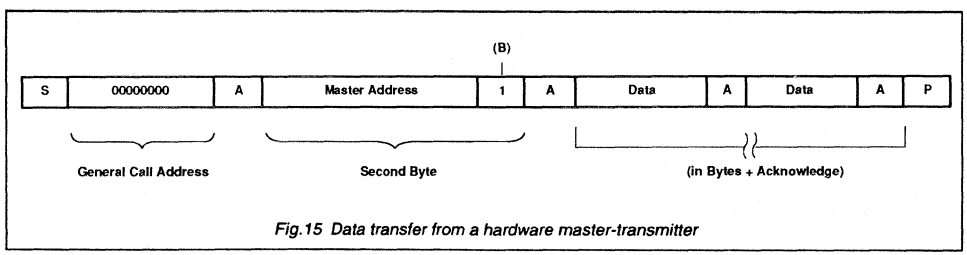


Fig.15 Data transfer from a hardware master-transmitter

I²C -bus specification (including fast-mode)

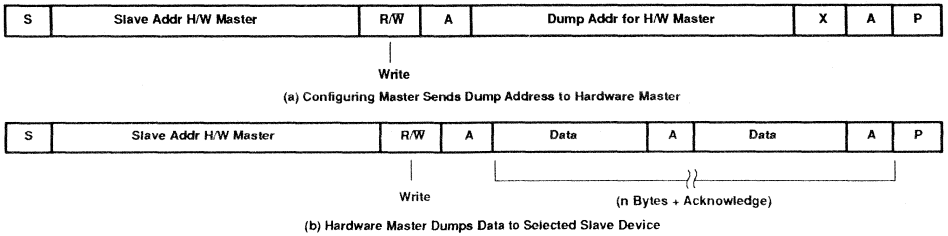


Fig.16 Data transfer by a hardware-transmitter capable of dumping data directly to slave devices (a) Configuring master sends dump address to hardware master (b) Hardware master dumps data to selected slave

transmitter is set in the slave-receiver mode after the system reset. In this way, a system configuring master can tell the hardware master-transmitter (which is now in slave-receiver mode) to which address data must be sent (Fig.16). After this programming procedure, the hardware master remains in the master-transmitter mode.

8.1.2 START byte

Microcontrollers can be connected to the I²C-bus in two ways. A microcontroller with an on-chip hardware I²C-bus interface can be programmed to be only interrupted by requests from the bus. When the device doesn't have such an interface, it must constantly monitor the bus via software. Obviously, the more times the microcontroller monitors, or polls, the bus the less time it can spend carrying out its intended function. There is therefore a speed difference between fast hardware devices and a relatively slow microcontroller which relies on software polling.

In this case, data transfer can be preceded by a start procedure which is much longer than normal (Fig.17). The start procedure consists of:

- A START condition (S)
- A START byte (00000001)
- An acknowledge clock pulse (ACK)
- A repeated START condition (Sr).

After the START condition S has been transmitted by a master which requires bus access, the START byte (00000001) is transmitted. Another microcontroller can therefore sample the SDA line at a low sampling rate until one of the seven zeros in the START byte is detected. After detection of this LOW level on the SDA line, the microcontroller can switch to a higher sampling rate to find the repeated START condition Sr which is then used for synchronization.

A hardware receiver will reset on receipt of the repeated START condition Sr and will therefore ignore the START byte.

An acknowledge-related clock pulse is generated after the START byte. This is present only to conform with the byte handling format used on the bus. No device is allowed to acknowledge the START byte.

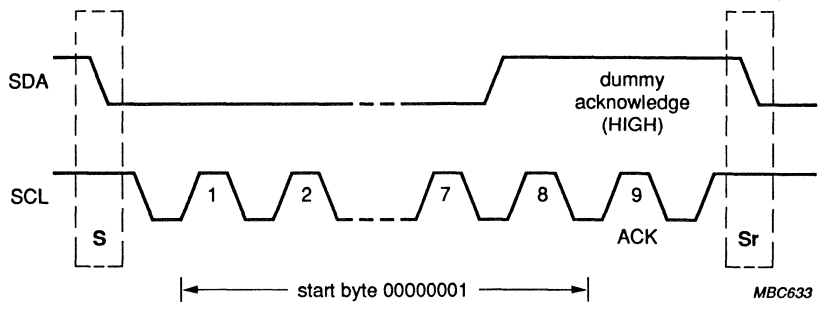


Fig.17 START byte procedure

I²C -bus specification (including fast-mode)

8.1.3 CBUS compatibility

CBUS receivers can be connected to the I²C-bus. However, a third line called DLEN must then be connected and the acknowledge bit omitted. Normally, I²C transmissions are sequences of 8-bit bytes; CBUS compatible devices have different formats.

In a mixed bus structure, I²C-bus devices must not respond to the CBUS message. For this reason, a special CBUS address (0000001X) to which no I²C-bus compatible device will respond, has been reserved. After transmission of the CBUS address, the DLEN line can be made active and a CBUS-format transmission (Fig.18) sent. After the STOP condition, all devices are again ready to accept data.

Master-transmitters can send CBUS formats after sending the CBUS address. The transmission is ended by a STOP condition, recognised by all devices.

NOTE: If the CBUS configuration is known, and expansion with CBUS compatible devices isn't foreseen, the designer is allowed to adapt the hold time to the specific requirements of the device(s) used.

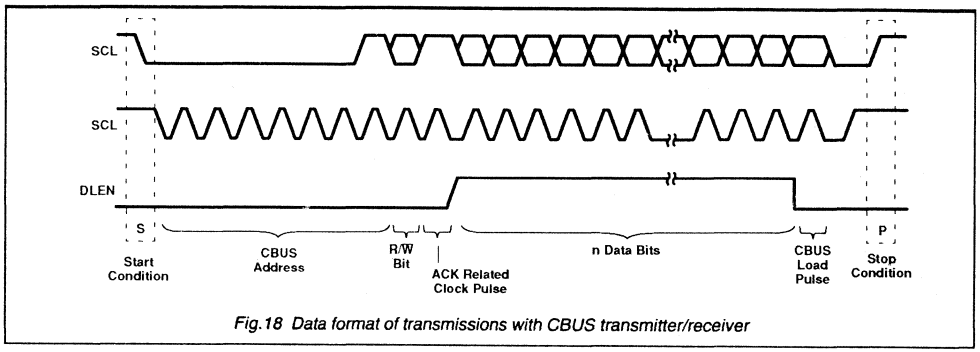


Fig.18 Data format of transmissions with CBUS transmitter/receiver

I²C -bus specification (including fast-mode)

9.0 ELECTRICAL CHARACTERISTICS FOR I²C-BUS DEVICES

The electrical specifications for the I/Os of I²C-bus devices and the characteristics of the bus lines connected to them are given in Tables 3 and 4 in Section 15.

I²C-bus devices with fixed input levels of 1.5 V and 3 V can each have their own appropriate supply voltage. Pull-up resistors must be connected to a 5 V ± 10% supply (Fig.19). I²C-bus devices with input levels related to V_{DD} must have one common supply line to which the pull-up resistor is also connected (Fig.20).

When devices with fixed input levels are mixed with devices with input levels related to V_{DD}, the latter devices must be connected to one common supply line of 5 V ± 10% and must have pull-up resistors connected to their SDA and SCL pins as shown in Fig.21.

Input levels are defined in such a way that:

- The noise margin on the LOW level is 0.1 V_{DD}
- The noise margin on the HIGH level is 0.2 V_{DD}
- Series resistors (R_S) of e.g. 300 Ω can be used for protection against high voltage spikes on the SDA and SCL line due to flash-over of a TV picture tube, for example (Fig.22).

9.1 Maximum and minimum values of resistors R_p and R_s

In a standard-mode I²C-bus system the values of resistors R_p and R_s in Fig.22 depend on the following parameters:

1) Supply voltage
2) Bus capacitance
3) Number of connected devices (input current + leakage current)

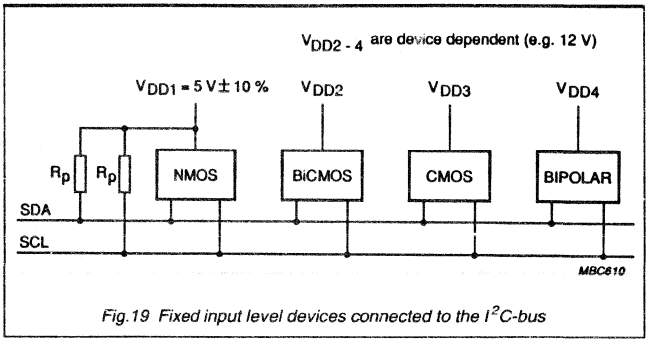


Fig.19 Fixed input level devices connected to the I²C-bus

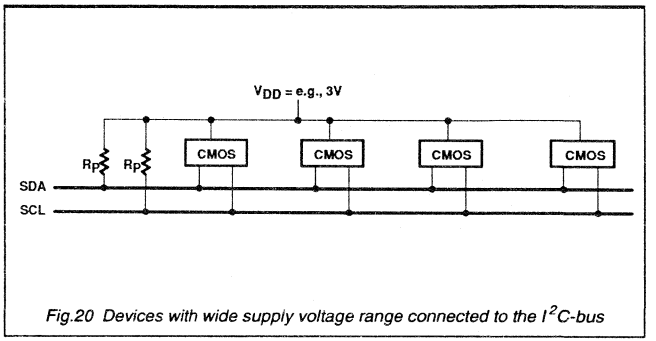


Fig.20 Devices with wide supply voltage range connected to the I²C-bus

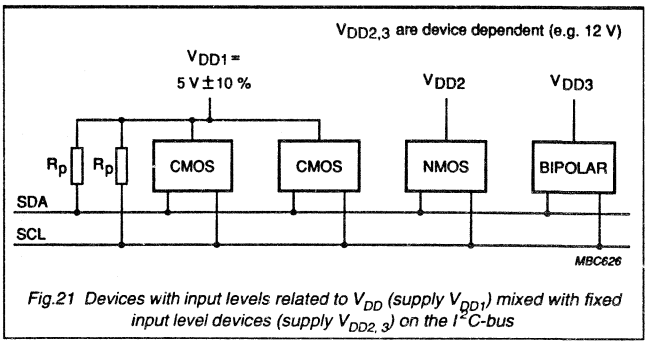


Fig.21 Devices with input levels related to V_{DD} (supply V_{DD1}) mixed with fixed input level devices (supply $V_{DD2, 3}$) on the I²C-bus

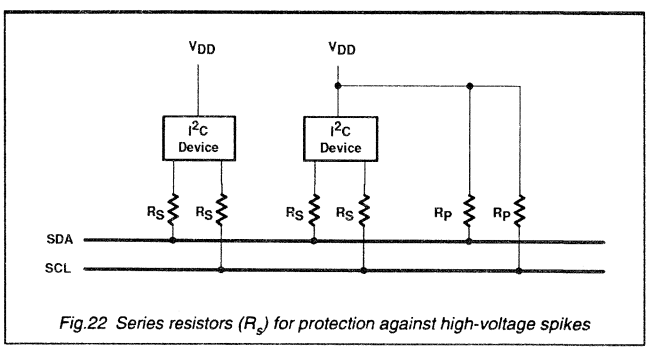


Fig.22 Series resistors (R_s) for protection against high-voltage spikes

I²C -bus specification (including fast-mode)

The supply voltage limits the minimum value of resistor R_p due to the specified minimum sink current of 3 mA at V_{OLmax} = 0.4 V for the output stages. V_{DD} as a function of $R_{p\ min}$ is shown in Fig.23. The desired noise margin of $0.1V_{DD}$ for the LOW level limits the maximum value of R_S. $R_{S\ max}$ as a function of R_p is shown in Fig.24.

The bus capacitance is the total capacitance of wire, connections and pins. This capacitance limits the maximum value of R_p due to the specified rise time. Fig.25 shows $R_{p\ max}$ as a function of bus capacitance.

The maximum HIGH level input current of each input/output connection has a specified maximum value of 10 µA. Due to the desired noise margin of $0.2V_{DD}$ for the HIGH level, this input current limits the maximum value of R_p. This limit depends on V_{DD}. The total HIGH level input current is shown as a function of R_p max in Fig.26.

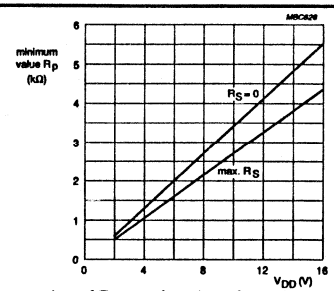


Fig.23 Minimum value of R_p as a function of supply voltage with the value of R_s as a parameter

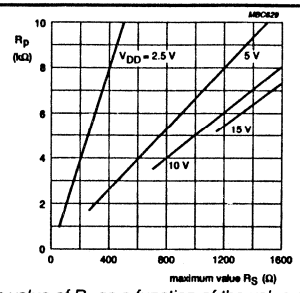


Fig.24 Maximum value of R_s as a function of the value of R_p with supply voltage as a parameter

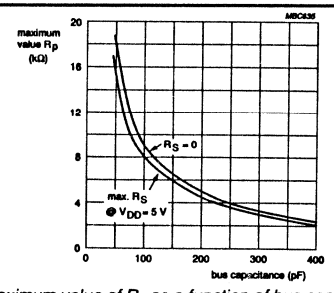


Fig.25 Maximum value of R_p as a function of bus capacitance for a standard-mode I²C-bus

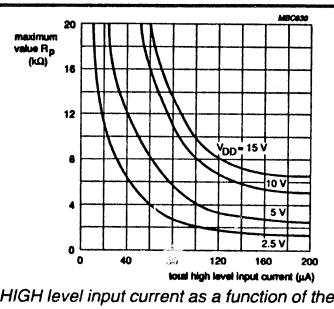


Fig.26 Total HIGH level input current as a function of the maximum value of R_p with supply voltage as a parameter

I²C -bus specification (including fast-mode)

10.0 EXTENSIONS TO THE I²C-BUS SPECIFICATION

The I²C-bus with a data transfer rate of up to 100 kbit/s and 7-bit addressing has now been in existence for more than ten years with an unchanged specification. The concept is accepted world-wide as a de facto standard and hundreds of different types of I²C-bus compatible ICs are available from Philips and other suppliers. The I²C-bus specification is now extended with the following two features:

- A **fast-mode** which allows a fourfold increase of the bit rate to 0 to 400 kbit/s
- **10-bit addressing** which allows the use of up to 1024 additional addresses.

There are two reasons for these extensions to the I²C-bus specification:

- New applications will need to transfer a larger amount of serial data and will therefore demand a higher bit rate than 100 kbit/s. Improved IC manufacturing technology now allows a fourfold speed increase without increasing the manufacturing cost of the interface circuitry
- Most of the 112 addresses available with the 7-bit addressing scheme have been issued more than once. To prevent problems with the allocation of slave addresses for new devices, it is desirable to have more address combinations. About a tenfold increase of the number of available addresses is obtained with the new 10-bit addressing.

All new devices with an I²C-bus interface are provided with the fast-mode. Preferably, they should be able to receive and/or transmit at 400 kbit/s. The minimum requirement is that they can synchronize with a 400 kbit/s transfer; they can then prolong the LOW period of the SCL signal to slow down the transfer. Fast-mode devices must be downward-compatible which means that they must still be able to communicate with 0 to 100 kbit/s devices in a 0 to 100 kbit/s I²C-bus system.

Obviously, devices with 0 to 100 kbit/s I²C-bus interface cannot be incorporated in a fast-mode I²C-bus system because, since they cannot follow the higher transfer rate. Unpredictable states of these devices would occur.

Slave devices with a fast-mode I²C-bus interface can have a 7-bit or 10-bit slave address. However, a 7-bit address is preferred because it is the cheapest solution in hardware and it results in the shortest message length. Devices with 7-bit and 10-bit addresses can be mixed in the same I²C-bus system regardless of whether it is a 0 to 100 kbit/s standard-mode system or a 0 to 400 kbit/s fast-mode system. Existing and future masters can generate 7-bit or 10-bit addresses.

11.0 FAST-MODE

In the fast-mode of the I²C-bus, the protocol, format, logic levels and maximum capacitive load for the SDA and SCL lines given in the previous I²C-bus specification remain unchanged. Changes to the previous I²C-bus specification are:

- The maximum bit rate is increased to 400 kbit/s
- Timing of the serial data (SDA) and serial clock (SCL) signals has been adapted. There is no need for compatibility with other bus systems such as CBUS because they cannot operate at the increased bit rate
- The inputs of fast-mode devices must incorporate spike suppression and a Schmitt trigger at the SDA and SCL inputs
- The output buffers of fast-mode devices must incorporate slope control of the falling edges of the SDA and SCL signals
- If the power supply to a fast-mode device is switched off, the SDA and SCL I/O pins must be floating so that they don't obstruct the bus lines
- The external pull-up devices connected to the bus lines must be adapted to accommodate the shorter maximum permissible rise time for the fast-mode I²C-bus. For bus loads up to 200 pF, the pull-up device for each bus line can be a resistor; for bus loads between 200 pF and 400 pF, the pull-up device can be a current source (3 mA max.) or a switched resistor circuit as shown in Fig.34.

12.0 10-BIT ADDRESSING

The 10-bit addressing does not change the format in the I²C-bus specification. Using 10 bits for addressing exploits the reserved combination 1111XXX for the first 7 bits of the first byte following a START (S) or repeated START (Sr) condition as explained in Section 8.1. The 10-bit addressing does not affect the existing 7-bit addressing. Devices with 7-bit and 10-bit addresses can be connected to the same I²C-bus, and both 7-bit and 10-bit addressing can be used in a standard-mode system (up to 100 kbit/s) or a fast-mode system (up to 400 kbit/s) system.

Although there are eight possible combinations of the reserved address bits 1111XXX, only the four combinations 11110XX are used for 10-bit addressing. The remaining four combinations 11111XX are reserved for future I²C-bus enhancements.

I²C -bus specification (including fast-mode)

12.1 Definition of bits in the first two bytes

The 10-bit slave address is formed from the first two bytes following a START condition (S) or a repeated START condition (Sr).

The first 7 bits of the first byte are the combination 11110XX of which the last two bits (XX) are the two most-significant bits (MSBs) of the 10-bit address; the eighth bit of the first byte is the R/$\overline{W}$ bit that determines the direction of the message. A 'zero' in the least significant position of the first byte means that the master will write information to a selected slave. A 'one' in this position means that the master will read information from the slave.

If R/$\overline{W}$ is 'zero', then the second byte contains the remaining 8 bits (XXXXXXXX) of the 10-bit address. If R/$\overline{W}$ is 'one', then the next byte contains data transmitted from slave to master.

Fig.27 A master-transmitter addresses a slave-receiver with a 10-bit address

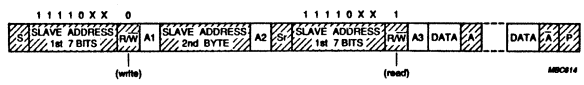


Fig.28 A master-receiver addresses a slave-transmitter with a 10-bit address

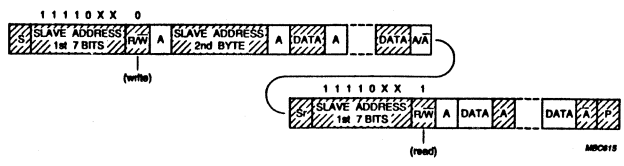


Fig.29 Combined format. A master addresses a slave with a 10-bit address, then transmits data to this slave and reads data from this slave

12.2 Formats with 10-bit addresses

Various combinations of read/write formats are possible within a transfer that includes 10-bit addressing. Possible data transfer formats are:

- **Master-transmitter transmits to slave-receiver with a 10-bit slave address. The transfer direction is not changed (Fig.27).** When a 10-bit address follows a START condition, each slave compares the first 7 bits of the first byte of the slave address (11110XX) with its own address and tests if the eighth bit (R/$\overline{W}$ direction bit) is 0. It is possible that more than one device will find a match and generate an acknowledge (A1). All slaves that found a match will compare the 8 bits of the second byte of the slave address (XXXXXXXX) with their own addresses, but only one slave will find a match and generate an acknowledge (A2). The matching slave will remain addressed by the master until it receives a STOP condition (P) or a repeated START condition (Sr) followed by a different slave address.
- **Master-receiver reads slave-transmitter with a 10-bit slave address. The transfer direction is changed after the second R/$\overline{W}$ bit (Fig.28).** Up to and including acknowledge bit A2, the procedure is the same as that described above for a master-transmitter

I²C -bus specification (including fast-mode)

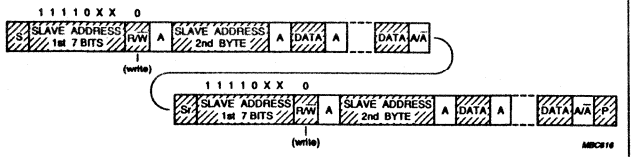


Fig.30 Combined format. A master transmits data to two slaves, both with 10-bit addresses

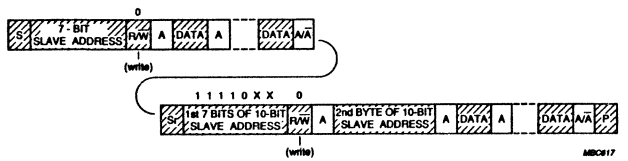


Fig.31 Combined format. A master transmits data to two slaves, one with a 7-bit address, and one with a 10-bit address

addressing a slave-receiver. After the repeated START condition (Sr), a matching slave remembers that it was addressed before. This slave then checks if the first 7 bits of the first byte of the slave address following Sr are the same as before after the START condition (S), and tests if the eighth (R/$\overline{W}$) bit is 1. If there is a match, the slave considers that it has been addressed as a transmitter and generates acknowledge A3. The slave-transmitter remains addressed until it receives a STOP condition (P) or until it receives another repeated START condition (Sr) followed by a different slave address. After Sr, all the other slave devices will also compare the first 7 bits of the first byte of the slave address (11110XX) with their own addresses and test the eighth (R/$\overline{W}$) bit. However, none of them will be addressed because R/$\overline{W}$ = 1 (for 10-bit devices), or the 11110XX slave address (for 7-bit devices) does not match)

- **Combined format. A master transmits data to a slave and then reads data from the same slave (Fig.29).** The same master occupies the bus all the time. The transfer direction is changed after the second R/$\overline{W}$ bit
- **Combined format. A master transmits data to one slave and then transmits data to another slave (Fig.30).** The master occupies the bus all the time
- **Combined format. 10-bit and 7-bit addressing combined in one serial transfer (Fig.31).** After each START condition (S), or each repeated START condition (Sr), a 10-bit or 7-bit slave address can be transmitted. Figure 30 shows how a master-transmits data to a slave with a 7-bit address and then transmits data to a slave with a 10-bit address. The same master occupies the bus all the time.

NOTES:

1) Combined formats can be used, for example, to control a serial memory. During the first data byte, the internal memory location has to be written. After the START condition and slave address is repeated, data can be transferred.
2) All decisions on auto-increment or decrement of previously accessed memory locations etc. are taken by the designer of the device.
3) Each byte is followed by an acknowledgement bit as indicated by the A or $\overline{A}$ blocks in the sequence.
4) I²C-bus compatible devices must reset their bus logic on receipt of a START or repeated START condition such that they all anticipate the sending of a slave address.

13.0 GENERAL CALL ADDRESS AND START BYTE

The 10-bit addressing procedure for the I²C-bus is such that the first two bytes after the START condition (S) usually determine which slave will be selected by the master. The exception is the 'general call' address 00000000 (H'00'). Slave devices with 10-bit addressing will react to a 'general call' in the same way as slave devices with 7-bit addressing (see Section 8.1.1).

Hardware masters can transmit their 10-bit address after a

'general call'. In this case, the 'general call' address byte is followed by two successive bytes containing the 10-bit address of the master-transmitter. The format is as shown in Fig. 15 where the first DATA byte contains the eight least-significant bits of the master address.

The START byte 00000001 (H'01') can precede the 10-bit addressing in the same way as for 7-bit addressing (see Section 8.1.2).

14.0 APPLICATION INFORMATION FOR FAST-MODE I²C-BUS DEVICES

14.1 Output stage with slope control

The electrical specifications for the I/Os of I²C-bus devices and the characteristics of the bus lines connected to them are given in Tables 3 and 4 in Section 15.

Figures 32 and 33 show examples of output stages with slope control in CMOS and bipolar technology. The slope of the falling edge is defined by a Miller capacitor (C1) and a resistor (R1). The typical values for C1 and R1 are indicated on the diagrams. The wide tolerance for output fall time t_{OF} given in Table 3 means that the design is not critical. The fall time is only slightly influenced by the external bus load (C_b) and external pull-up resistor (R_p). However, the rise time (t_R) specified in Table 4 is mainly determined by the bus load capacitance and the value of the pull-up resistor.

14.2 Switched pull-up circuit

The supply voltage (V_{DD}) and the maximum output LOW level determine the minimum value of pull-up resistor R_p (see Section 9.1). For example, with a supply voltage of V_{DD} = 5 V ± 10% and $V_{OL\ max.}$ = 0.4 V at 3 mA, $R_{p\ min.}$ = (5.5 – 0.4)/0.003 = 1.7 kΩ. As shown in Fig.35, this value of R_p limits the maximum bus capacitance to about 200 pF to meet the maximum t_R requirement of 300 ns. If the bus has a higher capacitance than this, a switched pull-up circuit as shown in Fig.34 can be used.

The switched pull-up circuit in Fig.34 is for a supply voltage of V_{DD} = 5 V ± 10 % and a maximum capacitive load of 400 pF. Since it is controlled by the bus levels, it needs no additional control signals. During the rising/falling edges, the bilateral switch in the HCT4066 switches pull-up resistor R_p2 on/off at bus levels between 0.8 V and 2.0 V. Combined resistors R_p1 and R_p2 can pull-up the bus line within the maximum specified rise time (t_R) of 300 ns. The maximum sink current for the driving I²C-bus device will not exceed 6 mA at V_{OL2} = 0.6 V, and 3 mA at V_{OL1} = 0.4 V.

Series resistors R_s are optional. They protect the I/O stages of the I²C-bus devices from high-voltage spikes on the bus lines, and minimize crosstalk and undershoot of the bus line signals. The maximum value of R_s is determined by the maximum permitted voltage drop across this resistor when the bus line is switched to the LOW level in order to switch off R_p2.

14.3 Wiring pattern of the bus lines

In general, the wiring must be so chosen that crosstalk and interference to/from the bus lines is minimized. The bus lines are most susceptible to crosstalk and interference at the HIGH level because of the relatively high impedance of the pull-up devices.

If the length of the bus lines on a PCB or ribbon cable exceeds 10 cm and includes the V_{DD} and V_{SS} lines, the wiring pattern must be:

SDA _____
V_{DD} _____
V_{SS} _____
SCL _____

If only the V_{SS} line is included, the wiring pattern must be:

SDA _____
V_{SS} _____
SCL _____

I²C -bus specification (including fast-mode)

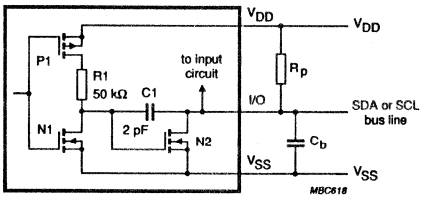


Fig.32 Slope-controlled output stage in CMOS technology

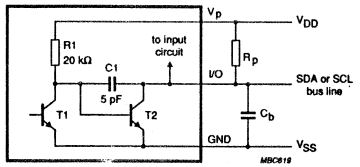


Fig.33 Slope-controlled output stage in bipolar technology

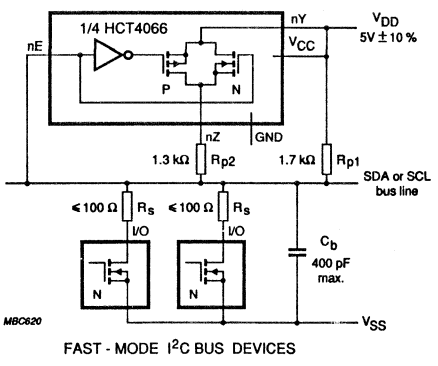


Fig.34 Switched pull-up circuit

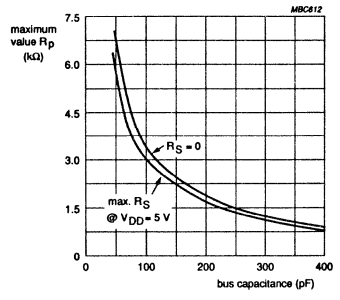


Fig.35 Maximum value of R_p as a function of bus capacitance for meeting the $t_{R\,max.}$ requirement for a fast-mode I²C-bus

These wiring patterns also result in identical capacitive loads for the SDA and SCL lines. The V_{SS} and V_{DD} lines can be omitted if a PCB with a V_{SS} and/or V_{DD} layer is used.

If the bus lines are twisted-pairs, each bus line must be twisted with a V_{SS} return. Alternatively, the SCL line can be twisted with a V_{SS} return, and the SDA line twisted with a V_{DD} return. In the latter case, capacitors must be used to decouple the V_{DD} line to the V_{SS} line at both ends of the twisted pairs.

If the bus lines are shielded (shield connected to V_{SS}), interference will be minimized. The shielded cable must have low capacitive coupling between the SDA and SCL lines to minimize crosstalk.

14.4 Maximum and minimum values of resistors R_p and R_s

The maximum and minimum values for resistors R_p and R_s connected to a fast-mode I²C-bus can be determined from Fig.23, 24 and 26 in Section 9.1. Because a fast-mode I²C-bus has faster rise times (t_R) the maximum value of R_p as a function of bus capacitance is less than that shown in Fig.25 The replacement graph for Fig.25 showing the maximum value of R_p as a function of bus capacitance (C_b) for a fast mode I²C-bus is given in Fig.35.

I²C -bus specification (including fast-mode)

15.0 ELECTRICAL SPECIFICATIONS AND TIMING FOR I/O STAGES AND BUS LINES

The I/O levels, I/O current, spike suppression, output slope control and pin capacitance for I²C-bus devices are given in Table 3. The I²C-bus timing is given in Table 4. Figure 36 shows the timing definitions for the I²C-bus.

The noise margin for levels on the bus lines for fast-mode devices are the same as those specified in Section 9.0 for standard-mode I²C-bus devices.

The minimum HIGH and LOW periods of the SCL clock specified in Table 4 determine the maximum bit transfer rates of 100 kbit/s for standard-mode devices and 400 kbit/s for fast mode devices. Standard-mode and fast-mode I²C-bus devices must be able to follow transfers at their own maximum bit rates, either by being able to transmit or receive at that speed or by applying the clock synchronization procedure described in Section 6 which will force the master into a wait state and stretch the LOW period of the SCL signal. Of course, in the latter case the bit transfer rate is reduced.

Table 3 Characteristics of the SDA and SCL I/O stages for I²C-bus devices

Parameter	Symbol	standard-mode devices		fast-mode devices		Unit
		Min.	Max.	Min.	Max.	
LOW level input voltage: fixed input levels V_{DD}-related input levels	V_{IL}	 -0.5 -0.5	 1.5 $0.3V_{DD}$	 -0.5 -0.5	 1.5 $0.3V_{DD}$	V
HIGH level input voltage: fixed input levels V_{DD}-related input levels	V_{IH}	 3.0 $0.7V_{DD}$	 *1) *1)	 3.0 $0.7V_{DD}$	 *1) *1)	V
Hysteresis of Schmitt trigger inputs: fixed input levels V_{DD}-related input levels	V_{hys}	 n/a n/a	 n/a n/a	 0.2 $0.05V_{DD}$	 - -	V
Pulse width of spikes which must be suppressed by the input filter	t_{SP}	n/a	n/a	0	50	ns
LOW level output voltage (open drain or open collector): at 3 mA sink current at 6 mA sink current	 V_{OL1} V_{OL2}	 0 n/a	 0.4 n/a	 0 0	 0.4 0.6	V
Output fall time from $V_{IH\ min.}$ to $V_{IL\ max.}$ with a bus capacitance from 10 pF to 400 pF: with up to 3 mA sink current at V_{OL1} with up to 6 mA sink current at V_{OL2}	t_{OF}	 - n/a	 250[2)] n/a	 $20 + 0.1C_b$[2)] $20 + 0.1C_b$[2)]	 250 250[3)]	ns
Input current each I/O pin with an input voltage between 0.4 V and $0.9V_{DD\ max.}$	I_i	-10	10	-10[3)]	10[3)]	µA
Capacitance for each I/O pin	C_i	-	10	-	10	pF

n/a = not applicable

1) maximum $V_{IH} = V_{DD\ max.} + 0.5$ V

2) C_b = capacitance of one bus line in pF. Note that the maximum t_F for the SDA and SCL bus lines quoted in Table 4 (300 ns) is longer than the specified maximum t_{OF} for the output stages (250 ns). This allows series protection resistors (R_s)to be connected between the SDA/SCL pins and the SDA/SCL bus lines as shown in Fig.34 without exceeding the maximum specified t_F.

3) I/O pins of fast-mode devices must not obstruct the SDA and SCL lines if V_{DD} is switched off.

I²C -bus specification (including fast-mode)

Table 4 Characteristics of the SDA and SCL bus lines for I²C-bus devices

Parameter	Symbol	Standard-mode I²C-bus		Fast-mode I²C-bus		Unit
		Min.	Max.	Min.	Max.	
SCL clock frequency	f_{SCL}	0	100	0	400	kHz
Bus free time between a STOP and START condition	t_{BUF}	4.7	-	1.3	-	µs
Hold time (repeated) START condition. After this period, the first clock pulse is generated	$t_{HD;STA}$	4.0	-	0.6	-	µs
LOW period of the SCL clock	t_{LOW}	4.7	-	1.3	-	µs
HIGH period of the SCL clock	t_{HIGH}	4.0	-	0.6	-	µs
Set-up time for a repeated START condition	$t_{SU;STA}$	4.7	-	0.6	-	µs
Data hold time: for CBUS compatible masters (see NOTE, Section 8.1.3) for I²C-bus devices	$t_{HD;DAT}$	 5.0 0[1]	 - -	 - 0[1]	 - 0.9[2]	 µs µs
Data set-up time	$t_{SU;DAT}$	250	-	100[3]	-	ns
Rise time of both SDA and SCL signals	t_R	-	1000	20 + 0.1C_b[4]	300	ns
Fall time of both SDA and SCL signals	t_F	-	300	20 + 0.1C_b[4]	300	ns
Set-up time for STOP condition	$t_{SU;STO}$	4.0	-	0.6	-	µs
Capacitive load for each bus line	C_b	-	400	-	400	pF

All values referred to $V_{IH\ min.}$ and $V_{IL\ max.}$ levels (see Table 3).

[1] A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the $V_{IH\ min.}$ of the SCL signal) in order to bridge the undefined region of the falling edge of SCL.

[2] The maximum $t_{HD;DAT}$ has only to be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.

[3] A fast-mode I²C-bus device can be used in a standard-mode I²C-bus system, but the requirement $t_{SU;DAT} \geq 250$ ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{R\ max.} + t_{SU;DAT} = 1000 + 250 = 1250$ ns (according to the standard-mode I²C-bus specification) before the SCL line is released.

[4] C_b = total capacitance of one bus line in pF.

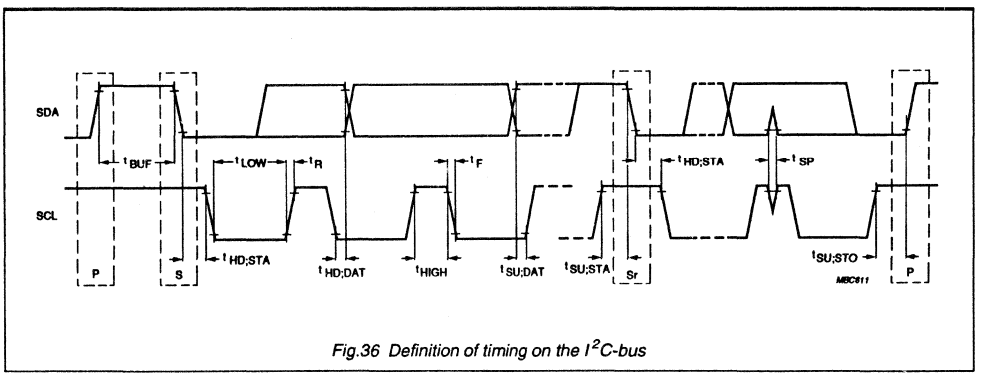


Fig.36 Definition of timing on the I²C-bus

I²C peripheral selection guide

GENERAL PURPOSE ICs

LCD Drivers

PCF8566	96-segment LCD driver 1:1 – 1:4 Mux
PCF8568	LCD row driver for dot matrix displays
PCF8569	Column driver for dot matrix displays
PCF8576	160-segment LCD driver 1:1 – 1:4 Mux
PCF8577C	64-segment LCD driver 1:1 – 1:2 Mux
PCF8578/79	Row/column LCD dot-matrix driver; 1:8 – 1:32 Mux

I/O Expanders

PCF8574/A	8-bit remote I/O port (I²C-bus to parallel converter)
PCD8584	8-bit parallel to I²C converter
SAA1064	4-digit LED driver
SAA1300	5-bit high-current driver

Data Converters

PCF8591	4-channel, 8-bit Mux ADC + one DAC
TDA8442	Quad 6-bit DAC
TDA8444	Octal 6-bit DAC

Memory

PCF8570/C	256-byte static RAM
PCF8571	128-byte static RAM
PCF8581	128-byte EEPROM
PC.8582	256-byte EEPROM
PCF8583	256-byte RAM/clock/calendar
PCF8594	512-byte EEPROM

Clocks/Calendars

PCF8573	Clock/calendar
PCF8583	Clock/calendar/ 256-byte RAM

68000-Based CMOS Microcontrollers

68070	68000 CPU/MMU/UART/ DMA/timer
93CXXX	UST/I²C/34k ROM/ 512 RAM

80C51-Based CMOS Microcontrollers*

8XCL410	4k ROM/128 RAM, low power
8XC528	32k ROM/512 RAM, T2, WD
8XC552	256-byte RAM/8k ROM/ ADC/UART/PWM
8XC652	256-byte RAM/8k ROM, UART
8XC654	256-byte RAM/16kROM, UART
8XC751	64-byte RAM/2k ROM
8XC752	64-byte RAM/2k ROM, ADC/PWM

8048 Instruction-Set Based CMOS Microcontrollers

PCF84C00	256-byte RAM/bond-out version for prototype development
PCF84C21	64-byte RAM/2k ROM
PCF84C41	128-byte RAM/2k ROM
PCF84C81	256-byte RAM/8k ROM
PCF84C85	256-byte RAM/8k ROM/ Extended I/O
PCF84C430	128-byte RAM/4k ROM/ 96-segment LCD driver

MULTIMEDIA ICs

Video/Radio/Audio

SAA5243	Enhanced Computer Controlled Teletext (ECCT) decoder
SAA5245	Enhanced Computer Controlled Teletext (USECCT) decoder
SAA7191	S-VHS digital multistandard decoder "square pixel"
SAA7192	Digital color space converter
SAA7199	Digital encoder
SAA9041	Digital video teletext (DVTB) processor
SAA9051	7-Bit digital video decoder
SAB3035/36/37	Digital tuning circuits for computer-controlled TV
SAF1135	Dataline 16 decoder for VCR
TDA1551Q	2 × 22W Audio Power Amp
TDA4670	Picture signal improvement circuit
TDA4680	Video processor
TDA6360	5 Band Equalizer
TDA8415/17	Stereo/dual sound processor
TDA8421	Audio processor with a loudspeaker channel and a headphone channel
TDA8425	Audio processor with a loudspeaker channel only
TDA8433	Deflection processor
TDA8440	Video/audio switch
TDA8442	Interface for color decoders
TDA8443/A	YUV/RGB matrix switch
TDA8461	PAL/NTSC color decoder and RGB processor
TDA8466	PAL/NTSC color decoder and RGB processor
TDA9150	Deflection processor
TEA6100	FM/IF and digital tuning IC for computer-controlled radio
TEA6300	Sound fader control and preamplifier/source selector for car radio
TEA6310T	Sound fader control with tone and volume control for car radio
TSA5511/12/14	PLL frequency synthesizer for TV
TSA6057	PLL frequency synthesizer for radio

Telecom

NE5750/51	Audio processor pair
PCD3311/12	Tone generator (DTMF/modem/musical)
PCD3341	Advanced 10 to 110-number repertory dialer with LCD control
PCD3343	Microcontroller with 224-byte RAM/3k ROM
PCD3348	Microcontroller with 256-byte RAM/8k ROM
UMA1000T	Data processor for mobile telephones
UMA1014T	1GHz frequency synthesizer for mobile telephones
UMF1009	Frequency synthesizer

Also available with extended temperature ranges.

Section 2
Data Sheets

INDEX

GENERAL DESCRIPTION

The PCD3311C and PCD3312C are single-chip silicon gate CMOS integrated circuits. They are intended to provide dual-tone multi-frequency (DTMF) combinations required for tone dialling systems in telephone sets which contain a microcontroller for the control functions.

The various audio output frequencies are generated from an on-chip 3,58 MHz quartz crystal-controlled oscillator.

The devices can interface directly to all standard microcontrollers by accepting a binary-coded parallel input or serial data input (I²C-bus).

With their on-chip voltage reference the PCD3311C and PCD3312C provide constant output amplitudes which are independent of the operating supply voltage and ambient temperature.

An on-chip filtering system assures a very low total harmonic distortion in accordance with the CEPT T/CS46-03 (= former CS203) recommendations.

In addition to the standard DTMF frequencies the devices provide 12 MODEM frequencies (300 to 1200 bits per second) used in simplex MODEM applications and two octaves of musical scale in steps of semitones.

Features

- Stabilized output voltage level
- Low output distortion with on-chip filtering (CEPT CS 203 compatible)
- Latched inputs for data bus applications
- I²C-bus compatible
- Mode select input (selection of parallel or serial data input)
- MODEM and melody tone generators

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Operating supply voltage	V_{DD}	2,5	–	6,0	V
Operating supply current	I_{DD}	–	–	0,9	mA
Static standby current	I_{DDO}	–	–	3	μA
DTMF output voltage level (RMS values)					
HIGH group	$V_{HG(rms)}$	158	192	205	mV
LOW group	$V_{LG(rms)}$	125	150	160	mV
Pre-emphasis of group	ΔV_G	1,85	2,10	2,35	dB
Total harmonic distortion	THD	–	−25	–	dB
Operating ambient temperature range	T_{amb}	−25	–	+70	°C

PACKAGE OUTLINES

PCD3311CP: 14-lead DIL; plastic (SOT27).
PCD3311CT: 16-lead mini-pack; plastic (SO16L; SOT162A).
PCD3312CP: 8-lead DIL; plastic (SOT97).
PCD3312CT: 8-lead mini-pack; plastic (SO8L; SOT176C).

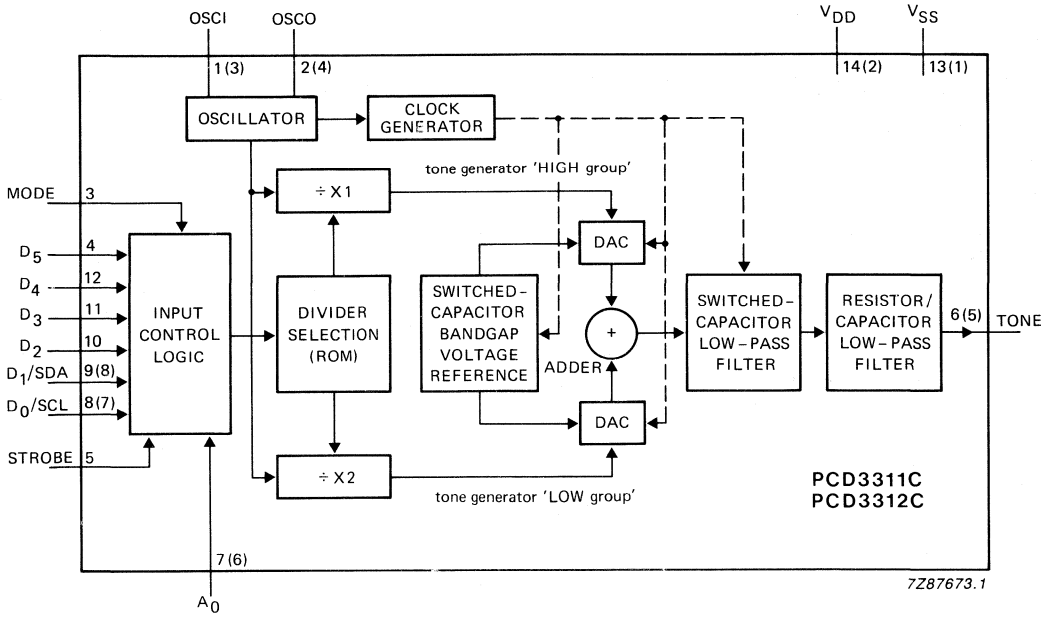


Fig. 1 Block diagram; the pin numbers in parenthesis refer to the PCD3312C.

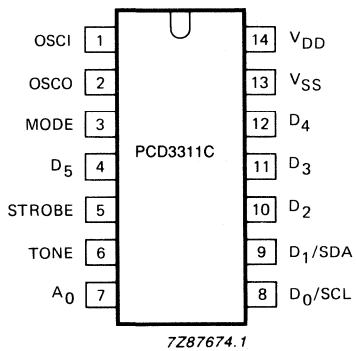


Fig. 2 Pinning diagram for the PCD3311CP.

PINNING

1	OSCI	oscillator input
2	OSCO	oscillator output
3	MODE	mode select input; used for the selection between serial mode (MODE = LOW) and parallel mode (MODE = HIGH)
4	D_5	parallel data input*
5	STROBE	strobe input; used for the loading of data in the parallel mode
6	TONE	frequency output for single or dual tones
7	A_0	slave address input in the serial mode; must be connected to V_{DD} or V_{SS}
8	D_0/SCL	parallel data input* or serial clock line (I^2C-bus)
9	D_1/SDA	parallel data input* or serial data line (I^2C-bus)
10	D_2	parallel data inputs*
11	D_3	
12	D_4	
13	V_{SS}	negative supply
14	V_{DD}	positive supply

* MODE = HIGH.

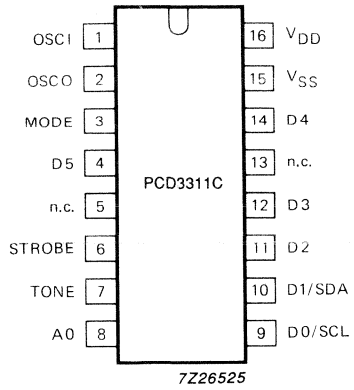


Fig. 3 Pinning diagram for the PCD3311CT.

PINNING

1	OSCI	oscillator input
2	OSCO	oscillator output
3	MODE	mode select input; used for the selection between serial mode (MODE = LOW) and parallel mode (MODE = HIGH)
4	D_5	parallel data input*
6	STROBE	strobe input; used for the loading of data in the parallel mode
7	TONE	frequency output for single or dual tones
8	A_0	slave address input in the serial mode; must be connected to V_{DD} or V_{SS}
9	D_0/SCL	parallel data input* or serial clock line (I²C-bus)
10	D_1/SDA	parallel data input* or serial data line (I²C-bus)
11	D_2	parallel data inputs*
12	D_3	
14	D_4	
15	V_{SS}	negative supply
16	V_{DD}	positive supply
5; 13	n.c.	not connected

* MODE = HIGH.

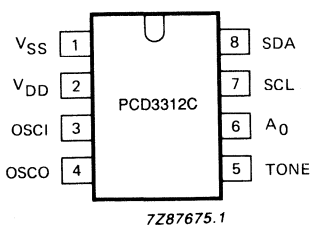


Fig. 4 Pinning diagram for the PCD3312C.

PINNING

1	V_{SS}	negative supply
2	V_{DD}	positive supply
3	OSCI	oscillator input
4	OSCO	oscillator output
5	TONE	frequency output for single or dual tones
6	A_0	slave address input in the serial mode; must be connected to V_{DD} or V_{SS}
7	SCL	serial clock line (I²C bus)
8	SDA	serial data line (I²C bus)

FUNCTIONAL DESCRIPTION

Clock/oscillator (OSCI and OSCO)

The timebase for the PCD3311C and PCD3312C is a crystal-controlled oscillator with a 3,58 MHz quartz crystal connected between OSCI and OSCO. Alternatively, the OSCI input can be driven from an external clock.

Mode select (MODE)

This input selects the data input mode. When connected to V_{DD}, data can be received in the parallel mode (only for the PCD3311C), or, when connected to V_{SS} or left open, data can be received via the serial I²C-bus (for both PCD3311C and PCD3312C).

Parallel mode can only be obtained for the PCD3311 by setting MODE input HIGH.

Data inputs (D_0, D_1, D_2, D_3, D_4 and D_5)

Inputs D_0 and D_1 have no internal pull-down or pull-up resistors and must not be left open in any application. Inputs D_2 to D_5 have internal pull-down. D_5 and D_4 are used to select between DTMF dual, DTMF single, MODEM and melody tones (see Table 1). D_3 to D_0 select the combination of the tones for DTMF or single-tone itself.

Table 1 D_5 and D_4 in accordance with the selected application

D_5	D_4	application
0	0	DTMF single tones; standby; melody tones
0	1	DTMF dual tones (all 16 combinations)
1	0	MODEM tones; standby; melody tones
1	1	melody tones

1 = H = HIGH voltage level
0 = L = LOW voltage level

Note: Tables 2, 3, 4 and 5 show all input codes and their corresponding output frequencies.

Strobe input (STROBE, only for the PCD3311C)

This input (with internal pull-down) allows the loading of parallel data into D_0 to D_5 when MODE is HIGH.

The data inputs must be stable preceeding the positive-going edge of the strobe pulse (active HIGH). Input data are loaded at the negative-going edge of the strobe pulse and then the corresponding tone (or standby mode) is provided at the TONE output. The output remains unchanged until the negative-going edge of the next STROBE pulse (for new data) is received.

Serial mode can only be obtained for the PCD3311C by setting MODE input LOW.

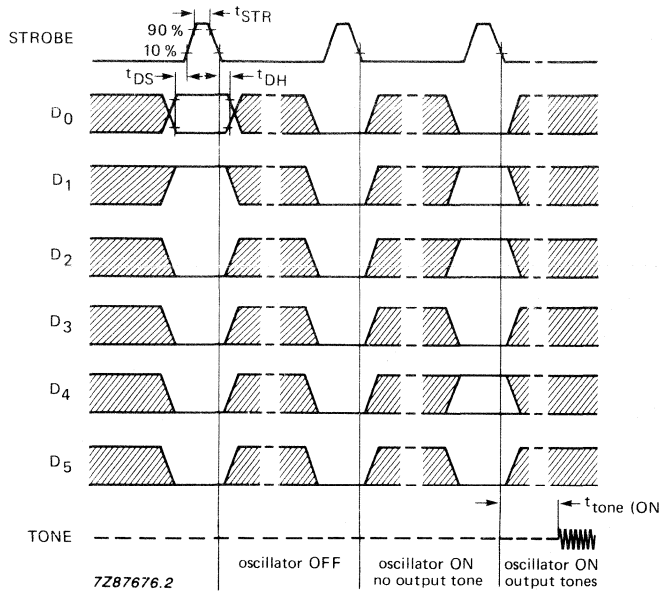


Fig. 5 Timing diagram showing control possibilities of the oscillator and the TONE output (e.g. 770 Hz + 1477 Hz) in the parallel mode (MODE = HIGH).

Serial clock and data inputs (SCL and SDA)

SCL and SDA are combined with D_0 and D_1 respectively. For the PCD3311C the selection of SCL and SDA is controlled by the MODE input. SCL and SDA are serial clock and data lines according to the I²C-bus specification (see "CHARACTERISTICS OF THE I²C-BUS"). Both inputs must be pulled-up externally to V_{DD}.

Address input (A_0)

A_0 is the slave address input and it identifies the device when up to two PCD3311C or PCD3312C devices are connected to the same I²C bus. In any case A_0 must be connected to V_{DD} or V_{SS}.

I²C bus data configuration (see Fig. 6)

The PCD3311C and PCD3312C are always slave receivers in the I²C-bus configuration (R/$\overline{W}$ bit = 0).

The slave address consists of 7 bits in the serial mode for the PCD3311C as well as for the PCD3312C, where the least significant bit is selectable by hardware on input A_0 and the other more significant bits are internally fixed. In the serial mode the same input codes are used as in the parallel mode (see Tables 2, 3, 4, and 5). D_6 and D_7 are don't care (X) bits.

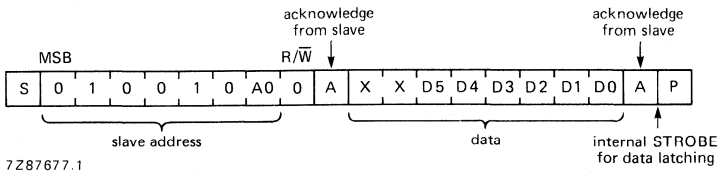


Fig. 6 I²C-bus data format.

Tone output (TONE)

The single and the dual tones which are provided at the TONE output are filtered by an on-chip switched-capacitor filter, followed by an active RC low-pass filter. Therefore, the total harmonic distortion of the DTMF tones fulfils the CEPT CS46-03 recommendations. An on-chip reference voltage provides output-tone levels independent of the supply voltage. Table 3 shows the frequency tolerance of the output tones for DTMF signalling; Tables 4 and 5 for the modem and melody tones.

Power-on reset

In order to avoid undefined states of the devices when the power is switched ON, an internal reset circuit sets them to the standby mode (oscillator OFF).

Table 2 Input data for control (no output tone; TONE in 3-state)

D_5	D_4	D_3	D_2	D_1	D_0	HEX	oscillator
X	0	0	0	0	0	00/20	ON
X	0	0	0	0	1	01/21	OFF
X	0	0	0	1	0	02/22	OFF
X	0	0	0	1	1	03/23	OFF

1 = H = HIGH voltage level
0 = L = LOW voltage level
X= don't care

Table 3 Input data for DTMF

D_5	D_4	D_3	D_2	D_1	D_0	HEX	symbol	standard frequency Hz	tone output freq. Hz**	frequency deviation %	frequency deviation Hz
0	0	1	0	0	0	08		697	697,90	+ 0,13	+ 0,90
0	0	1	0	0	1	09		770	770,46	+ 0,06	+ 0,46
0	0	1	0	1	0	0A		852	850,45	−0,18	−1,55
0	0	1	0	1	1	0B		941	943,23	+ 0,24	+ 2,23
0	0	1	1	0	0	0C		1209	1206,45	−0,21	−2,55
0	0	1	1	0	1	0D		1336	1341,66	+ 0,42	+ 5,66
0	0	1	1	1	0	0E		1477	1482,21	+ 0,35	+ 5,21
0	0	1	1	1	1	0F		1633	1638,24	+ 0,32	+ 5,24
0	1	0	0	0	0	10	0	941+1336			
0	1	0	0	0	1	11	1	697+1209			
0	1	0	0	1	0	12	2	697+1336			
0	1	0	0	1	1	13	3	697+1477			
0	1	0	1	0	0	14	4	770+1209			
0	1	0	1	0	1	15	5	770+1336			
0	1	0	1	1	0	16	6	770+1477			
0	1	0	1	1	1	17	7	852+1209			
0	1	1	0	0	0	18	8	852+1336			
0	1	1	0	0	1	19	9	852+1477			
0	1	1	0	1	0	1A	A	697+1633			
0	1	1	0	1	1	1B	B	770+1633			
0	1	1	1	0	0	1C	C	852+1633			
0	1	1	1	0	1	1D	D	941+1633			
0	1	1	1	1	0	1E	*	941+1209			
0	1	1	1	1	1	1F	#	941+1477			

Table 4 Input data for MODEM frequencies

D_5	D_4	D_3	D_2	D_1	D_0	HEX	standard frequency Hz	tone output freq. Hz**	frequency deviation %	frequency deviation Hz	remarks
1	0	0	1	0	0	24	1300	1296,94	−0,24	−3,06	V.23
1	0	0	1	0	1	25	2100	2103,14	+ 0,15	+ 3,14	
1	0	0	1	1	0	26	1200	1197,17	−0,24	−2,83	Bell 202
1	0	0	1	1	1	27	2200	2192,01	−0,36	−7,99	
1	0	1	0	0	0	28	980	978,82	−0,12	−1,18	V.21
1	0	1	0	0	1	29	1180	1179,03	−0,08	−0,97	
1	0	1	0	1	0	2A	1070	1073,33	+ 0,31	+ 3,33	Bell 103
1	0	1	0	1	1	2B	1270	1265,30	−0,37	−4,70	
1	0	1	1	0	0	2C	1650	1655,66	+ 0,34	+ 5,66	V.21
1	0	1	1	0	1	2D	1850	1852,77	+ 0,15	+ 2,77	
1	0	1	1	1	0	2E	2025	2021,20	−0,19	−3,80	Bell 103
1	0	1	1	1	1	2F	2225	2223,32	−0,08	−1,68	

** Tone output frequency when using a 3,579 545 MHz crystal.

1 = H = HIGH voltage level
0 = L = LOW voltage level

Table 5 Input data for melody tones

D_5	D_4	D_3	D_2	D_1	D_0	HEX	note	standard frequency Hz*	tone output frequency Hz**
1	1	0	0	0	0	30	D#5	622,3	622,5
1	1	0	0	0	1	31	E5	659,3	659,5
1	1	0	0	1	0	32	F5	698,5	697,9
1	1	0	0	1	1	33	F#5	740,0	741,1
1	1	0	1	0	0	34	G5	784,0	782,1
1	1	0	1	0	1	35	G#5	830,6	832,3
1	1	0	1	1	0	36	A5	880,0	879,3
1	1	0	1	1	1	37	A#5	932,3	931,9
1	1	1	0	0	0	38	B5	987,8	985,0
1	1	1	0	0	1	39	C6	1046,5	1044,5
1	1	1	0	1	0	3A	C#6	1108,7	1111,7
1	0	1	0	0	1	29	D6	1174,7	1179,0
1	1	1	0	1	1	3B	D#6	1244,5	1245,1
1	1	1	1	0	0	3C	E6	1318,5	1318,9
1	1	1	1	0	1	3D	F6	1396,9	1402,1
0	0	1	1	1	0	0E	F#6	1480,0	1482,2
1	1	1	1	1	0	3E	G6	1568,0	1572,0
1	0	1	1	0	0	2C	G#6	1661,2	1655,7
1	1	1	1	1	1	3F	A6	1760,0	1768,5
0	0	0	1	0	0	04	A#6	1864,7	1875,1
0	0	0	1	0	1	05	B6	1975,5	1970,0
1	0	0	1	0	1	25	C7	2093,0	2103,1
1	0	1	1	1	1	2F	C#7	2217,5	2223,3
0	0	0	1	1	0	06	D7	2349,3	2358,1
0	0	0	1	1	1	07	D#7	2489,0	2470,4

* Standard scale based on A4 = 440 Hz.

** Tone output frequency when using a 3,579 545 MHz crystal.

1 = H = HIGH voltage level

0 = L = LOW voltage level

CHARACTERISTICS OF THE I²C-BUS

The I²C-bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

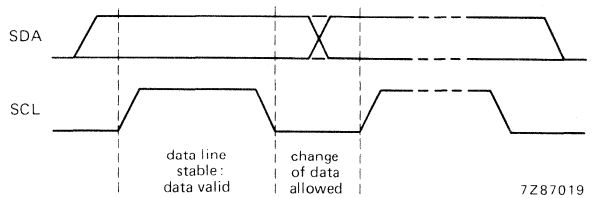


Fig. 7 Bit transfer.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

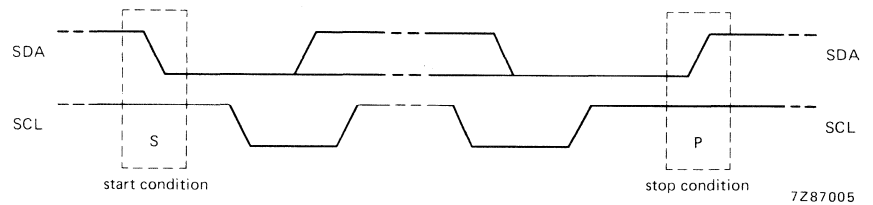


Fig. 8 Definition of start and stop conditions.

System configuration

A device generating a message is a "transmitter", a device receiving a message is the "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

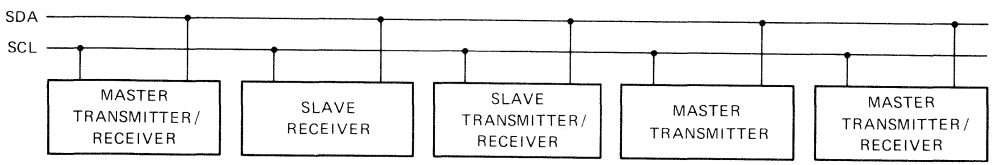


Fig. 9 System configuration.

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set-up and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

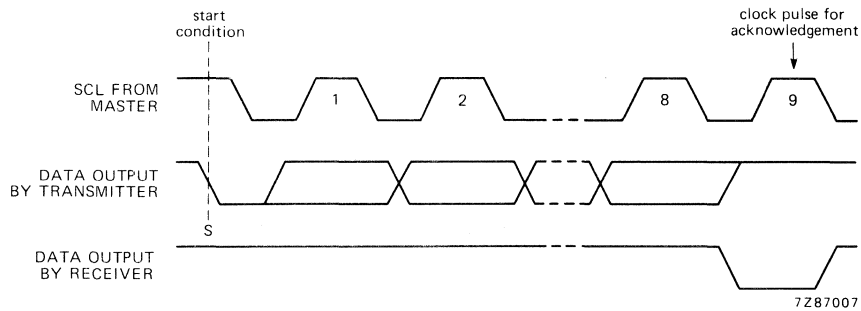


Fig. 10 Acknowledgement on the I²C-bus.

Timing specifications

Within the I²C-bus specifications a high-speed mode and a low-speed mode are defined. The ICs operate in both modes and the timing requirements are as follows:

High-speed mode

Masters generate a bus clock with a maximum frequency of 100 kHz. Detailed timing is shown in Fig. 11.

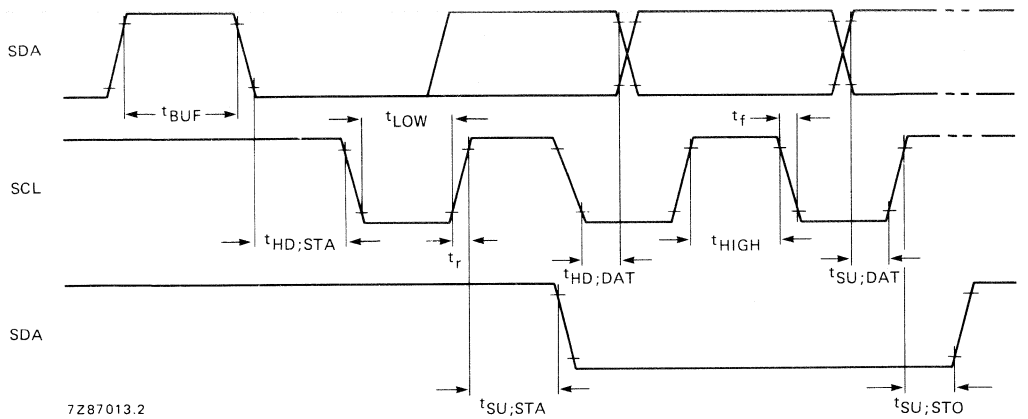


Fig. 11 Timing of the high-speed mode.

Where:

t_{BUF}	$t \geqslant t_{LOWmin}$	The minimum time the bus must be free before a new transmission can start
$t_{HD;STA}$	$t \geqslant t_{HIGHmin}$	Start condition hold time
t_{LOWmin}	4,7 μs	Clock LOW period
$t_{HIGHmin}$	4 μs	Clock HIGH period
$t_{SU;STA}$	$t \geqslant t_{LOWmin}$	Start condition set-up time, only valid for repeated start code
$t_{HD;DAT}$	$t \geqslant 0$ μs	Data hold time
$t_{SU;DAT}$	$t \geqslant 250$ ns	Data set-up time
t_r	$t \leqslant 1$ μs	Rise time of both the SDA and SCL line
t_f	$t \leqslant 300$ ns	Fall time of both the SDA and SCL line
$t_{SU;STO}$	$t \geqslant t_{LOWmin}$	Stop condition set-up time

Note

All the timing values refer to V_{IH} and V_{IL} levels with a voltage swing of V_{SS} to V_{DD}.

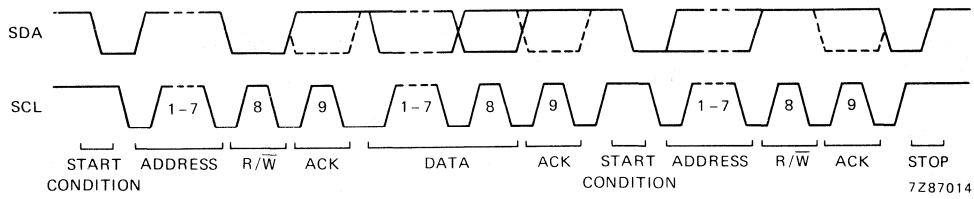


Fig. 12 Complete data transfer in the high-speed mode.

Where:

Clock t_{LOWmin}	4,7 μs
$t_{HIGHmin}$	4 μs

The dashed line is the acknowledgement of the receiver

Mark-to-space ratio	1 : 1 (LOW-to-HIGH)
Max. number of bytes	unrestricted
Premature termination of transfer	allowed by generation of STOP condition
Acknowledge clock bit	must be provided by the master

Low-speed mode

Masters generate a bus clock with a maximum frequency of 2 kHz; a minimum LOW period of 105 μs and a minimum HIGH period of 365 μs. The mark-to-space ratio is 1 : 3 LOW-to-HIGH. Detailed timing is shown in Fig. 13.

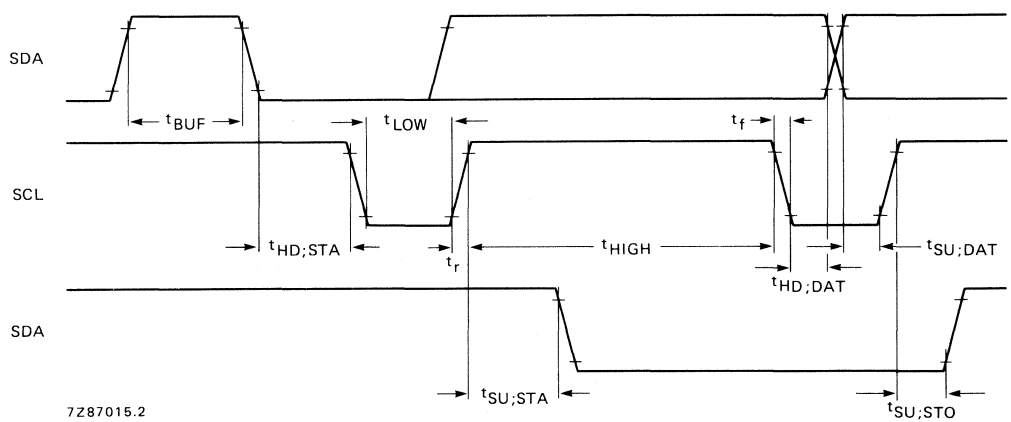


Fig. 13 Timing of the low-speed mode.

Timing specifications (continued)

Where:

t_{BUF}	$t \geqslant 105\ \mu s$ (t_{LOWmin})
$t_{HD;STA}$	$t \geqslant 365\ \mu s$ ($t_{HIGHmin}$)
t_{LOW}	$130\ \mu s \pm 25\ \mu s$
t_{HIGH}	$390\ \mu s \pm 25\ \mu s$
$t_{SU;STA}$	$130\ \mu s \pm 25\ \mu s$ *
$t_{HD;DAT}$	$t \geqslant 0\ \mu s$
$t_{SU;DAT}$	$t \geqslant 250$ ns
t_R	$t \leqslant 1\ \mu s$
t_F	$t \leqslant 300$ ns
$t_{SU;STO}$	$130\ \mu s \pm 25\ \mu s$

Note

All the timing values refer to V_{IH} and V_{IL} levels with a voltage swing of V_{SS} to V_{DD}. For definitions see high-speed mode.

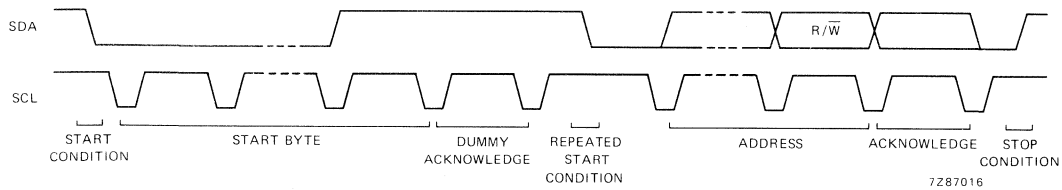


Fig. 14 Complete data transfer in the low-speed mode.

Where:

Clock t_{LOWmin}	$130\ \mu s \pm 25\ \mu s$
$t_{HIGHmin}$	$390\ \mu s \pm 25\ \mu s$
Mark-to-space ratio	1 : 3 (LOW-to-HIGH)
Start byte	0000 0001
Max. number of bytes	6
Premature termination of transfer	not allowed
Acknowledge clock bit	must be provided by master

* Only valid for repeated start code.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage range	V_{DD}	−0,8	+ 8,0	V
Input voltage range (any input)	V_I	−0,8	V_{DD}+0,8	V
DC input current (any input)	$\pm I_I$	–	10	mA
DC output current (any output)	$\pm I_O$	–	10	mA
Supply current	$\pm I_{DD}$; $\pm I_{SS}$	–	50	mA
Power dissipation per output	P_O	–	50	mW
Total power dissipation per package	P_{tot}	–	300	mW
Operating ambient temperature range	T_{amb}	−25	+ 70	°C
Storage temperature range	T_{stg}	−65	+ 150	°C

CHARACTERISTICS

V_{DD} = 2,5 to 6 V; V_{SS} = 0 V; crystal parameters: f_{osc} = 3,579 545 MHz, R_{Smax} = 50 Ω; T_{amb} = −25 to + 70 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Operating supply voltage	V_{DD}	2,5	–	6,0	V
Operating supply current (note 1) oscillator ON; V_{DD} = 3 V					
no output tone	I_{DD}	–	50	100	μA
single output tone	I_{DD}	–	0,5	0,8	mA
dual output tone	I_{DD}	–	0,6	0,9	mA
Static standby current oscillator OFF; note 1	I_{DDO}	–	–	3	μA
Inputs/outputs (SDA)					
D_0 to D_5; MODE; STROBE					
Input voltage LOW	V_{IL}	0	–	0,3 x V_{DD}	V
Input voltage HIGH	V_{IH}	0,7 x V_{DD}	–	V_{DD}	V
D_2 to D_5; MODE; STROBE; A_0					
Pull-down input current $V_I = V_{DD}$	$-I_{IL}$	30	150	300	nA
SCL (D_0); SDA (D_1)					
Output current LOW (SDA) V_{OL} = 0,4 V	I_{OL}	3	–	–	mA
Clock frequency (see Fig. 11)	f_{SCL}	–	–	100	kHz
Input capacitance; $V_I = V_{SS}$	C_I	–	–	7	pF
Allowable input spike pulse width	t_I	–	–	100	ns

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
TONE output (see Fig. 15)					
DTMF output voltage levels (r.m.s. values)					
HIGH group	$V_{HG(rms)}$	158	192	205	mV
LOW group	$V_{LG(rms)}$	125	150	160	mV
DC voltage level	V_{DC}	–	½ V_{DD}	–	V
Pre-emphasis of group	ΔV_G	1,85	2,10	2,35	dB
Total harmonic distortion T_{amb} = 25 °C					
dual tone; note 2	THD	–	–25	–	dB
modem tone, note 3	THD	–	–29	–	dB
Output impedance	$\|Z_O\|$	–	0,1	0,5	kΩ
OSCI input					
Maximum allowable amplitude at OSCI	$V_{OSC(p-p)}$	–	–	$V_{DD}-V_{SS}$	V
Timing (V_{DD} = 3 V)					
Oscillator start-up time	$t_{OSC(ON)}$	–	3	–	ms
TONE start-up time; note 4	$t_{TONE(ON)}$	–	0,5	–	ms
STROBE pulse width; note 5	t_{STR}	400	–	–	ns
Data set-up time; note 5	t_{DS}	150	–	–	ns
Data hold time; note 5	t_{DH}	100	–	–	ns

Notes to the characteristics

1. Crystal is connected between OSCI and OSCO; D_0/SCL and D_1/SDA via a resistance of 5,6 kΩ to V_{DD}; all other pins left open.
2. Related to the level of the LOW group frequency component (CEPT CS46-03).
3. Related to the level of the fundamental frequency.
4. Oscillator must be running.
5. Values are referenced to the 10% and 90% levels of the relevant pulse amplitudes, with a total voltage swing from V_{SS} to V_{DD}.

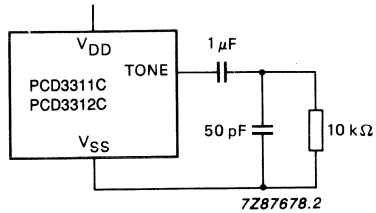


Fig. 15 TONE output test circuit.

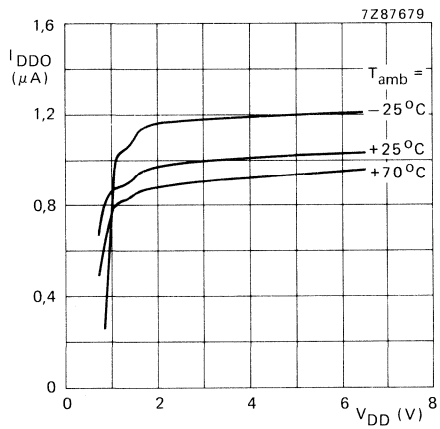


Fig. 16 Standby supply current as a function of supply voltage; oscillator OFF.

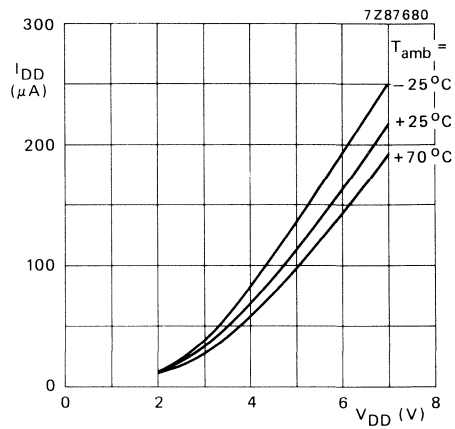


Fig. 17 Operating supply current as a function of supply voltage; oscillator ON; no output at TONE.

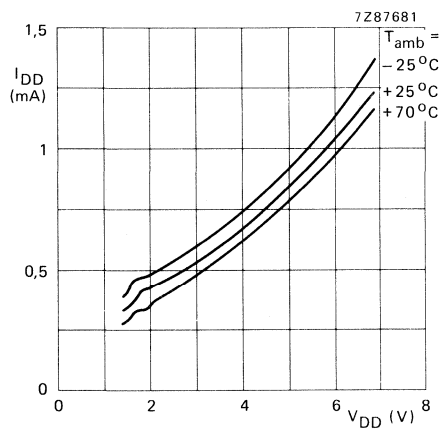


Fig. 18 Operating supply current as a function of supply voltage; oscillator ON; dual tone at TONE.

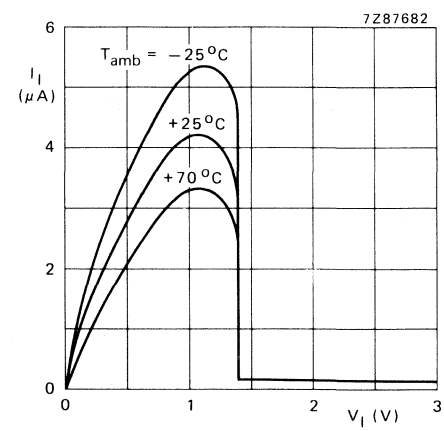


Fig. 19 Pull-down input current as a function of input voltage; V_{DD} = 3 V.

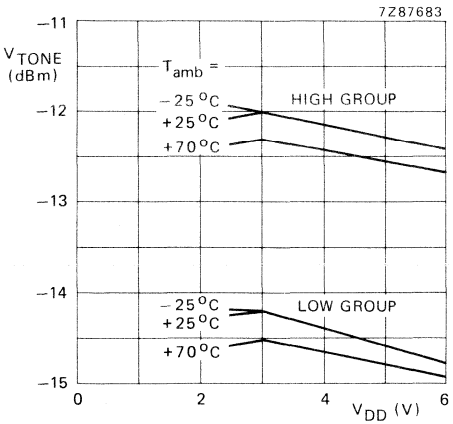


Fig. 20 DTMF output voltage levels as a function of operating supply voltage; R_L = 1 MΩ.

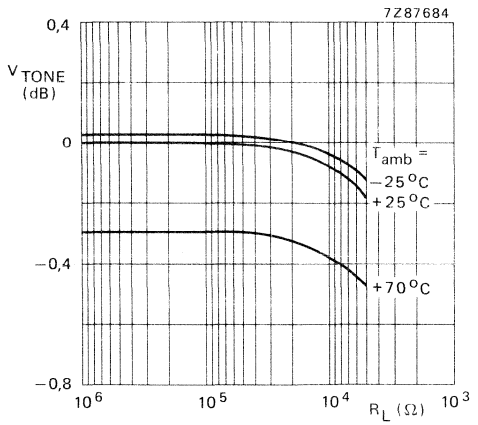


Fig. 21 Dual tone output voltage level as a function of output load resistance.

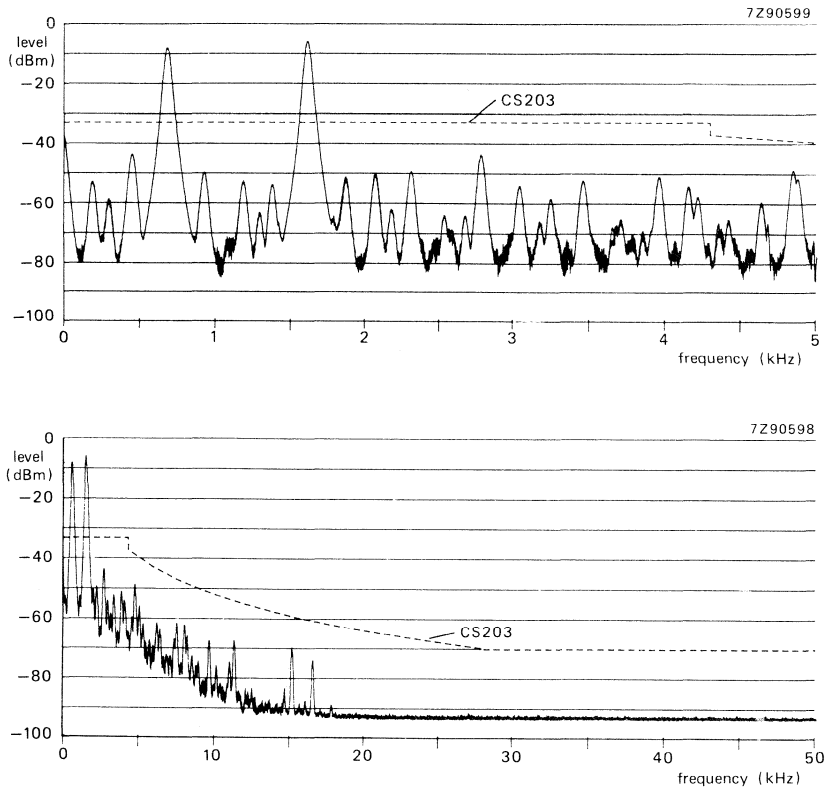


Fig. 22 Typical frequency spectrum of a dual tone signal after flat-band amplification of 6 dB.

APPLICATION INFORMATION

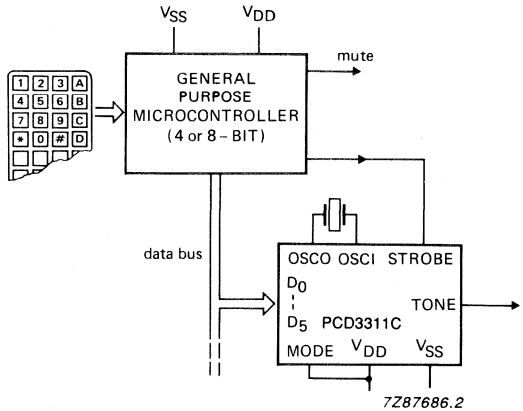


Fig. 23 PCD3311C driven by a microcontroller with parallel data bus.

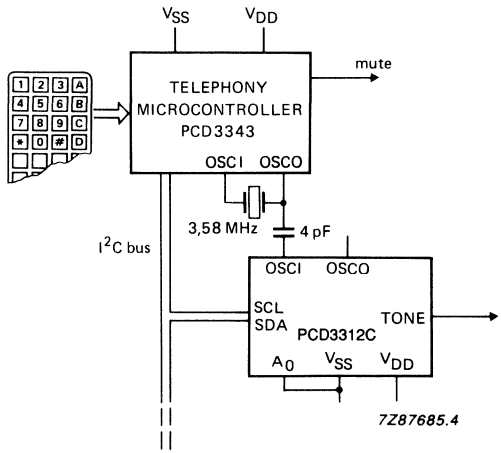


Fig. 24 PCD3312C driven by telephony microcontroller PCD3343 with serial I/O (I²C-bus).
The PCD3343 is a single-chip 8-bit microcontroller with 3K ROM/224 RAM bytes. The same application is possible with the PCD3311C with MODE = V_{SS}.

I²C-bus controller PCD8584

GENERAL DESCRIPTION

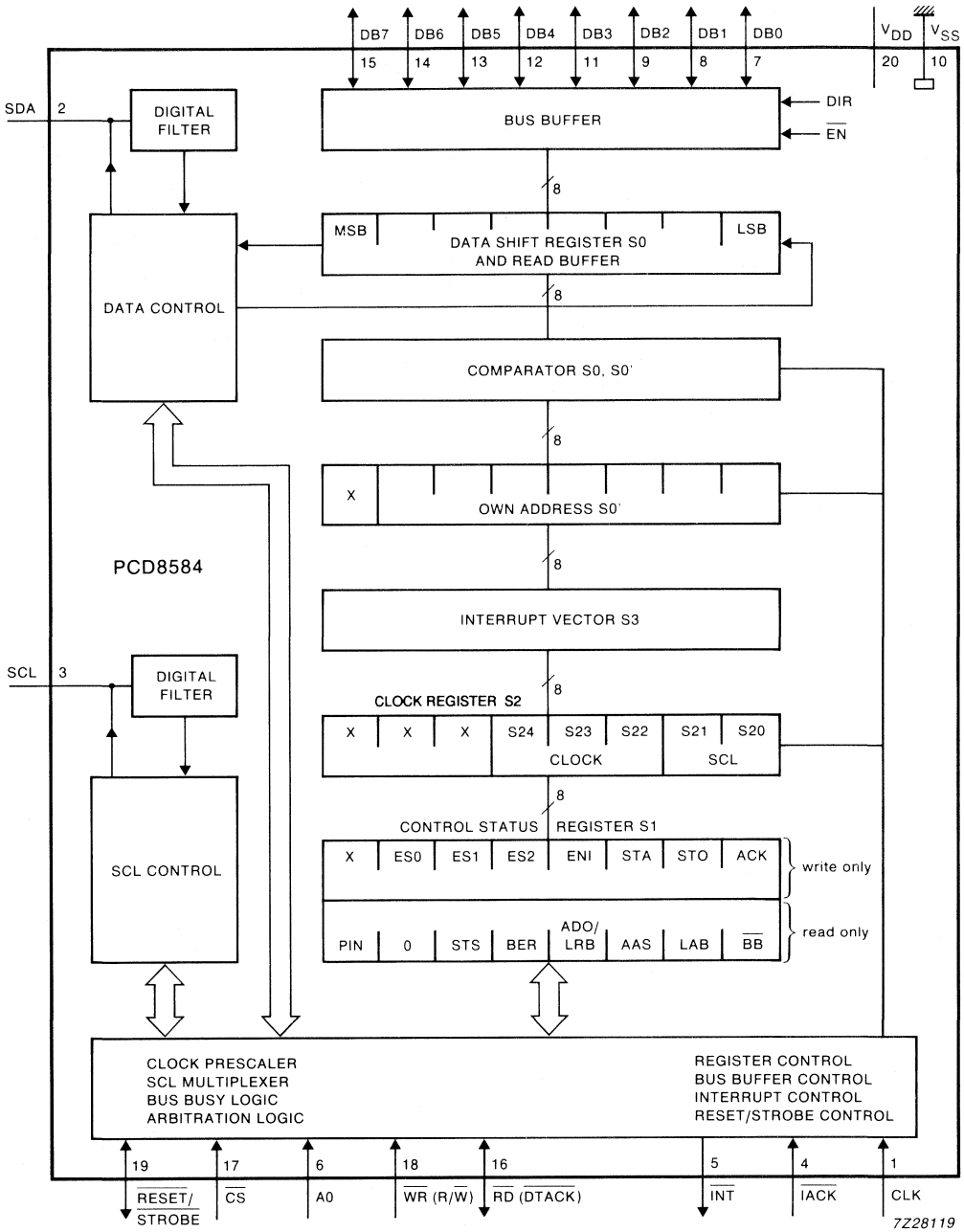
The PCD8584 is an integrated circuit designed in CMOS technology which serves as an interface between most standard parallel-bus microcontrollers/processors and the serial I²C-bus. The PCD8584 provides both master and slave functions. Communication with the I²C-bus is carried out on a byte-wise basis using interrupt or polled handshake. It controls all the I²C-bus specific sequencing, protocol, arbitration and timing. The PCD8584 allows parallel-bus systems to communicate bidirectionally with the I²C-bus.

Features

- Parallel-bus/I²C-bus protocol converter
- Compatible with most parallel-bus processors including MAB8049, MAB8051, SCN68000 and Z80
- Automatic selection of bus interface
- Programmable interrupt vector
- Multi-master capability
- I²C-bus monitor mode
- Long-distance mode
- Operating supply voltage 4.5 to 5.5 V
- Operating temperature range −20 to + 70 °C

PACKAGE OUTLINES

PCD8584P: 20-lead DIL; plastic (SOT146).
PCD8584T: 20-lead mini-pack; plastic (SO20; SOT163A).

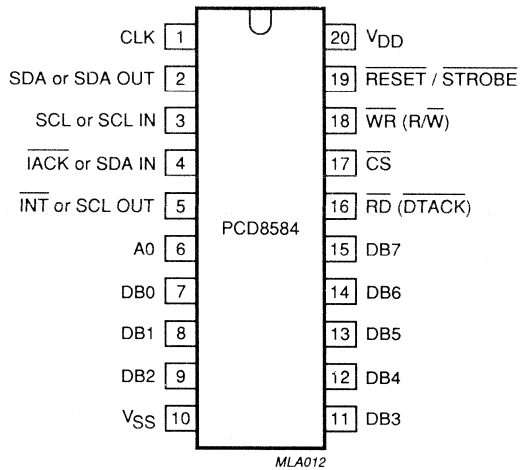


Where:

( ) indicate the SCN68000 pin name designations.
X = don't care.

Fig.1 Block diagram.

PINNING



Where:

( ) indicate the SCN68000 pin name designations.

Fig.2 Pinning diagram.

Pin functions

pin	mnemonic	function	description
1	CLK	I	Clock input from microprocessor clock generator (internal pull-up).
2	SDA or SDA OUT	I/O	I²C-bus serial data input/output (open-drain). Serial data output in long-distance mode.
3	SCL or SCL IN	I/O	I²C-bus serial clock input/output (open-drain). Serial clock input in long-distance mode.
4	$\overline{\text{IACK}}$ or SDA IN	I	Interrupt acknowledge input (internal pull-up); when this signal is asserted the interrupt vector in Register S2 will be available at the bus port if the ENI flag is set. Serial data input in long-distance mode.
5	$\overline{\text{INT}}$ or SCL OUT	O	Interrupt output (open-drain); this signal is enabled by the ENI flag in Register S1. It is asserted, when the PIN flag is reset. (PIN is reset after one byte is transmitted or received over the I²C-bus). Serial clock output in long-distance mode.
6	A0	I	Register select input (internal pull-up); this input selects between the control/status register and the other registers. Logic 1 selects Register S1, logic 0 selects one of the other registers depending on bits loaded in ES0, ES1 and ES2 of Register S1.
7	DB0	I/O	
8	DB1	I/O	Bidirectional 8-bit bus port.
9	DB2	I/O	
10	V_{SS}		Negative supply voltage.

Pin functions (continued)

pin	mnemonic	function	description
11	DB3	I/O	
12	DB4	I/O	
13	DB5	I/O	Bidirectional 8-bit bus port.
14	DB6	I/O	
15	DB7	I/O	
16	$\overline{RD}$ ($\overline{DTACK}$)	I (O)	$\overline{RD}$ is the read control input for MAB8049, MAB8051 or Z80-type processors. $\overline{DTACK}$ is the data transfer control output for 68000-type processors (open-drain).
17	$\overline{CS}$	I	Chip select input (internal pull-up).
18	$\overline{WR}$ (R/$\overline{W}$)	I	$\overline{WR}$ is the write control input for MAB8048, MAB8051 or Z80-type processors (internal pull-up). R/$\overline{W}$ control input for 68000-type processors.
19	$\overline{RESET}$/ $\overline{STROBE}$	I/O	Reset input (open-drain); this input forces the I²C-bus controller into a predefined state; all flags are reset, except PIN, which is set. Also functions as strobe output.
20	V_{DD}		Positive supply voltage.

FUNCTIONAL DESCRIPTION

General

The PCD8584 acts as an interface device between standard high-speed parallel buses and the serial I²C-bus. On the I²C-bus, it can act either as master or slave. Bidirectional data transfer between the I²C-bus and the parallel-bus microprocessor is carried out on a byte-wise basis, using either an interrupt or polled handshake. Interface to either 80XX-type (e.g. MAB8048, MAB8051, Z80) or 68000-type buses is possible. Selection of bus type is automatically performed (see **Interface mode control).**

Table 1 Control signals utilized by the PCD8584 for processor interfacing

type	R/$\overline{W}$	$\overline{WR}$	$\overline{RD}$	$\overline{DTACK}$	$\overline{IACK}$
MAB8049/51	NO	YES	YES	NO	NO
SCC68000	YES	NO	NO	YES	YES
Z80	NO	YES	YES	NO	YES

The structure of the PCD8584 is similar to that of the I²C-bus interface section of the MAB8400-series of microcontrollers, but with a modified control structure. The PCD8584 has five internal register locations. Three of these (Own Address register S0', Clock register S2 and Interrupt Vector S3) are used for initialization of the PCD8584. Normally they are only written once directly after resetting of the PCD8584. The remaining two registers function as double registers (Data Buffer/Shift register S0, and Control/Status register S1) which are used during actual data transmission/reception. By using these double registers, which are separately write and read accessible, overhead for register access is reduced. S0 is a combination of a shift register and data buffer. S0 performs all serial-to-parallel interfacing with the I²C-bus. S1 contains I²C-bus status information required for bus access and/or monitoring.

FUNCTIONAL DESCRIPTION (continued)

Interface mode control (IMC)

Selection of either an 80XX-mode or 68000-mode interface is achieved by detection of the $\overline{WR}$ - $\overline{CS}$ signal sequence. The concept takes advantage of the fact that the write control input is common for both types of interfaces. The chip is non-initialized after reset until register S0' is accessed. An 80XX-type interface is default. If a HIGH-to-LOW transition of $\overline{WR}$ (R/$\overline{W}$) is detected while $\overline{CS}$ is HIGH, the 68000-type interface mode is selected and the $\overline{DTACK}$ output is enabled.

Note:

The very first access to the PCD8584 after a reset must be a write access to register S0' in order to set the appropriate interface mode.

Set-up Registers S0', S2 and S3

Own Address Register S0'

When addressed as a slave, this register is loaded with the 7-bit I²C-bus address to which the PCD8584 is to respond. The "Addressed As Slave" (AAS) bit in Status register S1 is set when this address is received. Programming of this register is accomplished via the parallel-bus when A0 is LOW, with the appropriate bit combinations set in Control Status register S1 (S1 is written when A0 is HIGH). Bit combinations for accessing all registers are given in Tables 4 and 5. After reset S0' has default address '00' Hex.

Clock Register S2

Register S2 provides control over chip clock frequency and SCL clock frequency. S20 and S21 provide a selection of 4 different I²C-bus SCL frequencies which are shown in Table 2.

Table 2 Register S2 selection of SCL frequency

bit		SCL approximate frequency (kHz)
S21	S20	
0	0	90
0	1	45
1	0	11
1	1	1.5

S22, S23 and S24 are used for control of the internal clock prescaler. Due to the possibility of varying microprocessor clock signals, the prescaler can be programmed to adapt to 5 different clock rates, thus providing a constant internal clock. This is required to provide a stable time base for the SCL generator and the digital filters associated with the I²C-bus signals SCL and SDA. Selection for adaption to external clock rates is shown in Table 3. After reset, a clock frequency of 12 MHz is the default value.

Table 3 Register S2 selection of clock frequency

bit			clock frequency
S24	S23	S22	(MHz)
0	X	X	3
1	0	0	4.43
1	0	1	6
1	1	0	8
1	1	1	12

Where: X = don't care.

Interrupt Vector S3

The interrupt vector register provides an 8-bit user-programmable vector for vectored-interrupt microprocessors. The vector is sent to the bus port when an interrupt acknowledge signal is asserted and the ENI (enable interrupt) flag is set. Default vector values are as follows:

- Vector is '00' Hex in 80XX-mode
- Vector is '0F' Hex in 68000-mode

On reset the PCD8584 is in the 80XX mode, thus the default interrupt vector becomes '00' Hex.

Interface Registers S0 and S1

Data Shift Register S0

S0 acts as serial shift register interfacing to the I²C-bus. S0 is a combination of a shift register and a data buffer; parallel data is always written to the shift register and read from the data buffer. Serial data is shifted in/out the shift register, and in receiver mode the data from the shift register is copied to the data buffer during the acknowledge phase (see also PIN bit). All read and write operations to the I²C-bus are done via this register.

Control/Status Register S1

Register S1 is accessed by a HIGH signal on register select input A0. To facilitate communication between the microcontroller/processor and the I²C-bus, register S1 has separate read and write functions for all bit positions.

The write-only section has been split into 2 parts:

- The ESO (Enable Serial Output) enables or disables the serial output. When ESO is LOW, register access for initialization is possible. When ESO is HIGH, serial communication is enabled; communication with serial shift register S0 is enabled and the S1 bus status bits are made available for reading. Select control bits ES1 and ES2 control selection of other registers for initialization and control of normal operation. After these bits are programmed for access to the desired register (see Tables 4 and 5), the register is selected by a logic LOW level on register select pin A0.

Note:

With ESO = 0, bits ENI, STA, STO and ACK of S1 can be read for test purposes.

FUNCTIONAL DESCRIPTION (continued)

Control/Status Register S1 (continued)

Table 4 Register access control; ESO = logic 0 (serial interface off)

A0	ES1	ES1	$\overline{IACK}$	operation
H	X	X	X	READ/WRITE CONTROL REGISTER (S1) STATUS (S1) not available
L	0	0	X	READ/WRITE OWN ADDRESS (S0')
L	0	1	X	READ/WRITE INTERRUPT VECTOR (S3)
L	1	0	X	READ/WRITE CLOCK REGISTER (S2)

Table 5 Register access control; ESO = logic 1 (serial interface on)

A0	ES1	ES2	$\overline{IACK}$	operation
H	X	X	H	WRITE CONTROL REGISTER (S1)
H	X	X	H	READ STATUS REGISTER (S1)
L	X	0	H	READ/WRITE DATA (S0)
L	X	1	H	READ/WRITE INTERRUPT VECTOR (S3)
X	0	X	L	READ INTERRUPT VECTOR (acknowledge cycle)
X	1	X	L	long-distance mode

Instruction control bits ENI, STA, STO and ACK are used in normal operation to enable the interrupt output ($\overline{INT}$), generate I²C-bus START and STOP conditions, and program the acknowledge response, respectively. These possibilities are shown in Table 6.

Table 6 Instruction table for serial bus control

STA	STO	present mode	function	operation
1	0	SLV/REC	START	transmit START + address remain MST/TRM if R/$\overline{W}$ = logic 0; go to MST/REC if R/$\overline{W}$ = logic 1
1	0	MST/TRM	REPEAT START	same as for SLV/REC
0	1	MST/REC MST/TRM	STOP READ STOP WRITE	transmit stop go to SLV/REC mode (see note 1)
1	1	MST	DATA CHAINING	send STOP, START and address after last master frame without STOP sent (see note 2)
0	0	ANY	NOP	no operation (see note 3)

Notes to Table 6

1. In master-receiver mode, the last byte must be terminated with ACK bit HIGH (''negative-acknowledge''; see I²C-bus specification).
2. If both STA and STO are set HIGH simultaneously in master mode, a STOP condition followed by a START condition + address will be generated. This allows "chaining" of transmissions without relinquishing bus control.
3. All other STA, STO mode combinations not mentioned in Table 6 are NOPs.

The instruction bits are defined as follows:

- STA, STO: These bits control the generation of the I²C-bus START condition + transmission of slave address and R/$\overline{W}$ bit, generation of repeated START condition, and generation of the STOP condition.
- ENI: This bit enables the external interrupt output $\overline{INT}$, which is generated when the PIN bit is reset.
- ACK: This bit must be set normally to a '1'. This causes the I²C-bus controller to send an acknowledge automatically after each byte (this occurs during the ninth clock pulse). The bit must be reset when the I²C-bus controller is operating in master/receiver mode, and requires no further data to be sent from the slave transmitter. This causes a negative acknowledge on the I²C-bus, which halts further transmission from the slave device.

FUNCTIONAL DESCRIPTION (continued)

I²C-bus status information

The read-only section consists of I²C-bus status information. The functions are as follows:

- STS: When in slave-receiver mode, this flag is asserted when an externally generated STOP condition is detected (only used in slave-receiver mode).
- BER: Bus error. A misplaced START or STOP condition has been detected.
- LRB/AD0: Last Received Bit/Address 0 "General Call" Bit. This dual function status bit holds the value of the last received bit over the I²C-bus when AAS = 0. Normally this will be the value of the slave acknowledge; thus checking for slave acknowledgment is done via testing of the LRB bit. When AAS = 1 ("Address As Slave"), the I²C-bus controller has been addressed as a slave and this bit will be set if the slave address received was the "general call" address, or if it was the I²C-bus controller's slave address.
- AAS: "Addressed As Slave" bit. When acting as slave-receiver, this flag is set when an incoming address over the I²C-bus matches the value in Own Address register S0', or if the I²C-bus "general call" address ("00" Hex) has been received.
- LAB: "Lost Arbitration" bit. This bit is set when, in multmaster operation, arbitration is lost to another master on the I²C-bus.
- $\overline{BB}$: "Bus Busy" bit. This is read-only flag indicating when the I²C-bus is in use. A zero indicated that the bus is busy, and access is not possible. This bit is set/reset by STOP/START conditions.

PIN bit

The PIN bit "Pending Interrupt Not" is a read-only flag which is used to synchronize serial communication. Each time a serial data transmission is initiated (by setting the STA bit in the same register), the PIN will be set automatically. After successful transmission of one byte (9 clock pulses, including acknowledge), this bit will be automatically reset indicating a complete byte transmission. When the ENI bit is also set, the PIN flag triggers an external interrupt via the $\overline{INT}$ output when PIN is reset. When in receiver mode, the PIN bit is also reset on completion of each received byte. In polled applications, the PIN bit is tested to determine when a serial transmission has been completed. During register transfers the I²C-bus controller Data Register S0 and its internal shift register (not accessible directly), the I²C-bus controller will delay serial transmission by holding the SCL line LOW until the PIN bit becomes set. In receiver mode, the PIN bit is automatically set when the data register S0 is read. When the PIN bit becomes set all status bits will be reset, with exception of $\overline{BB}$.

Multi-master operations

To avoid conflict between data and repeated START and STOP operations, multi-master systems have some limitations:

- Transmissions requiring a repeated START condition must have identical format among all potential masters for both read and write operations
- For correct arbitration masters may only attempt to send data simultaneously to the same location, if they use the same formats (i.e. number of data bytes, location of the repeated START, etc.). If this condition is designed not to occur, differing formats may be used.

Reset A low-level pulse on the $\overline{RESET}$ input forces the I²C-bus controller into a well-defined state. All flags are reset (zero state), except the PIN flag, which is set. The $\overline{RESET}$ pin is also used for the $\overline{STROBE}$ output signal. Both functions are separated on-chip by a digital filter. The reset input signal has to be sufficiently long (minimum 30 clock cycles) to pass through the filter. The $\overline{STROBE}$ output signal is sufficiently short (8 clock cycles) to be blocked by the filter. For more detailed information on the Strobe function see **Special function modes.**

FUNCTIONAL DESCRIPTION (continued)

Comparison to the MAB8400 I²C-bus interface

The structure of the PCD8584 is similar to that of the MAB8400 series of microcontrollers, but with a modified control structure. Access to all I²C-bus control and status registers is done via the parallel-bus port in conjunction with register select input A0, and control bits ESO, ES1 and ES2. The main differences are highlighted below.

Deleted functions

The following functions are not available in the PCD8584:

- Always selected (ALS flag)
- Access to the bit counter (BC0 to BC2)
- Full SCL frequency selection (2 bits instead of 5 bits)
- The non-acknowledge mode (ACK flag)
- Asymmetrical clock (ASC flag)

Added functions

The following functions either replace the deleted functions or are completely new:

- Chip clock prescaler
- Assert acknowledge bit (ACK flag)
- Register selection bits (ES1 and ES2 flags)
- Additional status flags
- Automatic interface control between 80XX and 68000-type microprocessors
- Programmable interrupt vector
- Strobe generator
- Bus monitor function
- Long-distance mode (non-I²C-bus mode; only for communication between remote parallel-bus processors)

Special function modes

Strobe

When the I²C-bus controller receives its own address (or the "00" Hex general call address) followed immediately by a STOP condition (i.e. no further data transmitted after the address), a strobe output signal is generated at the $\overline{\text{RESET}}/\overline{\text{STROBE}}$ pin (pin 19). The $\overline{\text{STROBE}}$ signal consists of a monostable output pulse (active LOW), eight clock cycles long (see Fig.10). It is generated after the STOP condition is received, preceded by the correct slave address. This output can be used as a bus access controller for multi-master parallel-bus systems (see Fig.14).

Long-distance mode

The long-distance mode provides a serial communication link between parallel processors using two or more I²C-bus controllers. This mode is selected by setting ES1 to logic 1 while the serial interface is enabled (ESO = 1). In this mode the I²C-bus protocol is transmitted over 4 unidirectional lines, SDA, OUT, SCL IN, SDA IN and SCL OUT (pins 2, 3, 4 and 5). These communication lines should be connected to the line drivers/receivers for long distance applications. Specification for long distance transmission is then given by the chosen standard. Control of bus frequency, data transmission etc. is the same as in normal I²C-bus mode. After reading or writing data to shift register SO, long-distance mode must be initialized by setting ESO and ES1 to logic 1. Because the interrupt output $\overline{\text{INT}}$ is not available in this operating mode, data reception must be polled.

Monitor mode

When the 7-bit Own Address register S0' is loaded with all zeros, the I²C-bus controller acts as a passive I²C monitor. The main features of the monitor mode are as follows:

- The controller is always selected
- The controller is always in the slave-receiver mode
- The controller never generates an acknowledge
- The controller never generates an interrupt request
- A pending interrupt condition does not force SCL LOW
- Received data is automatically transferred to the read buffer
- Bus traffic is monitored by the PIN bit, which is reset after the acknowledge bit has been transmitted and is set as soon as the first bit of the next byte is detected

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage range (pin 20)	V_{DD}	−0.3	+ 7.0	V
Voltage range on any input*	V_I	−0.8	V_{DD} + 0.5	V
DC input current (any input)	$\pm I_I$	–	10	mA
DC output current (any output)	$\pm I_O$	–	10	mA
Total power dissipation	P_{tot}	–	300	mW
Power dissipation per output	P_O	–	50	mW
Operating ambient temperature range	T_{amb}	−20	+ 70	°C
Storage temperature range	T_{stg}	−65	+ 150	°C

Note to the Ratings

Stresses above those listed in accordance with Absolute Maximum System may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating condition for extended periods may affect reliability.

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is good practice to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

CHARACTERISTICS

V_{DD} = 5 ± 10%; V_{SS} = 0 V; T_{amb} = −20 to + 70 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage range		V_{DD}	4.5	5.0	5.5	V
Supply current						
standby	note 1	I_{DD1}	–	–	2.5	μA
operating	note 2	I_{DD2}	–	–	1.5	mA
Inputs						
SCL, SDA						
Input voltage LOW	note 3	V_{IL1}	0	–	0.8	V
Input voltage HIGH	note 3	V_{IH1}	2.0	–	V_{DD}	V
Input voltage LOW	note 4	V_{IL2}	0	–	$0.3V_{DD}$	V
Input voltage HIGH	note 4	V_{IH2}	$0.7V_{DD}$	–	V_{DD}	V
Resistance to V_{DD}	T_{amb} = 25 °C; note 5	R_i	25	–	100	kΩ
Outputs						
Output current LOW	V_{OL} = 0.4 V	I_{OL}	3.0	–	–	mA
Output current HIGH	V_{OH} = 2.4 V; note 6	$-I_{OH}$	2.4	–	–	mA
Leakage current	note 7	$\pm I_{LO}$	–	–	1	μA

Notes to the characteristics

1. 22 kΩ pull-ups on D0 to D7; 10 kΩ pull-ups on SDA, SCL, $\overline{RD}$; $\overline{RESET}$ tied to V_{SS}; remaining pins open-circuit.
2. Same as note 1, but CLK waveform with 50% duty factor at 12 MHz.
3. CLK, $\overline{IACK}$, A0, $\overline{CS}$, $\overline{WR}$, $\overline{RD}$, $\overline{RESET}$, TTL level inputs.
4. SDA, SCL, D0 to D7, CMOS level inputs.
5. CLK, $\overline{IACK}$, A0, $\overline{CS}$, $\overline{WR}$.
6. D0 to D7.
7. D0 to D7 3-state, SDA, SCL, $\overline{INT}$, $\overline{RD}$, $\overline{RESET}$.

Timing specifications

All the timing values are valid within the operating supply voltage and ambient temperature range and refer to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.

parameter	symbol	min.	typ.	max.	unit
I²C-bus timing					
SCL clock frequency	f_{SCL}	–	–	100	kHz
Tolerable bus spike width	t_{SW}	–	–	100	ns
Bus free time	t_{BUF}	4.7	–	–	μs
Start condition set-up time	$t_{SU;STA}$	4.7	–	–	μs
Start condition hold time	$t_{HD;STA}$	4.0	–	–	μs
SCL LOW time	t_{LOW}	4.7	–	–	μs
SCL HIGH time	t_{HIGH}	4.0	–	–	μs
SCL and SDA rise time	t_r	–	–	1.0	μs
SCL and SDA fall time	t_f	–	–	0.3	μs
Data set-up time	$t_{SU;DAT}$	250	–	–	ns
Data hold time	$t_{HD;DAT}$	0	–	–	ns
SCL LOW to data out valid	$t_{VD;DAT}$	–	–	3.4	μs
Stop condition set-up time	$t_{SU;STO}$	4.0	–	–	μs

Parallel interface timing (see Figs 3 to 10)

All the timing limits are valid within the operating supply voltage and ambient temperature range and refer to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.
C_L = 100 pF, R_L = 1.5 kΩ (connected to V_{DD}) for open-drain and high-impedance outputs, where applicable (for measurement purposes only).

parameter	figure	symbol	min.	typ.	max.	unit
Clock rise time	3	t_r	–	–	6	ns
Clock fall time	3	t_f	–	–	6	ns
Input clock period (50% duty factor)	3	t_{CLK}	83	–	333	ns
$\overline{CS}$ set-up to $\overline{RD}$, $\overline{WR}$ LOW	4	t_{SU1}	30	–	–	ns
$\overline{CS}$ hold from $\overline{RD}$, $\overline{WR}$ HIGH	4	t_{HD1}	0	–	–	ns
A0 set-up to $\overline{RD}$, $\overline{WR}$ LOW	4	t_{SU2}	10	–	–	ns
A0 hold from $\overline{RD}$, $\overline{WR}$ HIGH	4	t_{HD2}	20	–	–	ns
$\overline{WR}$ pulse width	4	t_{W1}	230	–	–	ns
$\overline{RD}$ pulse width	4	t_{W2}	230	–	–	ns
Data set-up before $\overline{WR}$ HIGH	4	t_{SU3}	150	–	–	ns
Data valid after $\overline{RD}$ LOW	4	t_{VD}	–	110	180	ns
Data hold after $\overline{WR}$ HIGH	4	t_{HD3}	30	–	–	ns
Data bus floating after $\overline{RD}$ HIGH	4	t_{FL}	70	–	–	ns
A0 set-up to $\overline{CS}$ LOW	5 and 6	t_{SU4}	30	–	–	ns
R/$\overline{WR}$ set-up to $\overline{CS}$ LOW	5 and 6	t_{SU5}	30	–	–	ns
Data valid after $\overline{CS}$ LOW	5	t_{VD1}	–	110	180	ns
$\overline{DTACK}$ LOW after $\overline{CS}$ LOW	5 and 6	t_{d1}	–	$3t_{CLK}+75$	$3t_{CLK}+150$	ns
A0 hold from $\overline{CS}$ HIGH	5 and 6	t_{HD4}	0	–	–	ns
R/$\overline{WR}$ hold from $\overline{CS}$ HIGH	5 and 6	t_{HD5}	0	–	–	ns
Data hold after $\overline{CS}$ HIGH	5	t_{HD6}	160	–	–	ns
$\overline{DTACK}$ HIGH from $\overline{CS}$ HIGH	5 and 6	t_{d2}	–	100	120	ns
Data hold after $\overline{CS}$ HIGH	6	t_{HD7}	0	–	–	ns
Data set-up to $\overline{CS}$ LOW	6	t_{SU6}	0	–	–	ns
$\overline{INT}$ HIGH from $\overline{IACK}$ LOW	7 and 8	t_{d3}	–	130	180	ns
Data valid after $\overline{IACK}$ LOW	7 and 8	t_{VD2}	–	140	190	ns

Parallel interface timing (continued)

parameter	figure	symbol	min.	typ.	max.	unit
$\overline{IACK}$ pulse width	7 and 8	t_{W3}	230	–	–	ns
Data hold after $\overline{IACK}$ HIGH	7 and 8	t_{HD8}	100	–	–	ns
$\overline{DTACK}$ LOW from $\overline{IACK}$ LOW	8	t_{d4}	–	$3t_{CLK}+75$	$3t_{CLK}+150$	ns
$\overline{DTACK}$ HIGH from $\overline{IACK}$ HIGH	8	t_{d5}	–	120	140	ns
Reset pulse width	9	t_{W4}	$30t_{CLK}$	–	–	ns
Strobe pulse width	10	t_{W5}	$8t_{CLK}$	$8t_{CLK}+90$	–	ns

Notes to parallel interface timing

1. A minimum of 6 clock cycles must elapse between consecutive parallel-bus accesses when the I²C-bus controller operates at 8 or 12 MHz. This may be reduced to 3 clock cycles for lower operating frequencies.
2. After reset the chip clock default is 12 MHz.

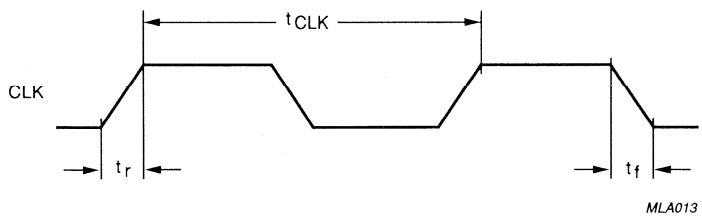
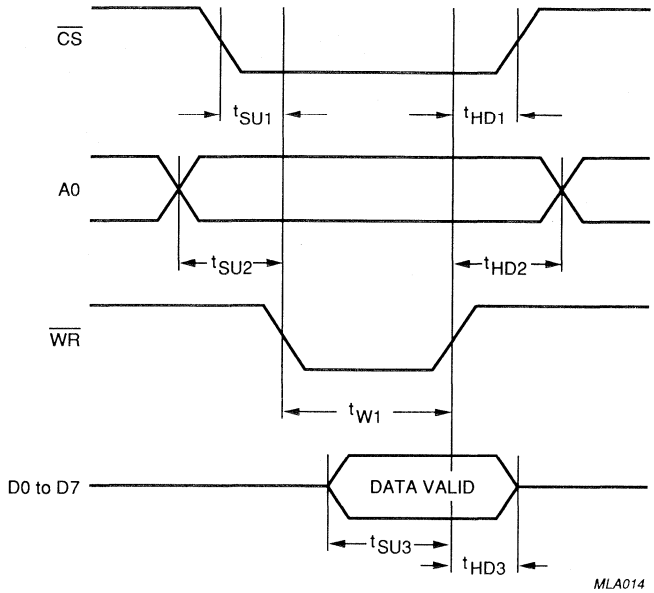
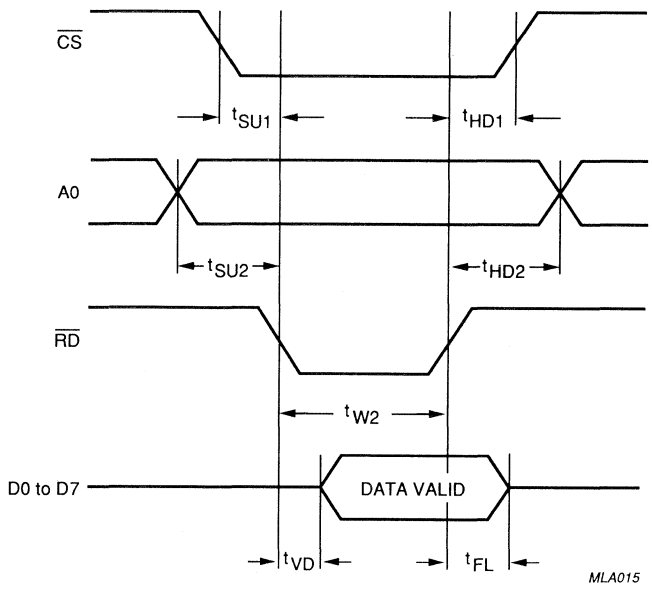


Fig.3 Clock input timing.

Timing diagrams



(a)



(b)

Fig. 4 Bus timing (80XX-mode); (a) write cycle, (b) read cycle.

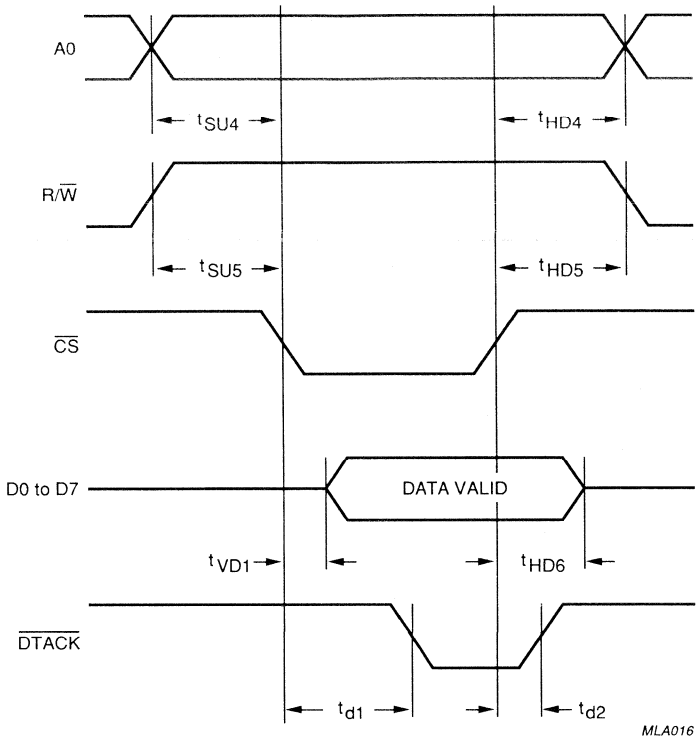


Fig.5 Bus timing; 68000-mode read cycle.

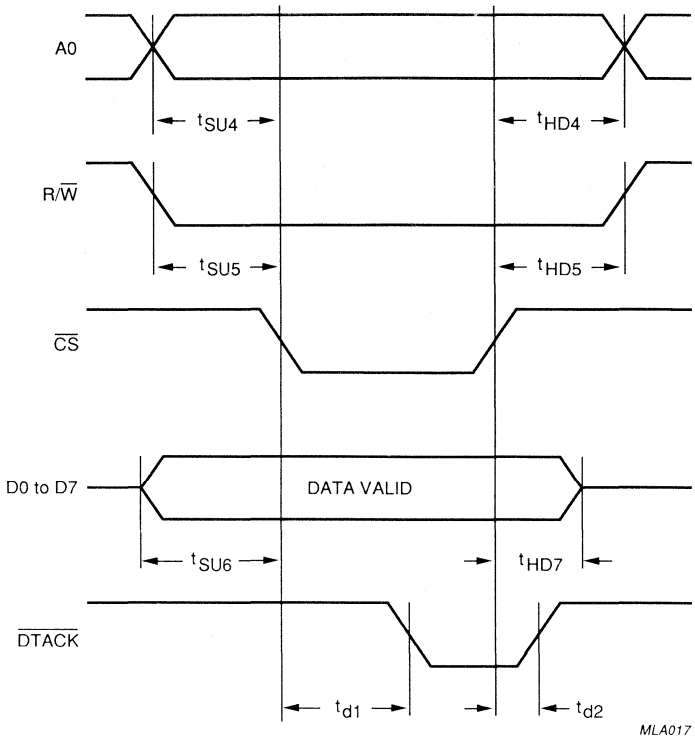


Fig.6 Bus timing; 68000-mode write cycle.

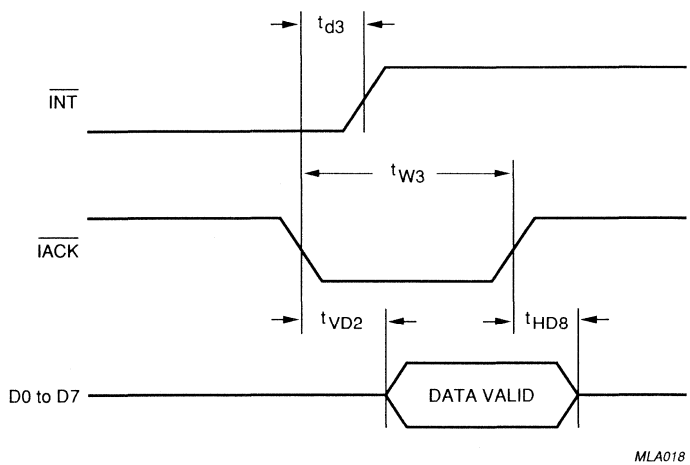


Fig.7 Interrupt timing; 80XX-mode.

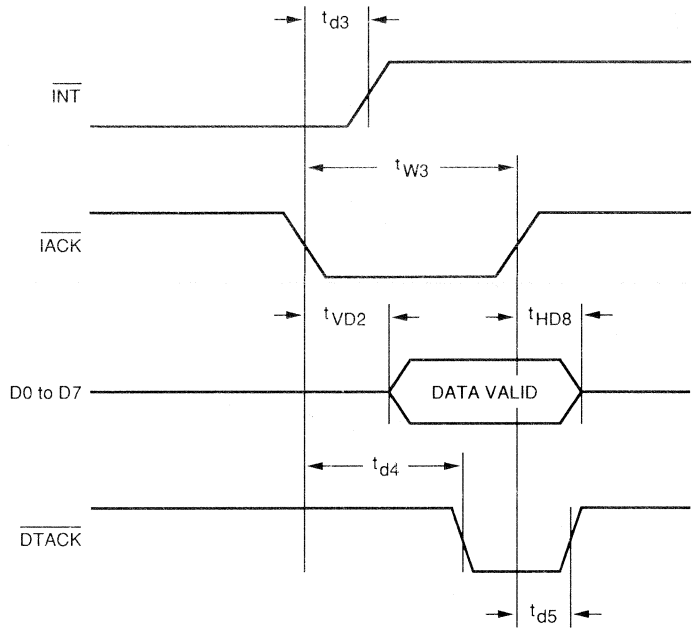


Fig.8 Interrupt timing; 68000-mode.

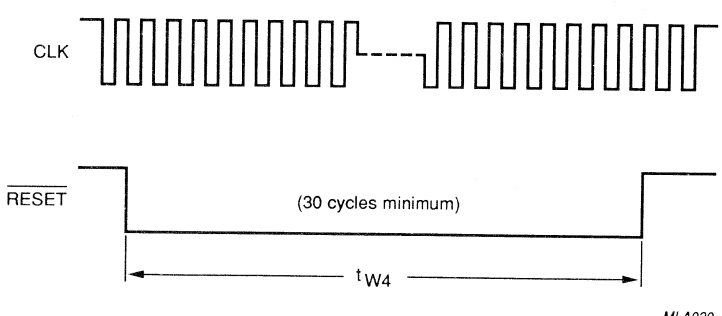


Fig.9 Reset timing.

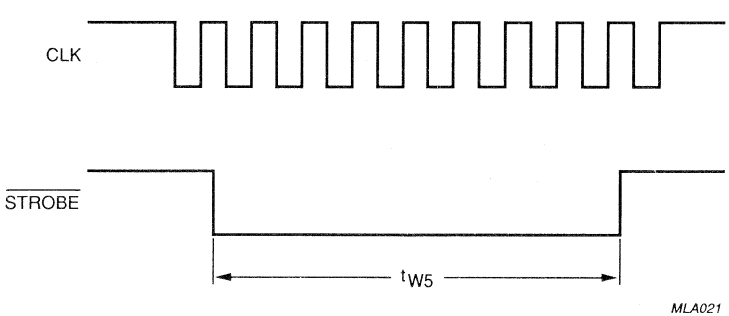


Fig.10 Strobe timing.

APPLICATION INFORMATION

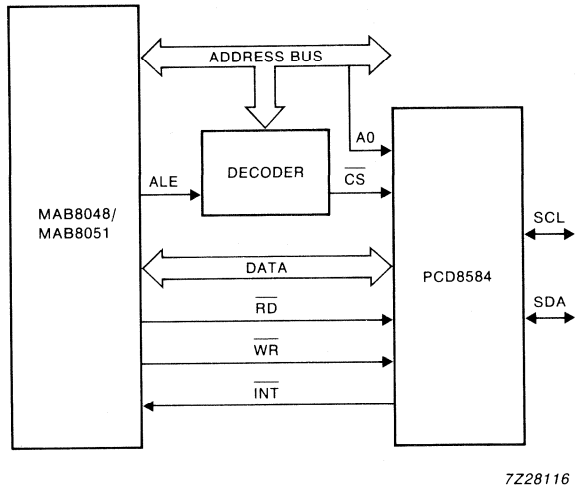


Fig.11 Application diagram using the MAB8048/MAB8051.

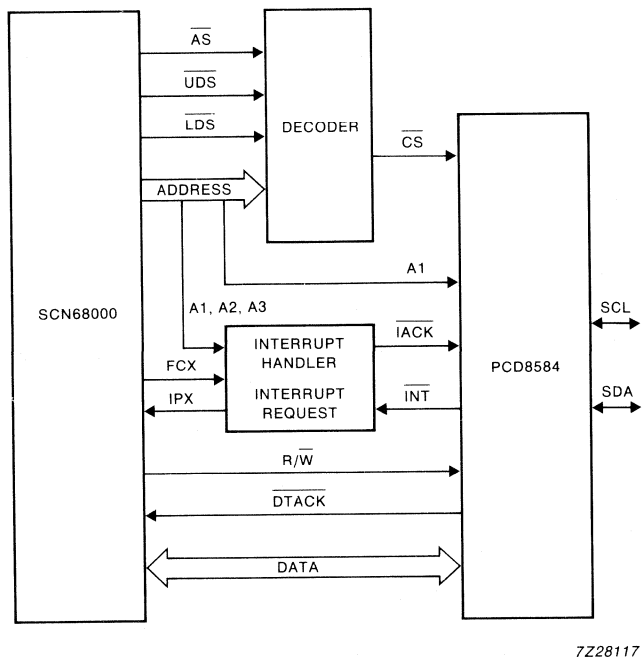


Fig.12 Application diagram using the SCN68000.

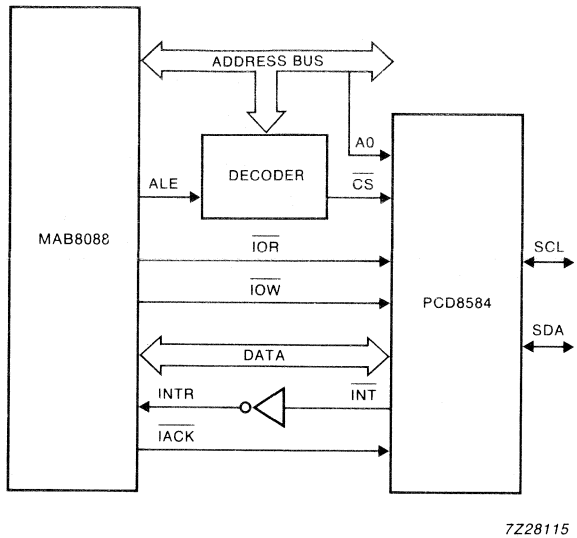


Fig.13 Application diagram using the 8088.

APPLICATION INFORMATION (continued)

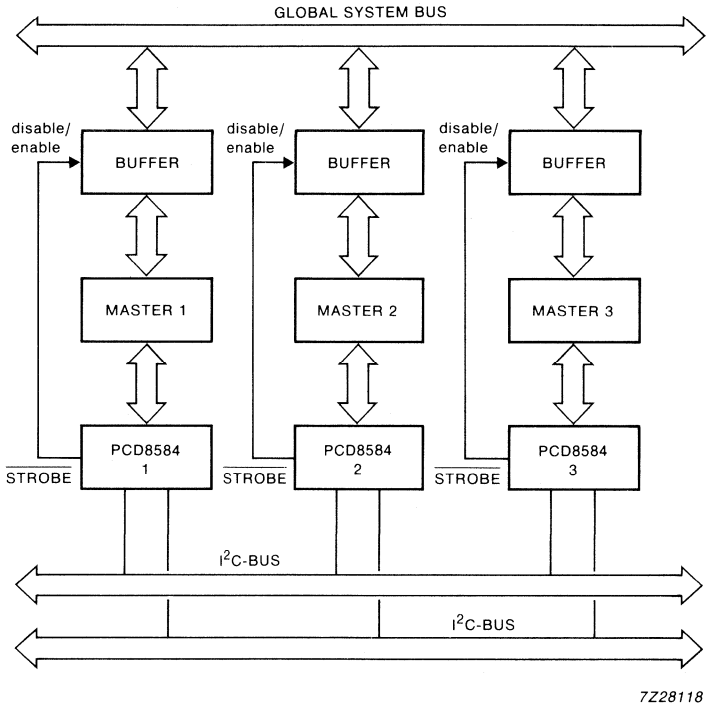


Fig.14 $\overline{\text{STROBE}}$ as bus access controller.

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

Universal LCD driver for low multiplex rates PCF8566

GENERAL DESCRIPTION

The PCF8566 is a peripheral device which interfaces to almost any liquid crystal display (LCD) having low multiplex rates. It generates the drive signals for any static or multiplexed LCD containing up to four backplanes and up to 24 segments and can easily be cascaded for larger LCD applications. The PCF8566 is compatible with most microprocessors/microcontrollers and communicates via a two-line bidirectional bus (I²C). Communication overheads are minimized by a display RAM with auto-incremented addressing, by hardware subaddressing and by display memory switching (static and duplex drive modes).

Features

- Single-chip LCD controller/driver
- Selectable backplane drive configuration: static or 2/3/4 backplane multiplexing
- Selectable display bias configuration: static, 1/2 or 1/3
- Internal LCD bias generation with voltage-follower buffers
- 24 segment drives: up to twelve 8-segment numeric characters; up to six 15-segment alphanumeric characters; or any graphics of up to 96 elements
- 24 x 4-bit RAM for display data storage
- Auto-incremented display data loading across device subaddress boundaries
- Display memory bank switching in static and duplex drive modes
- Versatile blinking modes
- LCD and logic supplies may be separated
- 2,5 V to 6 V power supply range
- Low power consumption
- Power-saving mode for extremely low power consumption in battery-operated and telephone applications
- I²C bus interface
- TTL/CMOS compatible
- Compatible with any 4-bit, 8-bit or 16-bit microprocessors/microcontrollers
- May be cascaded for large LCD applications (up to 1536 segments possible)
- Cascadable with the 40 segment LCD driver PCF8576
- Optimized pinning for single plane wiring in both single and multiple PCF8566 applications
- Space-saving 40-lead plastic mini-pack (VSO-40; SOT-158A)
- No external components required (even in multiple device applications)
- Manufactured in silicon gate CMOS process

PACKAGE OUTLINES

PCF8566P: 40-lead DIL; plastic (SOT129).
PCF8566T: 40-lead mini-pack (VSO40; SOT158A).

Universal LCD driver for low multiplex rates | PCF8566

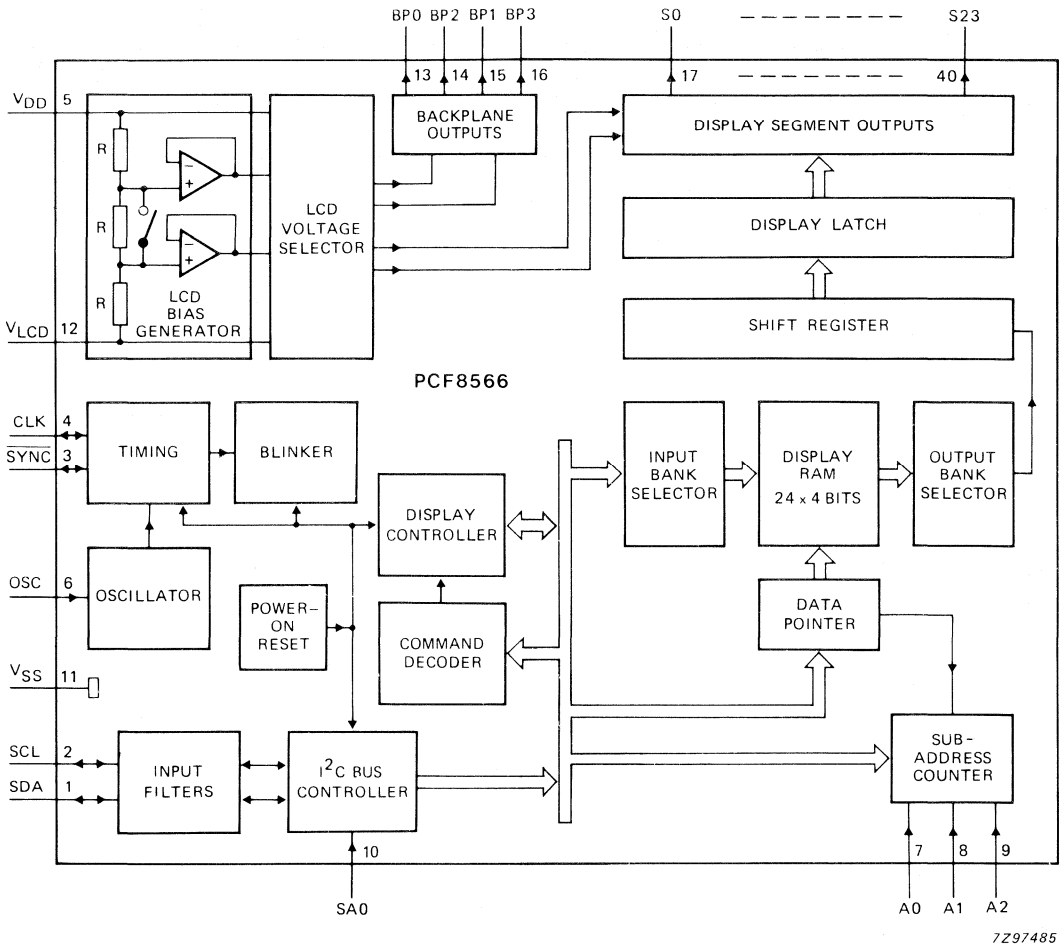


Fig. 1 Block diagram.

Universal LCD driver for low multiplex rates PCF8566

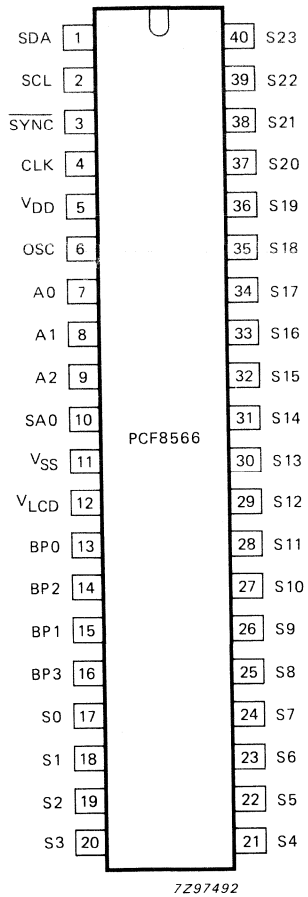


Fig. 2 Pinning diagram.

PINNING

1	SDA	I²C bus data input/output
2	SCL	I²C bus clock input/output
3	$\overline{\text{SYNC}}$	cascade synchronization input/output
4	CLK	external clock input/output
5	V_{DD}	positive supply voltage
6	OSC	oscillator input
7	A0	I²C bus subaddress inputs
8	A1	
9	A2	
10	SA0	I²C bus slave address bit 0 input
11	V_{SS}	logic ground
12	V_{LCD}	LCD supply voltage
13	BP0	LCD backplane outputs
14	BP2	
15	BP1	
16	BP3	
17	S0	LCD segment outputs
to	to	
40	S23	

FUNCTIONAL DESCRIPTION

The PCF8566 is a versatile peripheral device designed to interface any microprocessor to a wide variety of LCDs. It can directly drive any static or multiplexed LCD containing up to four backplanes and up to 24 segments. The display configurations possible with the PCF8566 depend on the number of active backplane outputs required; a selection of display configurations is given in Table 1.

Table 1 Selection of display configurations

active back-plane outputs	no. of segments	7-segment numeric	14-segment alphanumeric	dot matrix
4	96	12 digits + 12 indicator symbols	6 characters + 12 indicator symbols	96 dots (4 x 24)
3	72	9 digits + 9 indicator symbols	4 characters + 16 indicator symbols	72 dots (3 x 24)
2	48	6 digits + 6 indicator symbols	3 characters + 6 indicator symbols	48 dots (2 x 24)
1	24	3 digits + 3 indicator symbols	1 characters + 10 indicator symbols	24 dots

All of the display configurations given in Table 1 can be implemented in the typical system shown in Fig. 3. The host microprocessor/microcontroller maintains the two-line I²C bus communication channel with the PCF8566. The internal oscillator is selected by tying OSC (pin 6) to V_{SS}. The appropriate biasing voltages for the multiplexed LCD waveforms are generated internally. The only other connections required to complete the system are to the power supplies (V_{DD}, V_{SS} and V_{LCD}) and to the LCD panel chosen for the application.

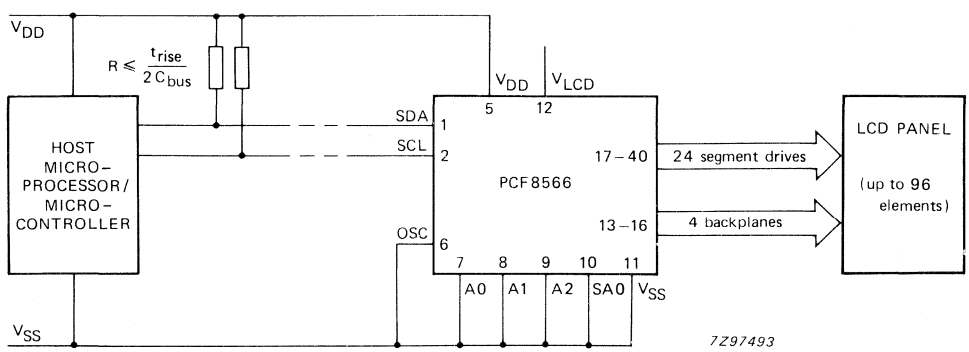


Fig. 3 Typical system configuration.

Power-on reset

At power-on the PCF8566 resets to a defined starting condition as follows:

1. All backplane outputs are set to V_{DD}.
2. All segment outputs are set to V_{DD}.
3. The drive mode '1 : 4 multiplex with 1/3 bias' is selected.
4. Blinking is switched off.
5. Input and output bank selectors are reset (as defined in Table 5).
6. The I²C bus interface is initialized.
7. The data pointer and the subaddress counter are cleared.

Data transfers on the I²C bus should be avoided for 1 ms following power-on to allow completion of the reset action.

LCD bias generator

The full-scale LCD voltage (V_{op}) is obtained from $V_{DD} - V_{LCD}$. The LCD voltage may be temperature compensated externally through the V_{LCD} supply to pin 12. Fractional LCD biasing voltages are obtained from an internal voltage divider of three series resistors connected between V_{DD} and V_{LCD}. The centre resistor can be switched out of circuit to provide a ½ bias voltage level for the 1 : 2 multiplex configuration.

LCD voltage selector

The LCD voltage selector coordinates the multiplexing of the LCD according to the selected LCD drive configuration. The operation of the voltage selector is controlled by MODE SET commands from the command decoder. The biasing configurations that apply to the preferred modes of operation, together with the biasing characteristics as functions of $V_{op} = V_{DD} - V_{LCD}$ and the resulting discrimination ratios (D), are given in Table 2.

Table 2 Preferred LCD drive modes: summary of characteristics

LCD drive mode	LCD bias configuration	$\frac{V_{off(rms)}}{V_{op}}$	$\frac{V_{on\ (rms)}}{V_{op}}$	$D = \frac{V_{on(rms)}}{V_{off(rms)}}$
static (1 BP)	static (2 levels)	0	1	∞
1 : 2 MUX (2 BP)	1/2 (3 levels)	$\sqrt{2}/4 = 0{,}354$	$\sqrt{10}/4 = 0{,}791$	$\sqrt{5} = 2{,}236$
1 : 2 MUX (2 BP)	1/3 (4 levels)	$1/3 = 0{,}333$	$\sqrt{5}/3 = 0{,}745$	$\sqrt{5} = 2{,}236$
1 : 3 MUX (3 BP)	1/3 (4 levels)	$1/3 = 0{,}333$	$\sqrt{33}/9 = 0{,}638$	$\sqrt{33}/3 = 1{,}915$
1 : 4 MUX (4 BP)	1/3 (4 levels)	$1/3 = 0{,}333$	$\sqrt{3}/3 = 0{,}577$	$\sqrt{3} = 1{,}732$

LCD voltage selector (continued)

A practical value for V_{op} is determined by equating $V_{off(rms)}$ with a defined LCD threshold voltage (V_{th}), typically when the LCD exhibits approximately 10% contrast. In the static drive mode a suitable choice is $V_{op} \gtrapprox 3\ V_{th}$.
Multiplex drive ratios of 1 : 3 and 1 : 4 with 1/2 bias are possible but the discrimination and hence the contrast ratios are smaller ($\sqrt{3} = 1{,}732$ for 1 : 3 multiplex or $\sqrt{21}/3 = 1{,}528$ for 1 : 4 multiplex).
The advantage of these modes is a reduction of the LCD full scale voltage V_{op} as follows:

1 : 3 multiplex (1/2 bias) : $V_{op} = \sqrt{6}\ V_{off(rms)} = 2{,}449\ V_{off(rms)}$

1 : 4 multiplex (1/2 bias) : $V_{op} = 4\sqrt{3}/3\ V_{off(rms)} = 2{,}309\ V_{off(rms)}$

These compare with $V_{op} = 3\ V_{off(rms)}$ when 1/3 bias is used.

LCD drive mode waveforms

The static LCD drive mode is used when a single backplane is provided in the LCD. Backplane and segment drive waveforms for this mode are shown in Fig. 4.

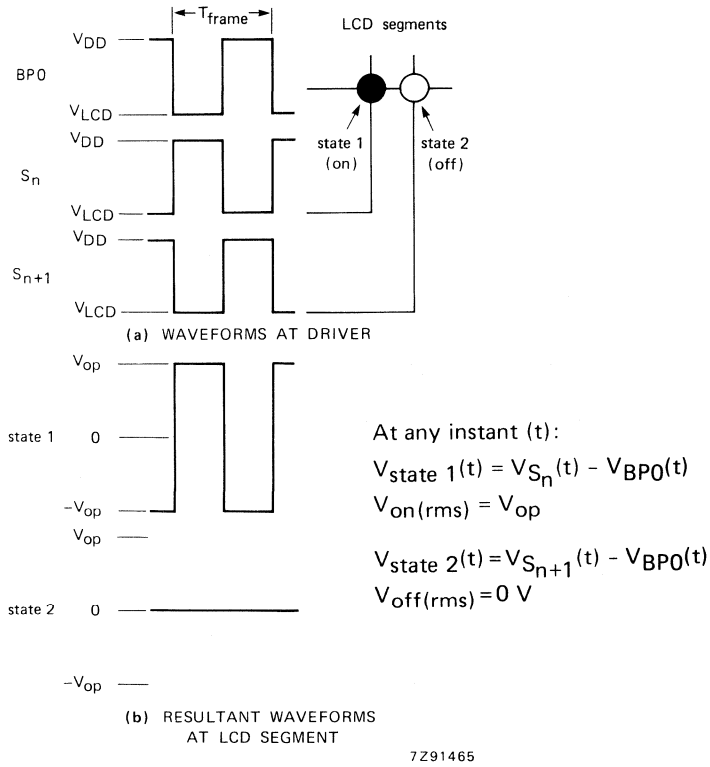


Fig. 4 Static drive mode waveforms: $V_{op} = V_{DD} - V_{LCD}$.

When two backplanes are provided in the LCD the 1 : 2 multiplex drive mode applies. The PCF8566 allows use of 1/2 or 1/3 bias in this mode as shown in Figs 5 and 6.

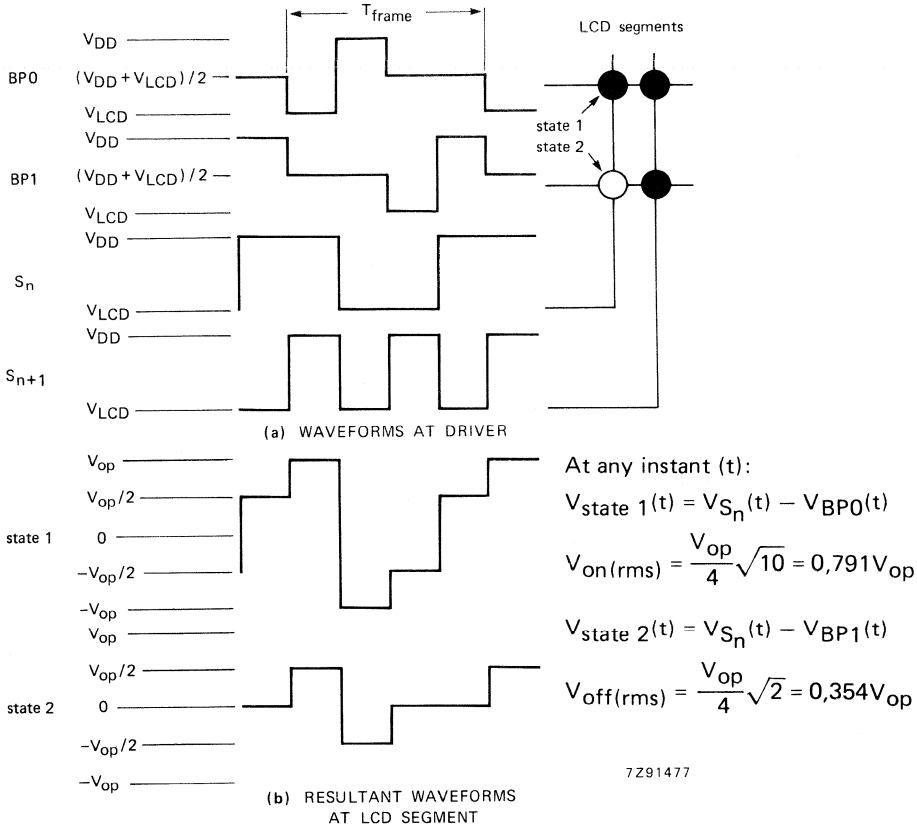


Fig. 5 Waveforms for 1 : 2 multiplex drive mode with 1/2 bias: $V_{op} = V_{DD} - V_{LCD}$.

LCD drive mode waveforms (continued)

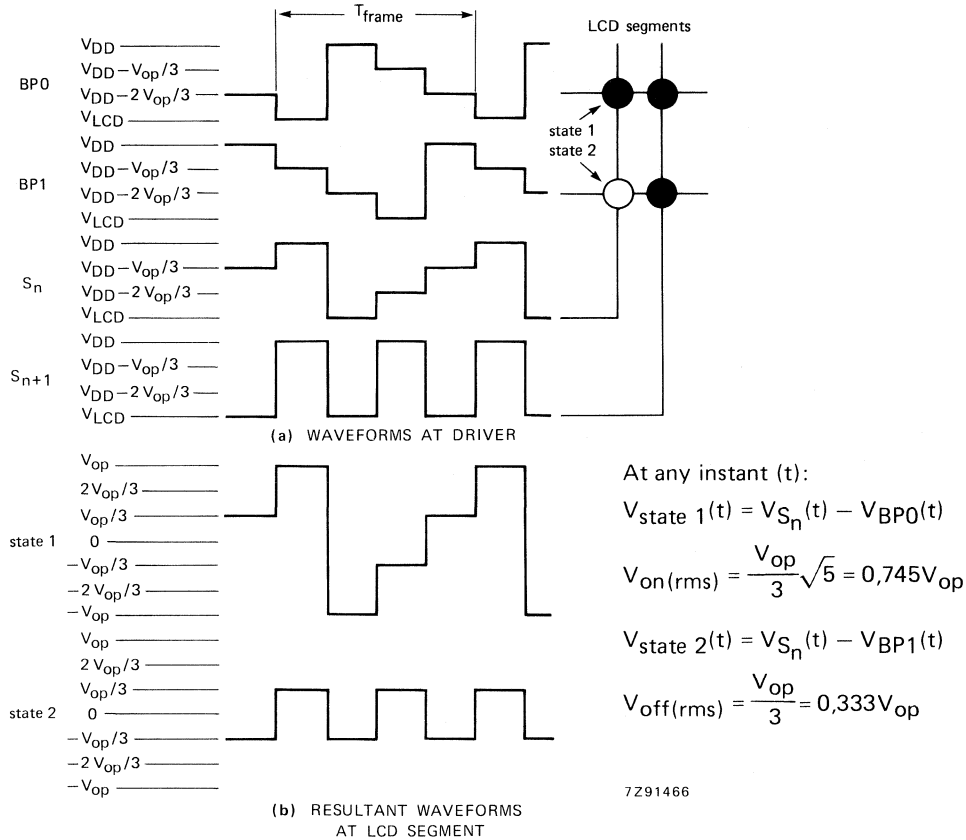


Fig. 6 Waveforms for 1 : 2 multiplex drive mode with 1/3 bias: $V_{op} = V_{DD} - V_{LCD}$.

The backplane and segment drive wavefront for the 1 : 3 multiplex drive mode (three LCD backplanes) and for the 1 : 4 multiplex drive mode (four LCD backplanes) are shown in Figs 7 and 8 respectively.

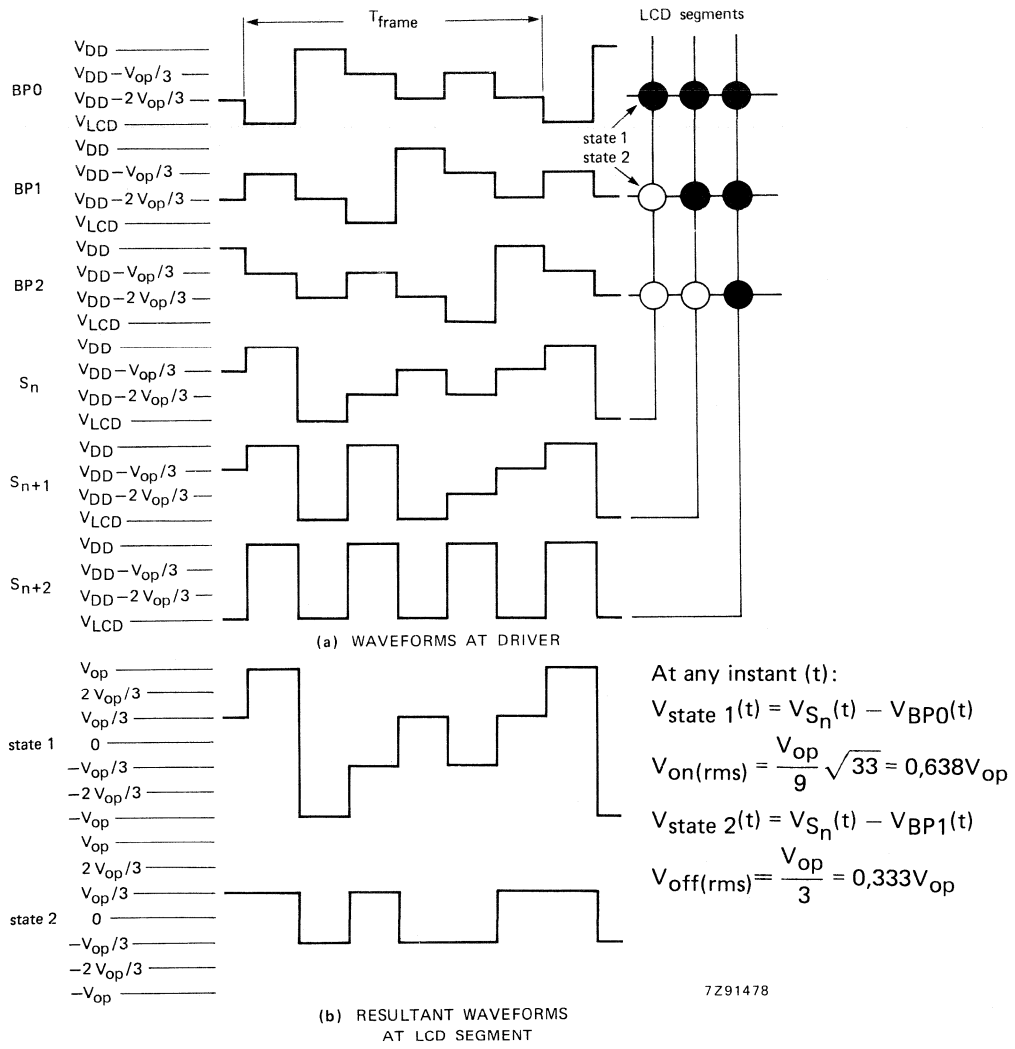


Fig. 7 Waveforms for 1 : 3 multiplex drive mode: $V_{op} = V_{DD} - V_{LCD}$.

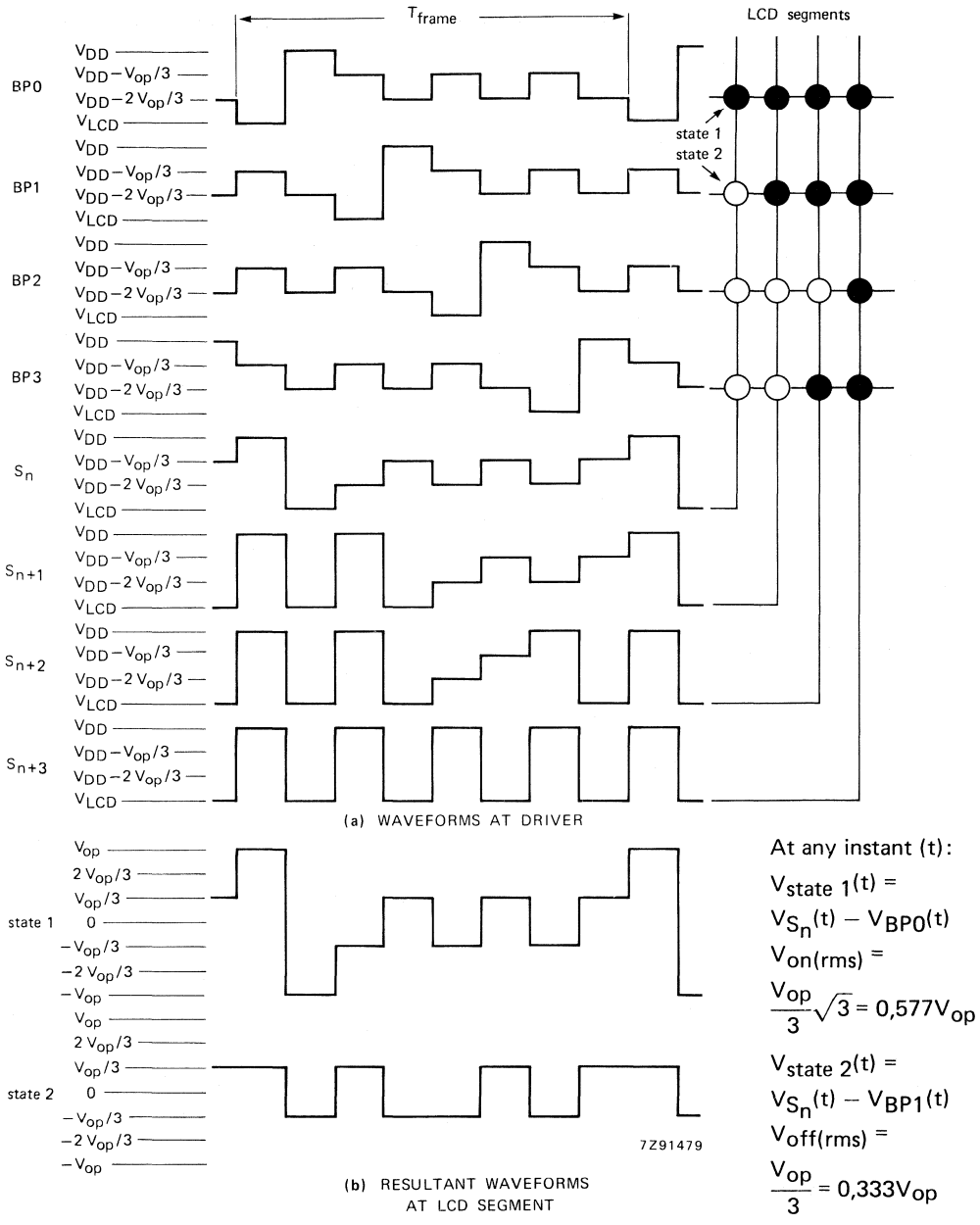


Fig. 8 Waveforms for 1 : 4 multiplex drive mode: $V_{op} = V_{DD} - V_{LCD}$.

Oscillator

The internal logic and the LCD drive signals of the PCF8566 or PCF8576 are timed either by the built-in oscillator or from an external clock.

The clock frequency (f_{CLK}) determines the LCD frame frequency and the maximum rate for data reception from the I²C bus. To allow I²C bus transmissions at their maximum data rate of 100 kHz, f_{CLK} should be chosen to be above 125 kHz.

A clock signal must always be supplied to the device; removing the clock may freeze the LCD in a DC state.

Internal clock

When the internal oscillator is used, OSC (pin 6) should be tied to V_{SS}. In this case, the output from CLK (pin 4) provides the clock signal for cascaded PCF8566s and PCF8576s in the system.

External clock

The condition for external clock is made by tying OSC (pin 6) to V_{DD}; CLK (pin 4) then becomes the external clock input.

Timing

The timing of the PCF8566 organizes the internal data flow of the device. This includes the transfer of display data from the display RAM to the display segment outputs. In cascaded applications, the synchronization signal $\overline{SYNC}$ maintains the correct timing relationship between the PCF8566s in the system. The timing also generates the LCD frame frequency which it derives as an integer multiple of the clock frequency (Table 3). The frame frequency is set by MODE SET commands when internal clock is used, or by the frequency applied to pin 4 when external clock is used.

Table 3 LCD frame frequencies

PCF8566 mode	f_{frame}	nominal f_{frame} (Hz)
normal mode	$f_{CLK}/2880$	64
power-saving mode	$f_{CLK}/480$	64

The ratio between the clock frequency and the LCD frame frequency depends on the mode in which the device is operating. In the power-saving mode the reduction ratio is six times smaller, this allows the clock frequency to be reduced by a factor of six. The reduced clock frequency results in a significant reduction in power dissipation. The lower clock frequency has the disadvantage of increasing the response time when large amounts of display data are transmitted on the I²C bus. When a device is unable to 'digest' a display data byte before the next one arrives, it holds the SCL line low until the first display data byte is stored. This slows down the transmission rate of the I²C bus but no data loss occurs.

Display latch

The display latch holds the display data while the corresponding multiplex signals are generated. There is a one-to-one relationship between the data in the display latch, the LCD segment outputs and one column of the display RAM.

Shift register

The shift register serves to transfer display information from the display RAM to the display latch while previous data are displayed.

Segment outputs

The LCD drive section includes 24 segment outputs S0 to S23 (pins 17 to 40) which should be connected directly to the LCD. The segment output signals are generated in accordance with the multiplexed backplane signals and with the data resident in the display latch. When less than 24 segment outputs are required the unused segment outputs should be left open-circuit.

Backplane outputs

The LCD drive section includes four backplane outputs BP0 to BP3 which should be connected directly to the LCD. The backplane output signals are generated in accordance with the selected LCD drive mode. If less than four backplane outputs are required the unused outputs can be left open. In the 1 : 3 multiplex drive mode BP3 carries the same signal as BP1, therefore these two adjacent outputs can be tied together to give enhanced drive capabilities. In the 1 : 2 multiplex drive mode BP0 and BP2, BP1 and BP3 respectively carry the same signals and may also be paired to increase the drive capabilities. In the static drive mode the same signal is carried by all four backplane outputs and they can be connected in parallel for very high drive requirements.

Display RAM

The display RAM is a static 24 x 4-bit RAM which stores LCD data. A logic 1 in the RAM bit-map indicates the 'on' state of the corresponding LCD segment; similarly, a logic 0 indicates the 'off' state. There is a one to one correspondence between the RAM addresses and the segment outputs, and between the individual bits of a RAM word and the backplane outputs. The first RAM column corresponds to the 24 segments operated with respect to backplane BP0 (Fig. 9). In multiplexed LCD applications the segment data of the second, third and fourth column of the display RAM are time-multiplexed with BP1, BP2 and BP3 respectively.

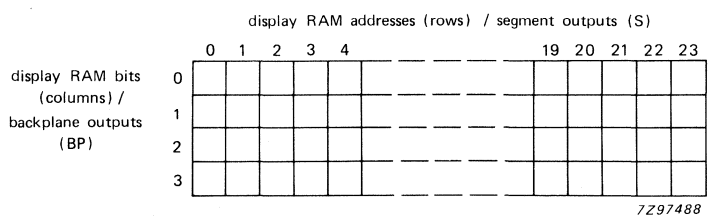


Fig. 9 Display RAM bit-map showing direct relationship between display RAM addresses and segment outputs, and between bits in a RAM word and backplane outputs.

When display data are transmitted to the PCF8566 the display bytes received are stored in the display RAM according to the selected LCD drive mode. To illustrate the filling order, an example of a 7-segment numeric display showing all drive modes is given in Fig. 10; the RAM filling organization depicted applies equally to other LCD types.

With reference to Fig. 10, in the static drive mode the eight transmitted data bits are placed in bit 0 of eight successive display RAM addresses. In the 1 : 2 multiplex drive mode the eight transmitted data bits are placed in bits 0 and 1 of four successive display RAM addresses. In the 1 : 3 multiplex drive mode these bits are placed in bits 0, 1 and 2 of three successive addresses, with bit 2 of the third address left unchanged. This last bit may, if necessary, be controlled by an additional transfer to this address but care should be taken to avoid overriding adjacent data because full bytes are always transmitted. In the 1 : 4 multiplex drive mode the eight transmitted data bits are placed in bits 0, 1, 2 and 3 of two successive display RAM addresses.

Data pointer

The addressing mechanism for the display RAM is realized using the data pointer. This allows the loading of an individual display data byte, or a series of display data bytes, into any location of the display RAM. The sequence commences with the initialization of the data pointer by the LOAD DATA POINTER command. Following this, an arriving data byte is stored starting at the display RAM address indicated by the data pointer thereby observing the filling order shown in Fig. 10. The data pointer is automatically incremented according to the LCD configuration chosen. That is, after each byte is stored, the contents of the data pointer are incremented by eight (static drive mode), by four (1 : 2 multiplex drive mode), by three (1 : 3 multiplex drive mode) or by two (1 : 4 multiplex drive mode).

Subaddress counter

The storage of display data is conditioned by the contents of the subaddress counter. Storage is allowed to take place only when the contents of the subaddress counter agree with the hardware subaddress applied to A0, A1 and A2 (pins 7, 8, and 9). A0, A1 and A2 should be tied to V_{SS} or V_{DD}. The subaddress counter value is defined by the DEVICE SELECT command. If the contents of the subaddress counter and the hardware subaddress do not agree then data storage is inhibited but the data pointer is incremented as if data storage had taken place. The subaddress counter is also incremented when the data pointer overflows.

The storage arrangements described lead to extremely efficient data loading in cascaded applications. When a series of display bytes are being sent to the display RAM, automatic wrap-over to the next PCF8566 occurs when the last RAM address is exceeded. Subaddressing across device boundaries is successful even if the change to the next device in the cascade occurs within a transmitted character.

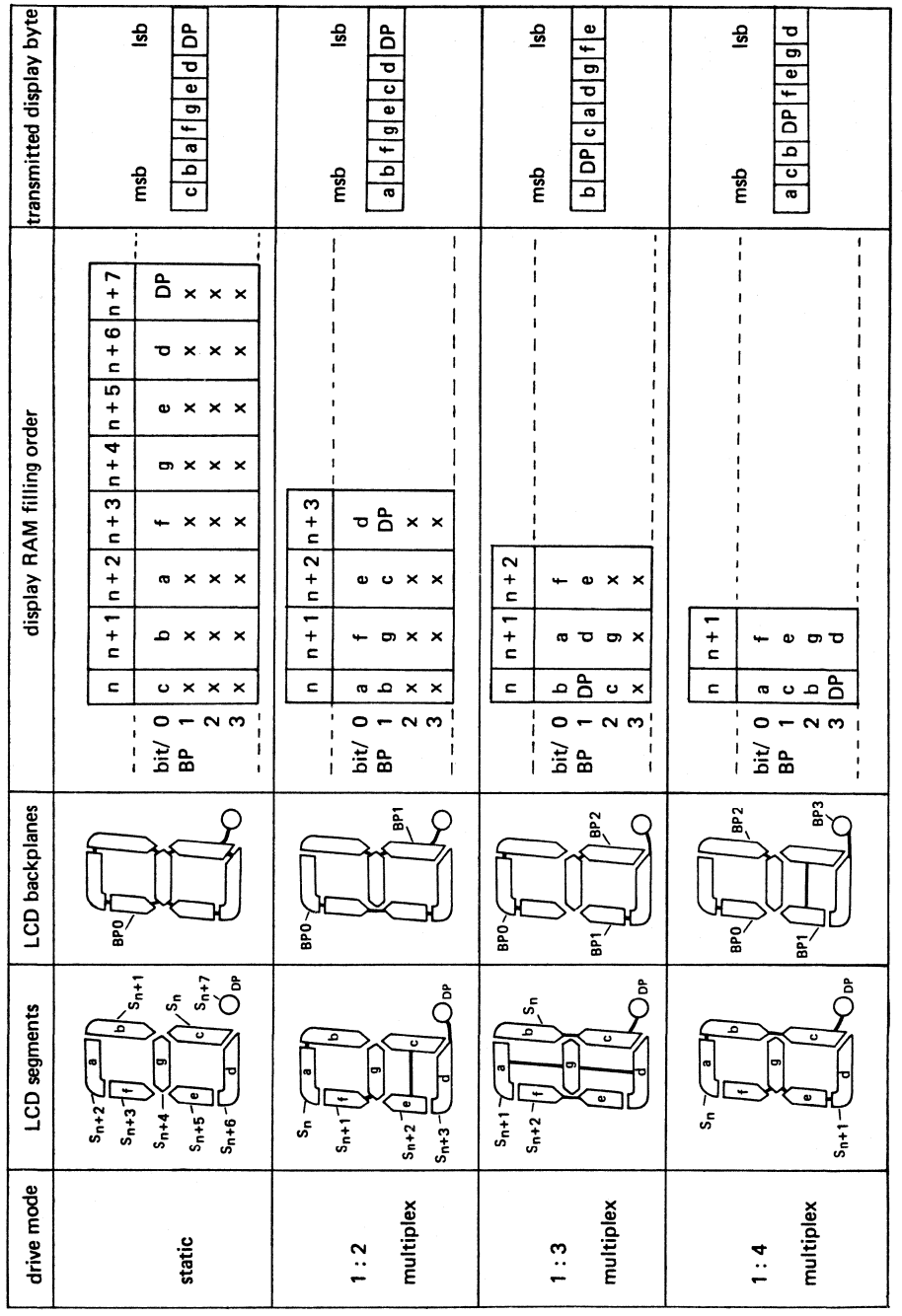


Fig. 10 Relationships between LCD layout, drive mode, display RAM filling order and display data transmitted over the I²C bus (x = data bit unchanged).

Output bank selector

This selects one of the four bits per display RAM address for transfer to the display latch. The actual bit chosen depends on the particular LCD drive mode in operation and on the instant in the multiplex sequence. In 1 : 4 multiplex, all RAM addresses of bit 0 are the first to be selected, these are followed by the contents of bit 1, bit 2 and then bit 3. Similarly in 1 : 3 multiplex, bits 0, 1 and 2 are selected sequentially. In 1 : 2 multiplex, bits 0 then 1 are selected and, in the static mode, bit 0 is selected.

The PCF8566 includes a RAM bank switching feature in the static and 1 : 2 multiplex drive modes. In the static drive mode, the BANK SELECT command may request the contents of bit 2 to be selected for display instead of bit 0 contents. In the 1 : 2 drive mode, the contents of bits 2 and 3 may be selected instead of bits 0 and 1. This gives the provision for preparing display information in an alternative bank and to be able to switch to it once it is assembled.

Input bank selector

The input bank selector loads display data into the display RAM according to the selected LCD drive configuration. Display data can be loaded in bit 2 in static drive mode or in bits 2 and 3 in 1 : 2 drive mode by using the BANK SELECT command. The input bank selector functions independently of the output bank selector.

Blinker

The display blinking capabilities of the PCF8566 are very versatile. The whole display can be blinked at frequencies selected by the BLINK command. The blinking frequencies are integer multiples of the clock frequency; the ratios between the clock and blinking frequencies depend on the mode in which the device is operating, as shown in Table 4.

An additional feature is for an arbitrary selection of LCD segments to be blinked. This applies to the static and 1 : 2 LCD drive modes and can be implemented without any communication overheads. By means of the output bank selector, the displayed RAM banks are exchanged with alternate RAM banks at the blinking frequency. This mode can also be specified by the BLINK command.

In the 1 : 3 and 1 : 4 multiplex modes, where no alternate RAM bank is available, groups of LCD segments can be blinked by selectively changing the display RAM data at fixed time intervals.

If the entire display is to be blinked at a frequency other than the nominal blinking frequency, this can be effectively performed by resetting and setting the display enable bit E at the required rate using the MODE SET command.

Table 4 Blinking frequencies

blinking mode	normal operating mode ratio	power-saving mode ratio	nominal blinking frequency f_{blink} (Hz)
off	–	–	blinking off
2 Hz	$f_{CLK}/92160$	$f_{CLK}/15360$	2
1 Hz	$f_{CLK}/184320$	$f_{CLK}/30720$	1
0,5 Hz	$f_{CLK}/368640$	$f_{CLK}/61440$	0,5

CHARACTERISTICS OF THE I²C BUS

The I²C bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

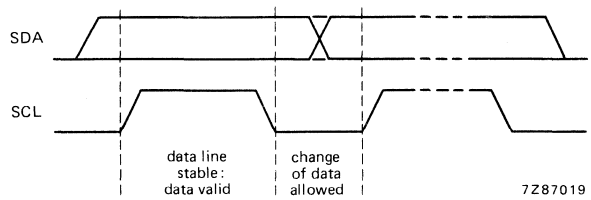


Fig. 11 Bit transfer.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

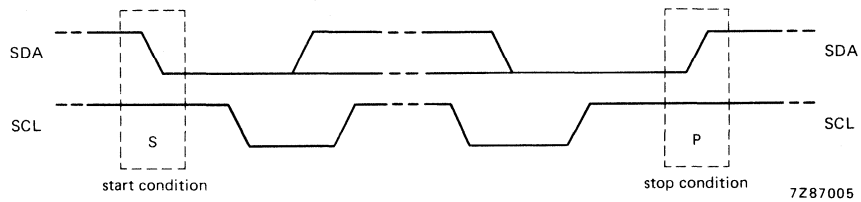


Fig. 12 Definition of start and stop conditions.

System configuration

A device generating a message is a "transmitter", a device receiving a message is a "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

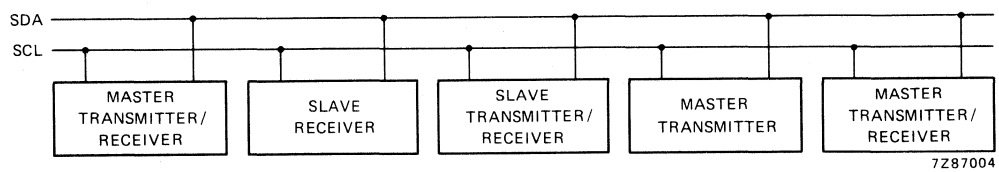


Fig. 13 System configuration.

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set up and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

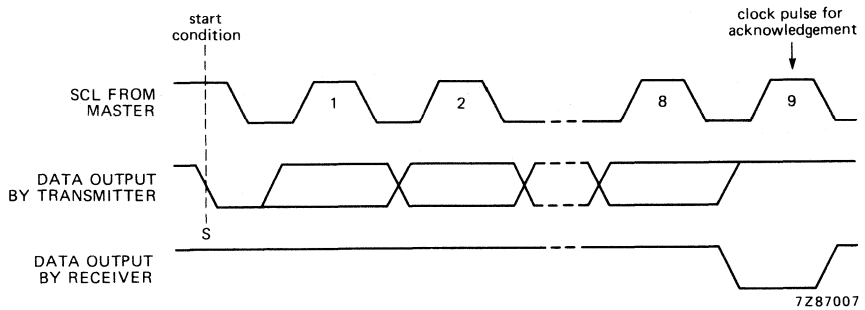


Fig. 14 Acknowledgement on the I²C bus.

PCF8566 I²C bus controller

The PCF8566 acts as an I²C slave receiver. It does not initiate I²C bus transfers or transmit data to an I²C master receiver. The only data output from the PCF8566 are the acknowledge signals of the selected devices. Device selection depends on the I²C bus slave address, on the transferred command data and on the hardware subaddress.

In single device applications, the hardware subaddress inputs A0, A1 and A2 are normally left open-circuit or tied to V_{SS} which defines the hardware subaddress 0. In multiple device applications A0, A1 and A2 are left open-circuit or tied to V_{SS} or V_{DD} according to a binary coding scheme such that no two devices with a common I²C slave address have the same hardware subaddress.

In the power-saving mode it is possible that the PCF8566 is not able to keep up with the highest transmission rates when large amounts of display data are transmitted. If this situation occurs, the PCF8566 forces the SCL line LOW until its internal operations are completed. This is known as the 'clock synchronization feature' of the I²C bus and serves to slow down fast transmitters. Data loss does not occur.

Input filters

To enhance noise immunity in electrically adverse environments, RC low-pass filters are provided on the SDA and SCL lines.

I²C bus protocol

Two I²C bus slave addresses (0111110 and 0111111) are reserved for PCF8566. The least-significant bit of the slave address that a PCF8566 will respond to is defined by the level tied at its input SA0 (pin 10). Therefore, two types of PCF8566 can be distinguished on the same I²C bus which allows:

(a) up to 16 PCF8566s on the same I²C bus for very large LCD applications;

(b) the use of two types of LCD multiplex on the same I²C bus.

The I²C bus protocol is shown in Fig. 15. The sequence is initiated with a start condition (S) from the I²C bus master which is followed by one of the two PCF8566 slave addresses available. All PCF8566s with the corresponding SA0 level acknowledge in parallel the slave address but all PCF8566s with the alternative SA0 level ignore the whole I²C bus transfer. After acknowledgement, one or more command bytes (m) follow which define the status of the addressed PCF8566s. The last command byte is tagged with a cleared most-significant bit, the continuation bit C. The command bytes are also acknowledged by all addressed PCF8566s on the bus.

After the last command byte, a series of display data bytes (n) may follow. These display data bytes are stored in the display RAM at the address specified by the data pointer and the subaddress counter. Both data pointer and subaddress counter are automatically updated and the data are directed to the intended PCF8566 device. The acknowledgement after each byte is made only by the (A0, A1, A2) addressed PCF8566. After the last display byte, the I²C bus master issues a stop condition (P).

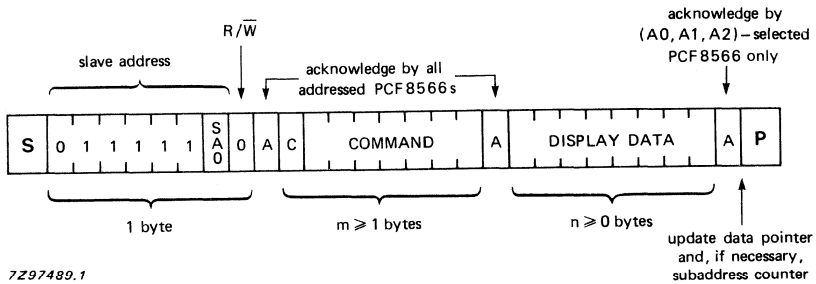


Fig. 15 I²C bus protocol.

Command decoder

The command decoder identifies command bytes that arrive on the I²C bus. All available commands carry a continuation bit C in their most-significant bit position (Fig. 16). When this bit is set, it indicates that the next byte of the transfer to arrive will also represent a command. If the bit is reset, it indicates the last command byte of the transfer. Further bytes will be regarded as display data.

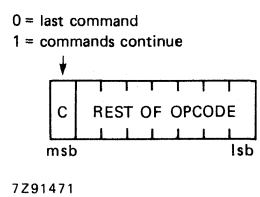


Fig. 16 General format of command byte.

The five commands available to the PCF8566 are defined in Table 5.

Command decoder (continued)

Table 5 Definition of PCF8566 commands

command/opcode	options	description
MODE SET C 1 0 LP E B M1 M0	LCD drive mode: bits M1 M0 static (1 BP): 0 1 1 : 2 MUX (2 BP): 1 0 1 : 3 MUX (3 BP): 1 1 1 : 4 MUX (4 BP): 0 0 LCD bias: bit B 1/3 bias: 0 1/2 bias: 1 display status: bit E disabled (blank): 0 enabled: 1 mode: bit LP normal mode: 0 power-saving mode: 1	Defines LCD drive mode Defines LCD bias configuration Defines display status The possibility to disable the display allows implementation of blinking under external control Defines power dissipation mode
LOAD DATA POINTER C 0 0 P4 P3 P2 P1 P0	bits P4 P3 P2 P1 P0 5-bit binary value of 0 to 23	Five bits of immediate data, bits P4 to P0, are transferred to the data pointer to define one of twenty-four display RAM addresses
DEVICE SELECT C 1 1 0 0 A2 A1 A0	bits A0 A1 A2 3-bit binary value of 0 to 7	Three bits of immediate data, bits A0 to A2, are transferred to the subaddress counter to define one of eight hardware subaddresses

<table>
<tr><th>command/opcode</th><th>options</th><th>description</th></tr>
<tr><td>BANK SELECT

C | 1 1 1 1 1 0 | I | O</td><td>
<table>
<tr><th>static</th><th>1 : 2 MUX</th><th>bit I</th></tr>
<tr><td>RAM bit 0
RAM bit 2</td><td>RAM bits 0, 1
RAM bits 2, 3</td><td>0
1</td></tr>
</table>
<table>
<tr><th>static</th><th>1 : 2 MUX</th><th>bit O</th></tr>
<tr><td>RAM bit 0
RAM bit 2</td><td>RAM bits 0, 1
RAM bits 2, 3</td><td>0
1</td></tr>
</table>
</td><td>Defines input bank selection (storage of arriving display data)

Defines output bank selection (retrieval of LCD display data)

The BANK SELECT command has no effect in 1 : 3 and 1 : 4 multiplex drive modes</td></tr>
<tr><td>BLINK

C | 1 1 1 0 | A | BF1 BF0</td><td>
<table>
<tr><th>blink frequency</th><th>bits BF1</th><th>BF0</th></tr>
<tr><td>off</td><td>0</td><td>0</td></tr>
<tr><td>2 Hz</td><td>0</td><td>1</td></tr>
<tr><td>1 Hz</td><td>1</td><td>0</td></tr>
<tr><td>0,5 Hz</td><td>1</td><td>1</td></tr>
</table>
<table>
<tr><th>blink mode</th><th>bit A</th></tr>
<tr><td>normal blinking
alternation blinking</td><td>0
1</td></tr>
</table>
</td><td>Defines the blinking frequency

Selects the blinking mode; normal operation with frequency set by bits BF1, BF0, or blinking by alternation of display RAM banks. Alternation blinking does not apply in 1 : 3 and 1 : 4 multiplex drive modes</td></tr>
</table>

Display controller

The display controller executes the commands identified by the command decoder. It contains the status registers of the PCF8566 and coordinates their effects. The controller is also responsible for loading display data into the display RAM as required by the filling order.

Cascaded operation

In large display configurations, up to 16 PCF8566s can be distinguished on the same I²C bus by using the 3-bit hardware subaddress (A0, A1, A2) and the programmable I²C slave address (SA0). It is also possible to cascade up to 16 PCF8566s. When cascaded, several PCF8566s are synchronized so that they can share the backplane signals from one of the devices in the cascade. Such an arrangement is cost-effective in large LCD applications since the backplane outputs of only one device need to be through-plated to the backplane electrodes of the display. The other PCF8566s of the cascade contribute additional segment outputs but their backplane outputs are left open-circuit (Fig. 17).

The $\overline{SYNC}$ line is provided to maintain the correct synchronization between all cascaded PCF8566s. This synchronization is guaranteed after the power-on reset. The only time that $\overline{SYNC}$ is likely to be needed is if synchronization is accidently lost (e.g. by noise in adverse electrical environments; or by the definition of a multiplex mode when PCF8566s with differing SA0 levels are cascaded). $\overline{SYNC}$ is organized as an input/output pin; the output section being realized as an open-drain driver with an internal pull-up resistor. A PCF8566 asserts the $\overline{SYNC}$ line at the onset of its last active backplane signal and monitors the $\overline{SYNC}$ line at all other times. Should synchronization in the cascade be lost, it will be restored by the first PCF8566 to assert $\overline{SYNC}$. The timing relationships between the backplane waveforms and the $\overline{SYNC}$ signal for the various drive modes of the PCF8576 are shown in Fig. 18. The waveforms are identical with the parent device PCF8576. Casadability between PCF8566s and PCF8576s is possible, giving cost effective LCD applications.

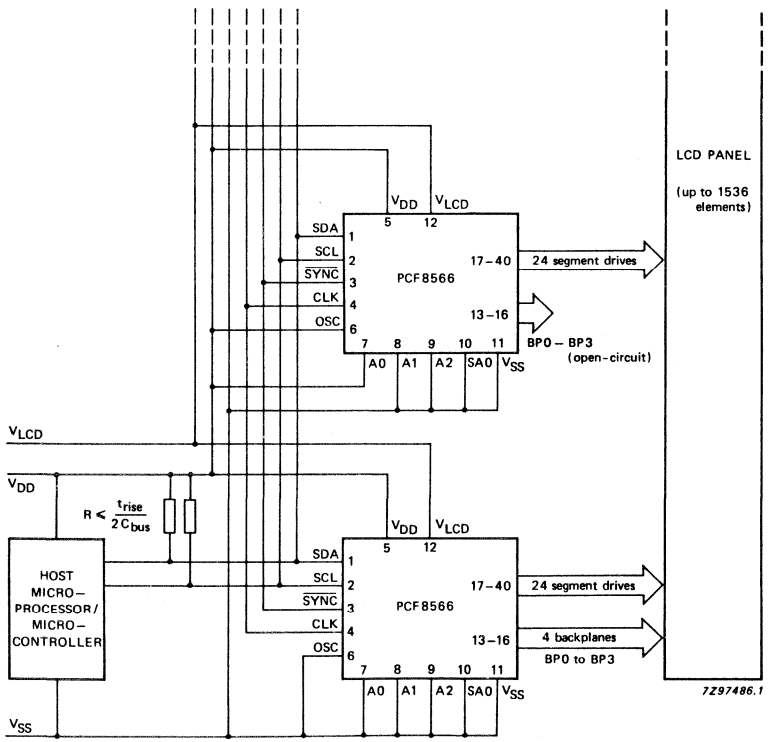


Fig. 17 Cascaded PCF8566 configuration.

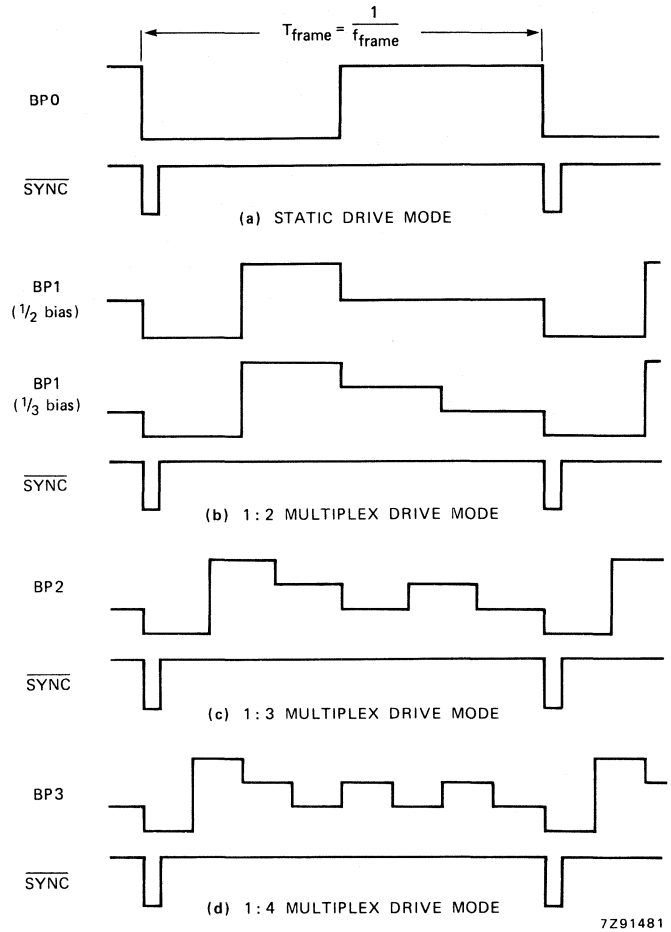


Fig. 18 Synchronization of the cascade for the various PCF8566 drive modes.

For single plane wiring of PCF8566s, see section "APPLICATION INFORMATION".

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range; see note	V_{DD}		−0,5 to + 7 V
LCD supply voltage range	V_{LCD}		V_{DD} −7 to V_{DD} V
Input voltage range (SCL; SDA; A0 to A2; OSC; CLK; $\overline{SYNC}$; SA0)	V_I		V_{SS} −0,5 to V_{DD} + 0,5 V
Output voltage range (S0 to S23; BP0 to BP3)	V_O		V_{LCD} −0,5 to V_{DD} + 0,5 V
DC input current	$\pm I_I$	max.	20 mA
DC output current	$\pm I_O$	max.	25 mA
V_{DD}, V_{SS} or V_{LCD} current	$\pm I_{DD}$, $\pm I_{SS}$, $\pm I_{LCD}$	max.	50 mA
Power dissipation per package	P_{tot}	max.	400 mW
Power dissipation per output	P_O	max.	100 mW
Storage temperature range	T_{stg}		−65 to + 150 °C

Note

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is advised to take handling precautions appropriate to handling MOS devices (see 'Handling MOS devices').

DC CHARACTERISTICS

V_{SS} = 0 V; V_{DD} = 2,5 to 6 V; V_{LCD} = V_{DD} −2,5 to V_{DD} −6 V;

T_{amb} = −40 to +85 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Operating supply voltage	V_{DD}	2,5	–	6	V
LCD supply voltage	V_{LCD}	V_{DD} −6	–	V_{DD} −2,5	V
Operating supply current (normal mode) at f_{CLK} = 200 kHz (note 1)	I_{DD}	–	30	90	μA
Power-saving mode supply current at V_{DD} = 3,5 V; V_{LCD} = 0 V; f_{CLK} = 35 kHz; A0, A1 and A2 tied to V_{SS} (note 1)	I_{LP}	–	15	40	μA

parameter	symbol	min.	typ.	max.	unit
Logic					
Input voltage LOW	V_{IL}	V_{SS}	–	$0,3\ V_{DD}$	V
Input voltage HIGH	V_{IH}	$0,7\ V_{DD}$	–	V_{DD}	V
Output voltage LOW at I_O = 0 mA	V_{OL}	–	–	0,05	V
Output voltage HIGH at I_O = 0 mA	V_{OH}	V_{DD} −0,05	–	–	V
Output current LOW (CLK, $\overline{SYNC}$) at V_{OL} = 1,0 V; V_{DD} = 5 V	I_{OL1}	1	–	–	mA
Output current HIGH (CLK) at V_{OH} = 4,0 V; V_{DD} = 5 V	I_{OH}	–	–	−1	mA
Output current LOW (SDA; SCL) at V_{OL} = 0,4 V; V_{DD} = 5 V	I_{OL2}	3	–	–	mA
Leakage current (SA0, CLK, OSC, A0, A1, A2, SCL, SDA) at $V_I = V_{SS}$ or V_{DD}	$\pm I_L$	–	–	1	μA
Pull-down current (A0; A1; A2; OSC) at V_I = 1 V and V_{DD} = 5 V	I_{pd}	15	50	150	μA
Pull-up resistor ($\overline{SYNC}$)	R_{SYNC}	15	25	60	kΩ
Power-on reset level (note 2)	V_{REF}	–	1,3	2,0	V
Tolerable spike width on bus	t_{sw}	–	–	100	ns
Input capacitance (note 3)	C_I	–	–	7	pF
LCD outputs					
D.C. voltage component (BP0 to BP3) at C_{BP} = 35 nF	$\pm V_{BP}$	–	20	–	mV
D.C. voltage component (S0 to S23) at C_S = 5 nF	$\pm V_S$	–	20	–	mV
Output impedance (BP0 to BP3) at $V_{LCD} = V_{DD}$ −5 V (note 4)	R_{BP}	–	1	5	kΩ
Output impedance (S0 to S23) at $V_{LCD} = V_{DD}$ −5 V (note 4)	R_S	–	3	7,0	kΩ

AC CHARACTERISTICS (note 5)

V_{SS} = 0 V; V_{DD} = 2,5 to 6 V; V_{LCD} = V_{DD} −2,5 to V_{DD} −6 V;
T_{amb} = −40 to +85 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Oscillator frequency (normal mode) at V_{DD} = 5 V (note 6)	f_{CLK}	125	200	315	kHz
Oscillator frequency (power-saving mode) at V_{DD} = 3,5 V	f_{CLKLP}	21	31	48	kHz
CLK HIGH time	t_{CLKH}	1	–	–	μs
CLK LOW time	t_{CLKL}	1	–	–	μs
$\overline{SYNC}$ propagation delay	t_{PSYNC}	–	–	400	ns
$\overline{SYNC}$ LOW time	t_{SYNCL}	1	–	–	μs
Driver delays with test loads at V_{LCD} = V_{DD} −5 V	t_{PLCD}	–	–	30	μs
I²C bus					
Bus free time	t_{BUF}	4,7	–	–	μs
Start condition hold time	$t_{HD;STA}$	4	–	–	μs
SCL LOW time	t_{LOW}	4,7	–	–	μs
SCL HIGH time	t_{HIGH}	4	–	–	μs
Start condition set-up time (repeated start code only)	$t_{SU;STA}$	4,7	–	–	μs
Data hold time	$t_{HD;DAT}$	0	–	–	μs
Data set-up time	$t_{SU;DAT}$	250	–	–	ns
Rise time	t_r	–	–	1	μs
Fall time	t_f	–	–	300	ns
Stop condition set-up time	$t_{SU;STO}$	4,7	–	–	μs

Notes to characteristics

1. Outputs open; inputs at V_{SS} or V_{DD}; external clock with 50% duty factor; I²C bus inactive.
2. Resets all logic when $V_{DD} < V_{REF}$.
3. Periodically sampled, not 100% tested.
4. Outputs measured one at a time.
5. All timing values referred to V_{IH} and V_{IL} levels with an input voltage swing of V_{SS} to V_{DD}.
6. At $f_{CLK} < 125$ kHz, I²C bus maximum transmission speed is derated.

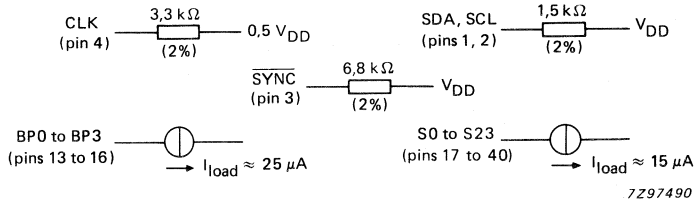


Fig. 19 Test loads.

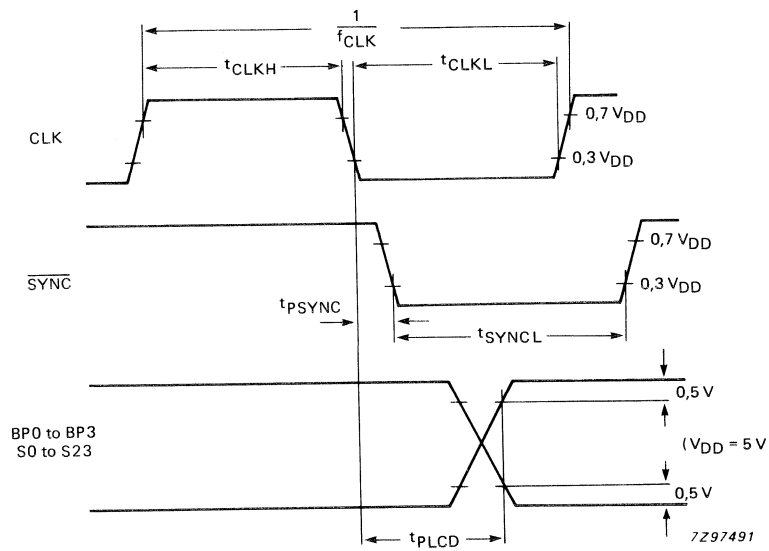


Fig. 20 Driver timing waveforms.

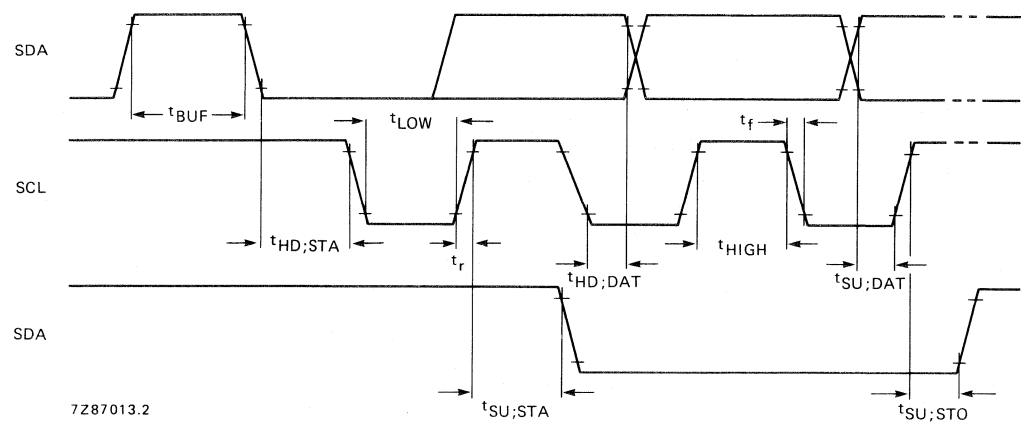
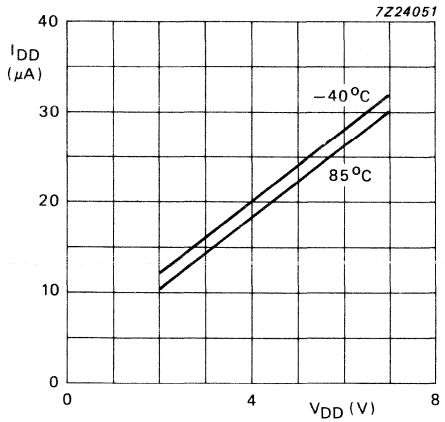
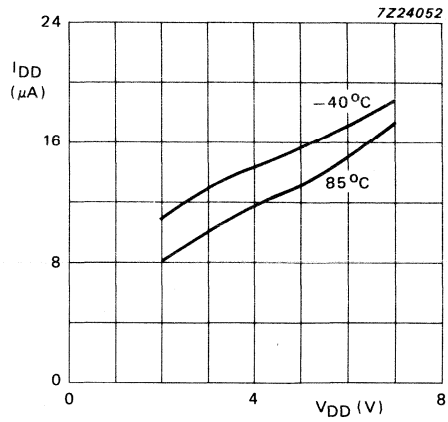


Fig. 21 I²C bus timing waveforms.

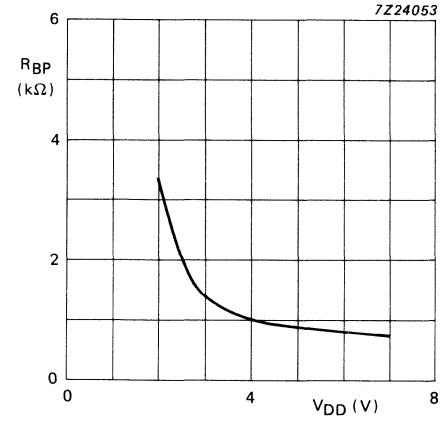


(a) Normal mode; V_{LCD} = 0 V; external clock = 200 kHz.

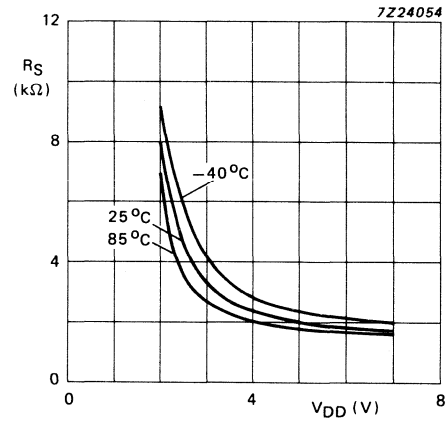


(b) Low power mode; V_{LCD} = 0 V; external clock = 35 kHz.

Fig. 22 Typical supply current characteristics.



(a) Backplane output impedance BP0 to BP3 (R_{BP}); V_{DD} = 5 V; T_{amb} = −40 to + 85 °C.



(b) Segment output impedance S0 to S23 (R_S); V_{DD} = 5 V.

Fig. 23 Typical characteristics of LCD outputs.

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

APPLICATION INFORMATION

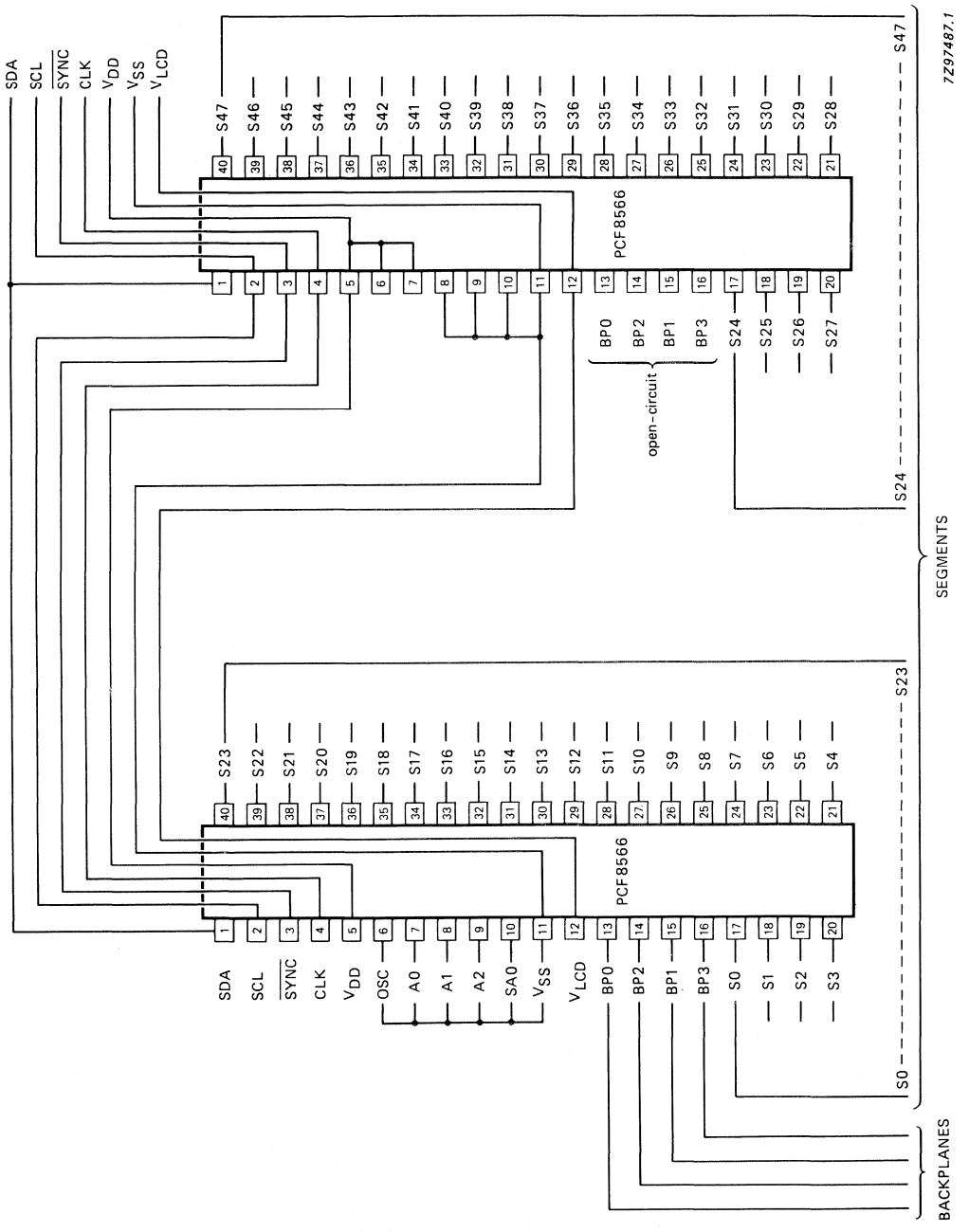


Fig. 24 Single plane wiring of packaged PCF8566s.

LCD row driver for dot matrix displays — PCF8568

FEATURES

- Single chip LCD row driver with 16 outputs
- Low power consumption
- Selectable multiplex rate 1:8, 1:16, 1:24, 1:32
- Cascadable to 1:24 or 1:32 multiplex rates
- Internally generated intermediate LCD bias voltages
- LCD column bias voltages available at pins VO3 and VO4
- Minimizes display system power requirements
- On-chip oscillator, requires only one external resistor
- Power-on reset blanks display
- Logic voltage range 2.5 V to 6.0 V
- Maximum LCD supply voltage 9.0 V
- I²C-bus interface
- TTL/CMOS compatible
- Compatible with most microcontrollers
- Optimized pinning for single plane wiring
- Available in 28-lead plastic DIL or space saving mini-pack
- Compatible with chip-on-glass technology.

APPLICATIONS

- Automotive information systems
- Telecommunication systems
- Point-of-sale terminals
- General instrumentation
- Consumer products.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage range	+2.5	-	+6.0	V
V_{LCD}	LCD supply voltage range voltage	V_{DD} −9	-	V_{DD} −3.5	V
I_{DD2}	supply current with internal clock (R_{OSC} = 330 kΩ)	-	67	150	µA
T_{amb}	operating ambient temperature range	−40	-	+85	°C

ORDERING AND PACKAGE INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
PCF8568P	28	DIL	plastic	SOT117
PCF8568T	28	SO28	plastic	SOT136A
PCF8568U/7	(28 pads)	die: bumped chip on tape	-	-

GENERAL DESCRIPTION

The PCF8568 is a low power LCD row driver, designed to drive dot matrix graphic displays with multiplex rates of 1:8 or 1:16. The device has 16 row outputs. Two devices may be cascaded to drive displays with multiplex rates of 1:24 or 1:32. The PCF8568 is optimised for use with the PCF8569 and PCF8579 LCD dot matrix column drivers. Intermediate LCD bias voltages are internally generated. LCD column bias voltages are available at pins VO3 and VO4 for connection to the column drivers. The PCF8568 is compatible with most microcontrollers and communicates via a two- line bidirectional bus (I²C).

LCD row driver for dot matrix displays PCF8568

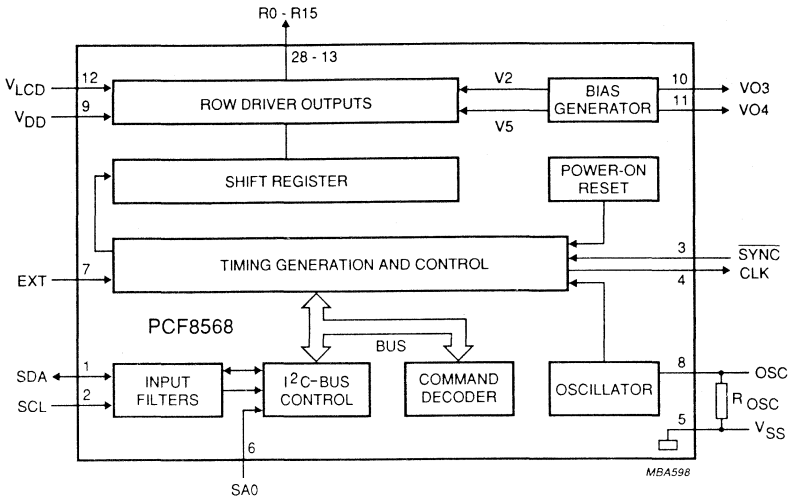


Fig.1 Block diagram.

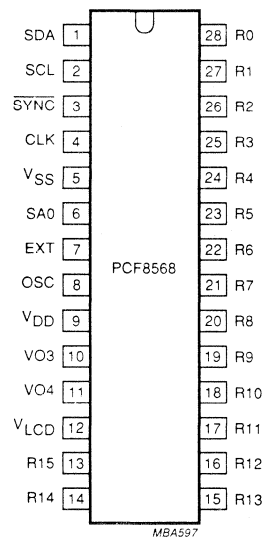


Fig.2 Pinning diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
SDA	1	I²C-bus serial data line
SCL	2	I²C-bus serial clock line
$\overline{\text{SYNC}}$	3	cascade synchronization input/output
CLK	4	clock output
V_{SS}	5	ground (logic)
SA0	6	I²C-bus slave address input (bit 0)
EXT	7	external clock select pin
OSC	8	oscillator or external clock input pin
V_{DD}	9	positive supply voltage
VO3	10	LCD bias voltage output (V3)
VO4	11	LCD bias voltage output (V4)
V_{LCD}	12	LCD supply voltage
R15 to R0	13 to 28	LCD row driver outputs

FUNCTIONAL DESCRIPTION

A single PCF8568 functions as a row driver with up to 16 row outputs and provides the clock and synchronization signals for the PCF8569 and PCF8579 column drivers.

System types and cascaded operation

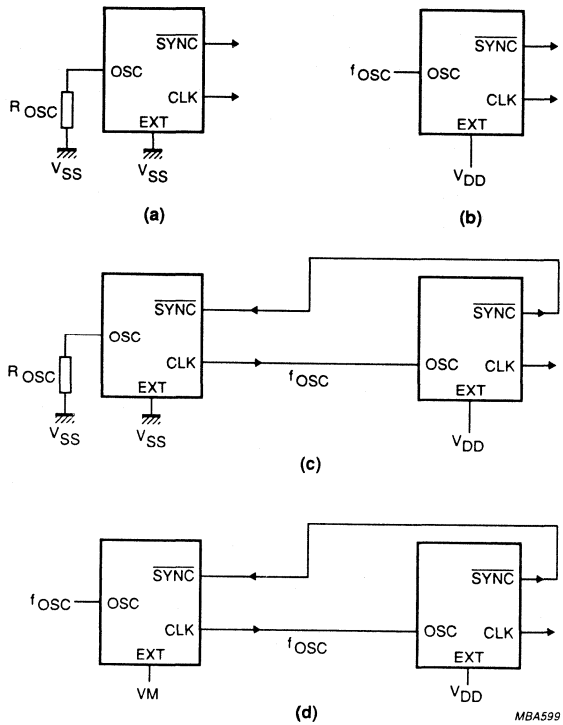
The PCF8568 may be configured in one of four different system types as shown in Fig. 3. The device operating mode is defined by the EXT and multiplex rate. EXT is programmed to one of three states by application of a DC level V_{DD}, V_M or V_{SS} to pin 7 (see DC characteristics).

A single PCF8568 may be used to drive up to 16 rows with a 1:8 or 1:16 multiplex rate. Two PCF8568s may be cascaded in order to drive up to 32 rows with a multiplex rate of 1:24 or 1:32. The device driving the last 16 rows provides the synchronization signal for the first device and the column drivers. LCD column bias voltages are available for connection from both devices at pins VO3 and VO4. Pins VO3 and VO4 from the first device must NOT be connected to pins VO3 and VO4 of the second device.

The system type is undefined before the first SET MODE command is sent. In order to avoid system conflicts during this time, the multiplex rate is set to 1:32, the CLK output oscillates with a frequency of 12 kHz, the $\overline{SYNC}$ pin outputs a high (V_{DD}) level and the row outputs toggle at a frequency of 12 kHz. This also ensures that the LCD remains blank at power-on for all system types. This information is summarized in Table 1.

Table 1 Cascade control.
Typically: R_{OSC} = 330 kΩ; f_{OSC} = 12 kHz; f_{CLK1} = 2 kHz; f_{CLK2} = 1.5 kHz.

EXT	DEVICE MODE	MULTIPLEX RATE	OSC	CLK OUTPUT	$\overline{SYNC}$
SYSTEM STATUS: after first SET-MODE					
V_{SS}	single	1:8; 1:16	connect R_{OSC}	f_{CLK1}	output
V_{DD}	single	1:8; 1:16	input f_{OSC}	f_{CLK1}	output
V_{SS}	first	1:24; 1:32	connect R_{OSC}	f_{OSC}	input
V_M	first	1:24; 1:32	input f_{OSC}	f_{OSC}	input
V_{DD}	second	1:24; 1;32	input f_{OSC}	$f_{CLK2/1}$	output
SYSTEM STATUS: before first SET-MODE					
V_{SS}	undefined	1:32	connect R_{OSC}	f_{OSC}	output V_{DD}
V_M	undefined	1:32	input f_{OSC}	f_{OSC}	output V_{DD}
V_{DD}	undefined	1:32	input f_{OSC}	f_{OSC}	output V_{DD}



(a) single device, internal clock.
(b) single device, external clock.
(c) cascaded system, internal clock.
(d) cascaded system, external clock.

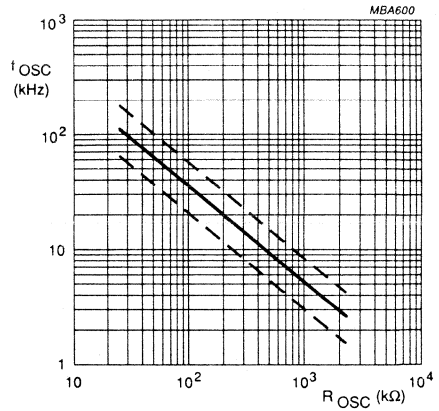
Fig.3 System types.

Oscillator

Timing signals are derived from an on-chip oscillator, whose frequency is determined by the value of the resistor connected between OSC and V_{SS}.

Internal clock

The clock signal for the system may be generated by the internal oscillator and prescaler. The frequency is determined by the value of the resistor R_{OSC}, see Fig. 4. For normal use a value of 330 kΩ is recommended. When a single PCF8568 is used, the clock signal for the column drivers is output at CLK and has a frequency one-sixth (multiplex rate 1:8, 1:16 and 1:32) or one-eighth (multiplex rate 1:24) of the oscillator frequency. In a cascaded system, the CLK output from the second device is fed to the column drivers.



Note: to avoid capacitive coupling, which could adversely affect oscillator stability, R_{OSC} should be placed as closely as possible to the OSC pin. If this proves to be a problem, a filtering capacitor may be connected in parallel to R_{OSC}.

Fig.4 Oscillator frequency as a function of R_{OSC}.

External clock

If an external clock is used, EXT must be connected to either V_{DD}, or V_M and the external clock signal to OSC. The external clock should have a 50% duty cycle in order to guarantee a DC free LCD waveform between power-on and the first set mode command. Table 2 summarizes the nominal CLK and $\overline{SYNC}$ frequencies.

Multiplexed LCD bias generation

The bias levels required to produce maximum contrast depend on the multiplex rate and the LCD threshold voltage (V_{th}). V_{th} is typically defined as the RMS voltage at which the LCD exhibits 10% contrast.

The PCF8568 generates the intermediate voltage bias levels internally using the V_{DD} and V_{LCD} supplies. For multiplex rates of 1:16, 1:24 and 1:32 a total of six bias levels are used including V_{DD}, V2, V3, V4 and V_{LCD}. Five bias levels are used for the 1:8 multiplex rate (V3 is set equal to V4 with a value half of the total operating voltage V_{OP}).

Buffered bias voltages are available for connection to the column drivers at pins VO3 and VO4. Table 3 shows the generated voltage bias levels for the PCF8568 as a function of V_{OP} ($V_{OP} = V_{DD}-V_{LCD}$), together with the discrimination ratios (D) for the different multiplex rates. A practical value for V_{OP} is obtained by equating $V_{OFF(RMS)}$ with V_{th}.

Table 2 Signal frequencies required for nominal 64 Hz frame frequency.
A clock signal must always be present otherwise the LCD may be frozen in a DC state.

OSCILLATOR FREQUENCY f_{osc} (Hz) (R_{osc} = 330 kΩ)	FRAME FREQUENCY $f_{\overline{SYNC}}$ (Hz)	MULTIPLEX RATE	DIVISION RATIO	CLOCK FREQUENCY f_{CLK} (Hz)
12288	64	1:8; 1:16; 1:32	6	2048
12288	64	1:24	8	1536

Table 3 LCD bias generation

PARAMETER	MULTIPLEX RATE LEVEL 5	MULTIPLEX RATE LEVEL 6		
mux rate	1:8	1:16	1:24	1:32
$V2/V_{OP}$	0.750	0.800	0.830	0.850
$V3/V_{OP}$	0.500	0.600	0.661	0.700
$V4/V_{OP}$	0.500	0.400	0.339	0.300
$V5/V_{OP}$	0.250	0.200	0.170	0.150
$V_{OFF(RMS)}/V_{OP}$	0.293	0.245	0.214	0.193
$V_{ON(RMS)}/V_{OP}$	0.424	0.316	0.263	0.230
$D = V_{ON(RMS)}/V_{OFF(RMS)}$	1.446	1.291	1.230	1.196
V_{OP}/V_{th}	3.41	4.08	4.68	5.19

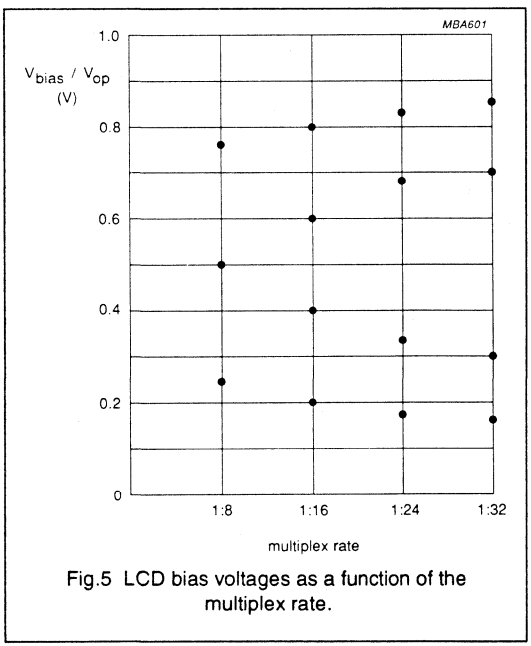


Fig.5 LCD bias voltages as a function of the multiplex rate.

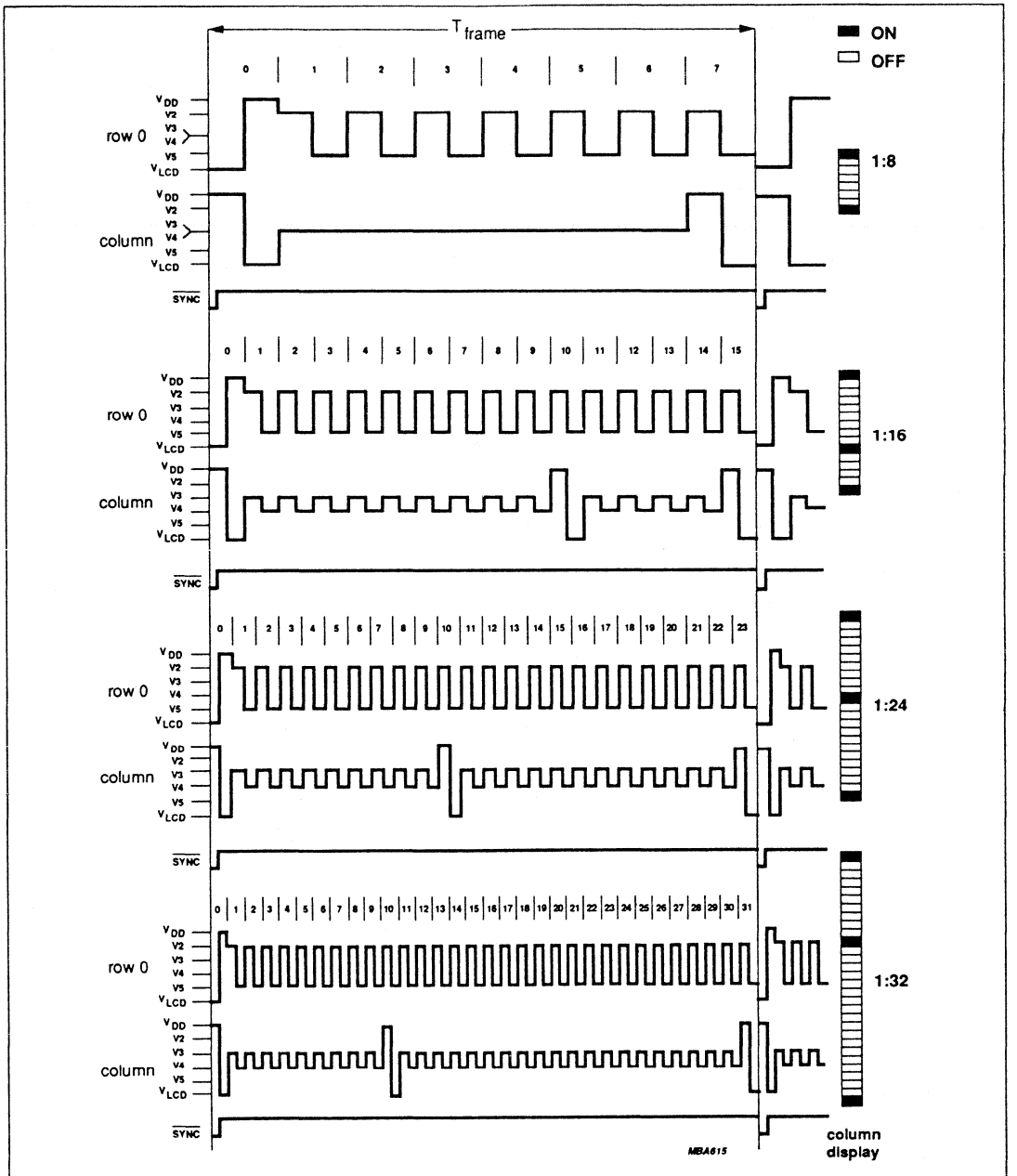


Fig.6 LCD row/column waveforms.

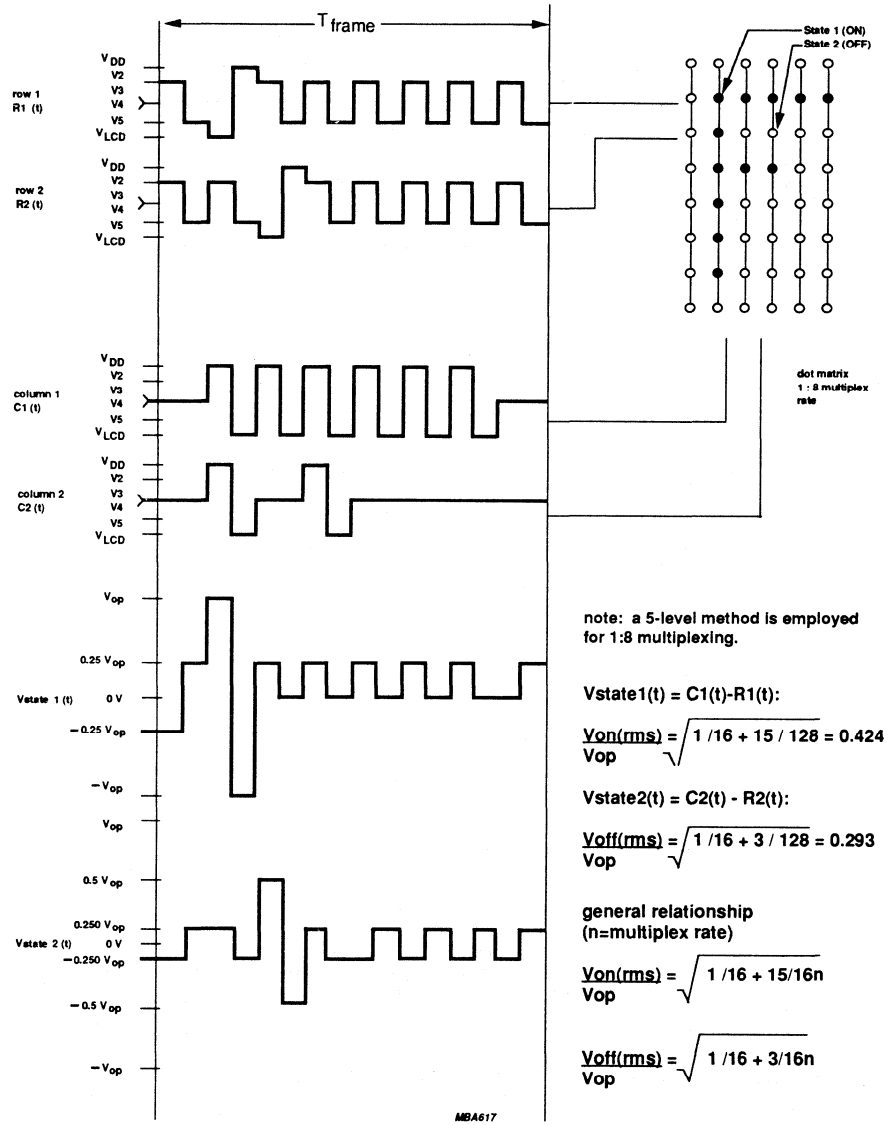


Fig.7 LCD drive mode waveforms for 1:8 multiplex.

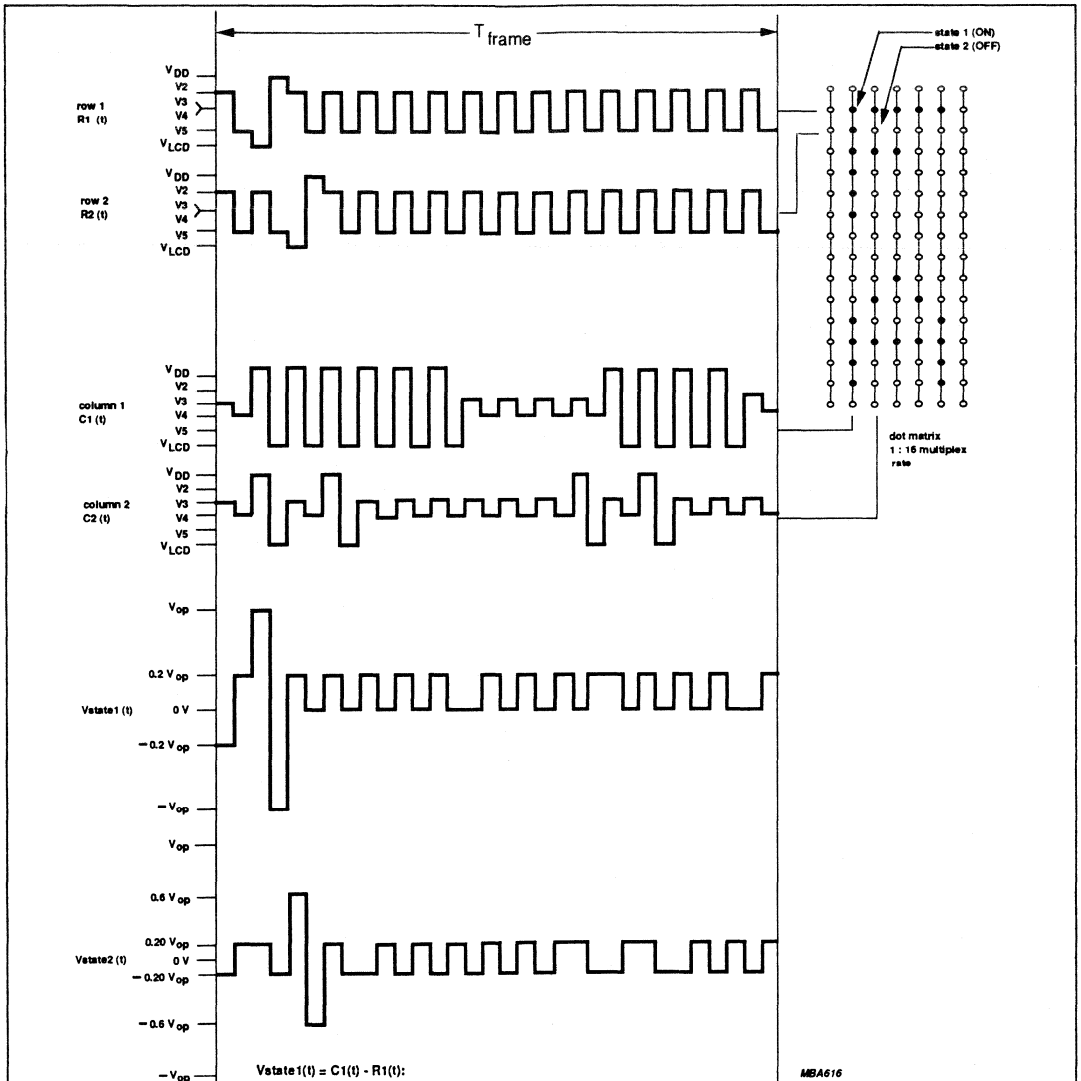


Fig.8 LCD drive mode waveforms for 1:16 multiplex.

Power-on Reset

At power-on the PCF8568 resets to a defined starting condition as follows:

1. Display blank.
2. I²C-bus interface is initialized.
3. Device in reset state awaiting first SET MODE (see Table 1).

Data transfers on the I²C-bus should be avoided for 1 ms following power-on to allow completion of the reset action.

Timing generation and control

The timing generation and control block of the PCF8568 organizes the internal data flow of the device and either generates or synchronizes with the LCD frame synchronization pulse $\overline{SYNC}$, whose period is an integer multiple of the clock period. This signal maintains the correct timing relationship between the PCF8568 and the column drivers (and, if also used, a cascaded PCF8568).

Row driver outputs

R0 to R15 are row outputs which must be connected to the LCD. Unused outputs should be left open-circuit. Using a multiplex rate of 1:8, two sets of row outputs are driven, thus facilitating split screen configurations; i.e. a row pulse appears simultaneously at R0 and R9, R1 and R10 etc.

Shift register

The row select pulse is shifted through the shift register. Timing is derived from the timing and control block.

Bias generator

The intermediate LCD bias voltages are generated in this block. Buffered row bias voltages (V2 and V5 in Fig. 1) are connected internally to the row driver outputs. Buffered column bias voltages are available at pins VO3 and VO4.

I²C-bus control

The I²C-bus controller detects the I²C-bus protocol, slave address and command bytes. It performs the conversion of the data input (serial-to-parallel). The PCF8568 acts as an I²C-bus slave receiver.

Input filters

To enhance noise immunity in electrically adverse environments, RC low-pass filters are provided on the SDA and SCL lines.

I²C-bus protocol

Two 7-bit slave addresses (0111100 and 0111101) are reserved for the PCF8568 and PCF8569 or PCF8579 column drivers (see note below). Depending on the address, which is defined by SA0, two types of LCD display systems can be distinguished on the same I²C-bus. This allows:

(a) one PCF8568 to operate with up to 32 PCF8579s on the same I²C-bus for very large applications

(b) the use of two types of LCD multiplex schemes on the same I²C-bus.

In most applications the PCF8568 will have the same slave address as the column drivers.

The I²C-bus protocol is shown in Fig.9. All communications are initiated with a start condition (S) from the I²C-bus master, which is followed by the desired slave address and the read/write bit. All devices with this slave address acknowledge in parallel. All other devices ignore the bus transfer.

The PCF8568 operates in slave receiver mode only, hence the read/write bit $R/\overline{W} = 0$. The device receives one or more commands following slave address acknowledgement. The commands are also acknowledged by all addressed devices on the bus. The last command must clear the continuation bit C. After the last command a series of data bytes for the column drivers may follow. The acknowledgement after each byte is made only by the (A0, A1, A2 and A3) addressed column driver. The PCF8568 ignores data bytes and does not acknowledge. After the last data byte has been acknowledged, the I²C-bus master issues a stop condition (P).

Note: the PCF8578 row/column driver also uses the slave addresses above and is also designed for use with the PCF8569 or PCF8579 column drivers. Either the PCF8578 row/column driver or the PCF8568 row driver can be used depending upon the application.

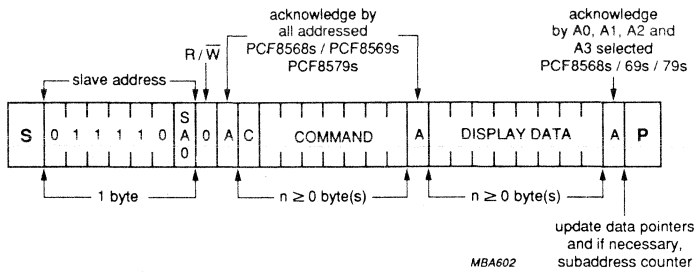


Fig.9 I²C-Bus protocol: master transmits to slave receiver.

Command decoder

The command decoder identifies command bytes that arrive on the I²C-bus. The most significant bit of a command is the continuation bit C (see Fig.10). When this bit is set, it indicates that the next byte to be transferred will also be a command. If the bit is reset, it indicates the conclusion of command transfer. Further bytes will be regarded as data. Commands are always transferred after a slave address with R/$\overline{W}$ = 0.

In an LCD system including the PCF8568, there are five commands. For the PCF8568 only one command, SET MODE, is relevant. All other commands are treated as NOP (No Operation) by the PCF8568. The SET MODE command is defined in Fig. 11.

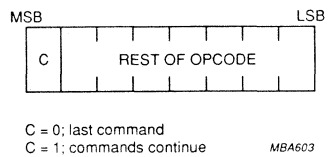


Fig.10 General format of command byte.

COMMAND / OPCODE	OPTIONS			DESCRIPTION
SET MODE C 1 0 0 E1 E0 M1 M0 Note: this bit must be zero	LCD DRIVE MODE BITS	M1	M0	DEFINES LCD DRIVE MODE
	1:8 MUX (8 ROWS)	0	1	
	1:16 MUX (16 ROWS)	1	0	
	1:24 MUX (24 ROWS)	1	1	
	1:32 MUX (32 ROWS)	0	0	
	DISPLAY STATUS BITS	E1	E0	DEFINES DISPLAY STATUS
	BLANK	0	0	
	NORMAL	0	1	
	ALL SEGMENTS ON	1	0	
	INVERSE VIDEO	1	1	

MBA604

Fig.11 Definition of the PCF8568 SET MODE command

CHARACTERISTICS OF THE I²C BUS

The I²C-bus is for bi-directional, two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as a control signal.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

System configuration

A device generating a message is a "transmitter", a device receiving a message is the "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is unlimited. Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter during which time the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.

The device that acknowledges must pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

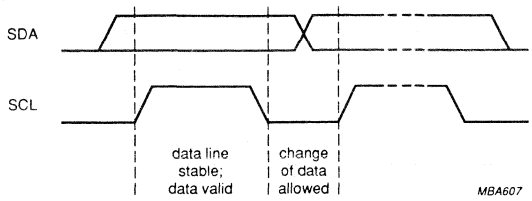


Fig.12 Bit transfer.

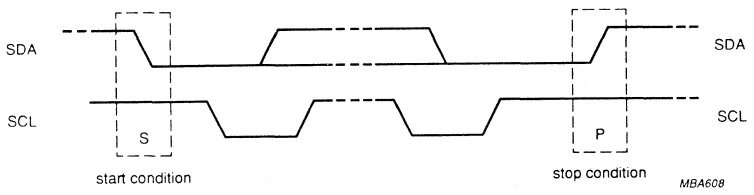


Fig.13 Definition of start and stop conditions.

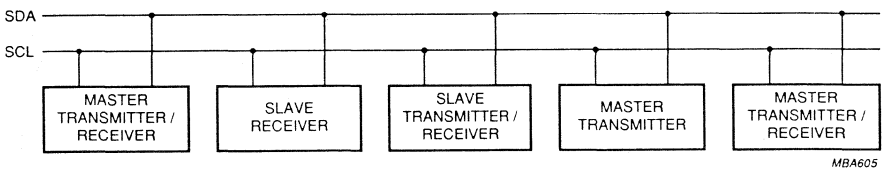
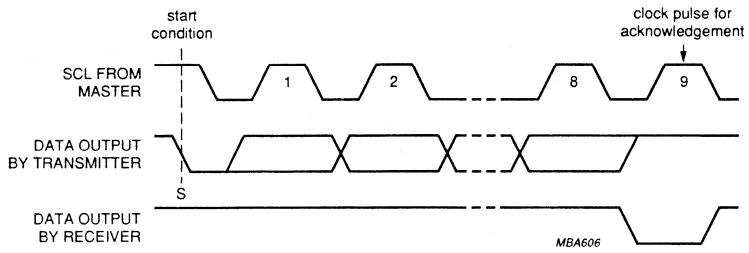


Fig.14 System configuration.



Note: the general characteristics and detailed specification of the I²C-bus are available on request.

Fig.15 Acknowledgement on the I²C-bus.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage range	−0.5	+8.0	V
V_{LCD}	LCD supply voltage range voltage	V_{DD} −11	V_{DD}	V
$V_{I(1)}$	input voltage range at SDA, SCL, $\overline{SYNC}$, SA0, EXT, and OSC	V_{SS} −0.5	V_{DD} +0.5	V
$V_{O(1)}$	output voltage range at SDA, OSC, and $\overline{SYNC}$	V_{SS} −0.5	V_{DD} +0.5	V
$V_{O(2)}$	VO3, VO4, and RO-R15	V_{LCD} −0.5	V_{DD} +0.5	V
I_I	DC input current	−10	10	mA
I_O	DC output current	−10	10	mA
I_{DD}, I_{SS} or I_{LCD}	V_{DD}, V_{SS} or V_{LCD} current	−50	50	mA
P_{tot}	power dissipation per package	-	400	mW
P_O	power dissipation per output	-	100	mW
T_{stg}	storage temperature range	−65	+150	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take precautions appropriate to handling MOS devices (see 'Handling MOS Devices'.)

CHARACTERISTICS

V_{DD} = 2.5 V to 6 V; V_{SS} = 0 V; V_{LCD} = V_{DD} −3.5 V to V_{DD} −9.0 V; T_{amb} = −40 to +85 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DC						
V_{DD}	supply voltage		2.5	-	6.0	V
V_{LCD}	LCD supply voltage		V_{DD} −9	-	V_{DD} −3.5	V
$I_{DD(1)}$	supply current external clock	note 1; f_{OSC} = 12 kHz	-	62	120	µA
$I_{DD(2)}$	supply current internal clock	note 1; R_{OSC} = 330 kΩ	-	67	150	µA
V_{POR}	power-on reset level	note 2	-	1.3	1.8	µA
logic (except EXT)						
V_{IL}	input logic LOW		V_{SS}	-	0.3 V_{DD}	V
V_{IH}	input voltage HIGH		0.7 V_{DD}	-	V_{DD}	V
EXT						
$V_{IL(E)}$	input voltage LOW		V_{SS}	-	V_{SS} +0.1	V
$V_{IH(E)}$	input voltage HIGH		V_{DD} −0.1	-	V_{DD}	V
V_M	input voltage V_M		1.15	-	V_{DD} −1.15	V
$I_{OL(1)}$	output current LOW at $\overline{SYNC}$ and CLK	V_{OL} = 1.0 V V_{DD} = 5.0 V	1	-	-	mA
$I_{OH(1)}$	output current HIGH at $\overline{SYNC}$ and CLK	V_{OH} = 4.0 V V_{DD} = 5.0 V	-	-	−1	mA
$I_{OL(2)}$	SDA output current LOW	V_{OL} = 0.4 V V_{DD} = 5.0 V	3.0	-	-	mA
$I_{L(1)}$	leakage current at SDA, SCL, $\overline{SYNC}$, SA0 and EXT	V_I = V_{DD} or V_{SS}	−1	-	1	µA
$I_{L(2)}$	leakage current at OSC	note 3; V_I = V_{DD} or V_{SS}	−1	-	1	µA
CI	input capacitor	note 4	-	-	5	pF
LCD Outputs						
R_O	output resistance at R0-R15	note 5	-	1.5	3.0	kΩ
±VTOL	V2, VO3, VO4 and V5 tolerance	note 6	-	20	100	mV
ISO	I (source) on VO3; VO4	note 7	-	-	−1.5	mA
ISI	I (sink) on VO3, VO4	note 8	1.5	-	-	mA
AC (note 9)						
f_{CLK1}	clock frequency at multiplex rates of 1:8, 1:16 and 1:32	R_{OSC} = 330 kΩ; V_{DD} = 6 V	1.2	2.1	3.3	kHz
f_{CLK2}	clock frequency at multiplex rate of 1:24	R_{OSC} = 330 kΩ; V_{DD} = 6 V	0.9	1.6	2.5	kHz
f_{OSC}	external clock		7.7	12.4	19.2	kHz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
AC (note 9)						
$t_{P\text{-}\overline{SYNC}}$	$\overline{SYNC}$ propagation delay		-	-	500	ns
t_{PLCD}	driver delays	$V_{DD} - V_{LCD} = 9$ V	-	-	100	µs
I²C-bus						
f_{SCL}	SCL clock frequency		-	-	100	kHz
t_{SW}	tolerable spike width on bus		-	-	100	ns
t_{BUF}	bus free time		4.7	-	-	µs
$t_{SU;STA}$	start condition set-up time	repeated start codes only	4.7	-	-	µs
$t_{HD;STA}$	start condition on hold time		4.0	-	-	µs
t_{LOW}	SCL LOW time		4.7	-	-	µs
t_{HIGH}	SCL HIGH time		4.0	-	-	µs
t_r	SCL and SDA rise time		-	-	1.0	µs
t_f	SCL and SDA fall time		-	-	0.3	µs
$t_{SU;DAT}$	data set-up time		250	-	-	ns
$t_{HD;DAT}$	data hold time		0	-	-	ns
$t_{VD;DAT}$	SCL LOW to data out valid		-	-	3.4	µs
$t_{SU;STO}$	stop condition set-up time		4.0	-	-	µs

Notes

1. Outputs are open; inputs at V_{DD} or V_{SS}; I²C-bus inactive; external clock with 50% duty cycle (I_{DD1} only).
2. Resets all logic when $V_{DD} < V_{POR}$.
3. EXT = V_{DD} or V_M.
4. Periodically sampled; not 100% tested.
5. Resistance of output terminal (R0 to R15) with $I_{LOAD} = 150$ µA; $V_{OP} = V_{DD}-V_{LCD} = 9.0$ V; outputs measured one at a time.
6. LCD outputs open.
7. $V_{OP} = V_{DD}-V_{LCD} = 9.0$ V; VO3 = 5.8 V; VO4 = 2.2 V; 1:32 multiplex.
8. $V_{OP} = V_{DD}-V_{LCD} = 9.0$ V; VO3 = 6.8 V; VO4 = 3.2 V; 1:32 multiplex.
9. All timing values referred to V_{IH} and V_{IL} levels with an input voltage swing of V_{SS} to V_{DD}.

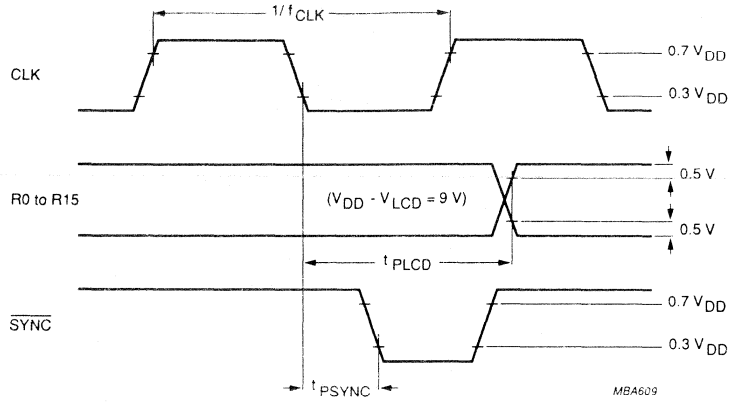


Fig.16 Driver timing waveforms.

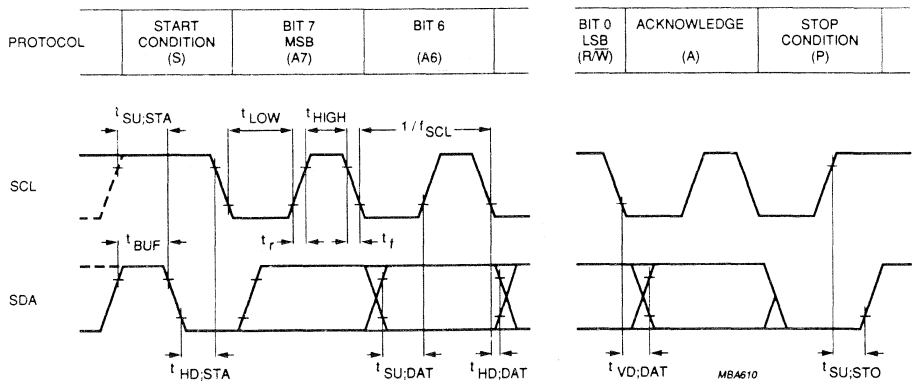


Fig.17 I²C timing diagram.

PURCHASE OF PHILIPS I²C COMPONENTS

Purchase of Philips I²C components conveys a license under Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips (ordering code of the I²C specification: 9398 358 10011).

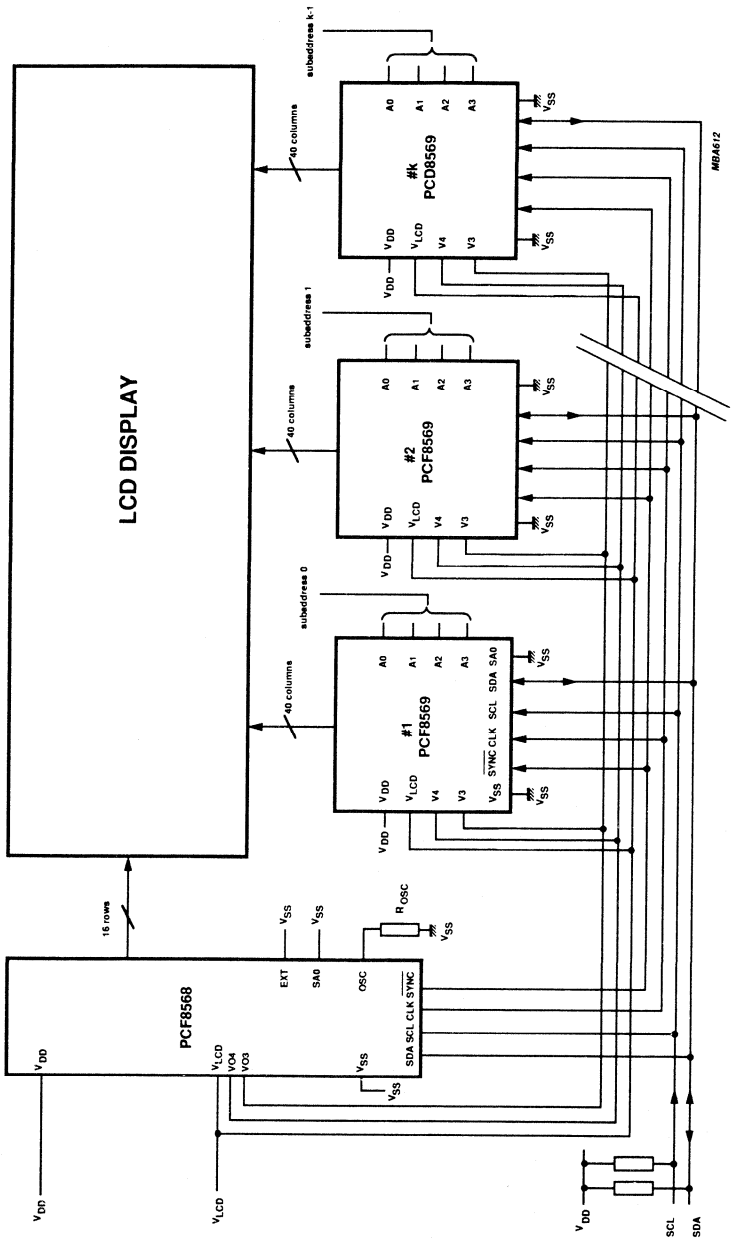


Fig.18 Typical driver system with 1:16 multiplex.

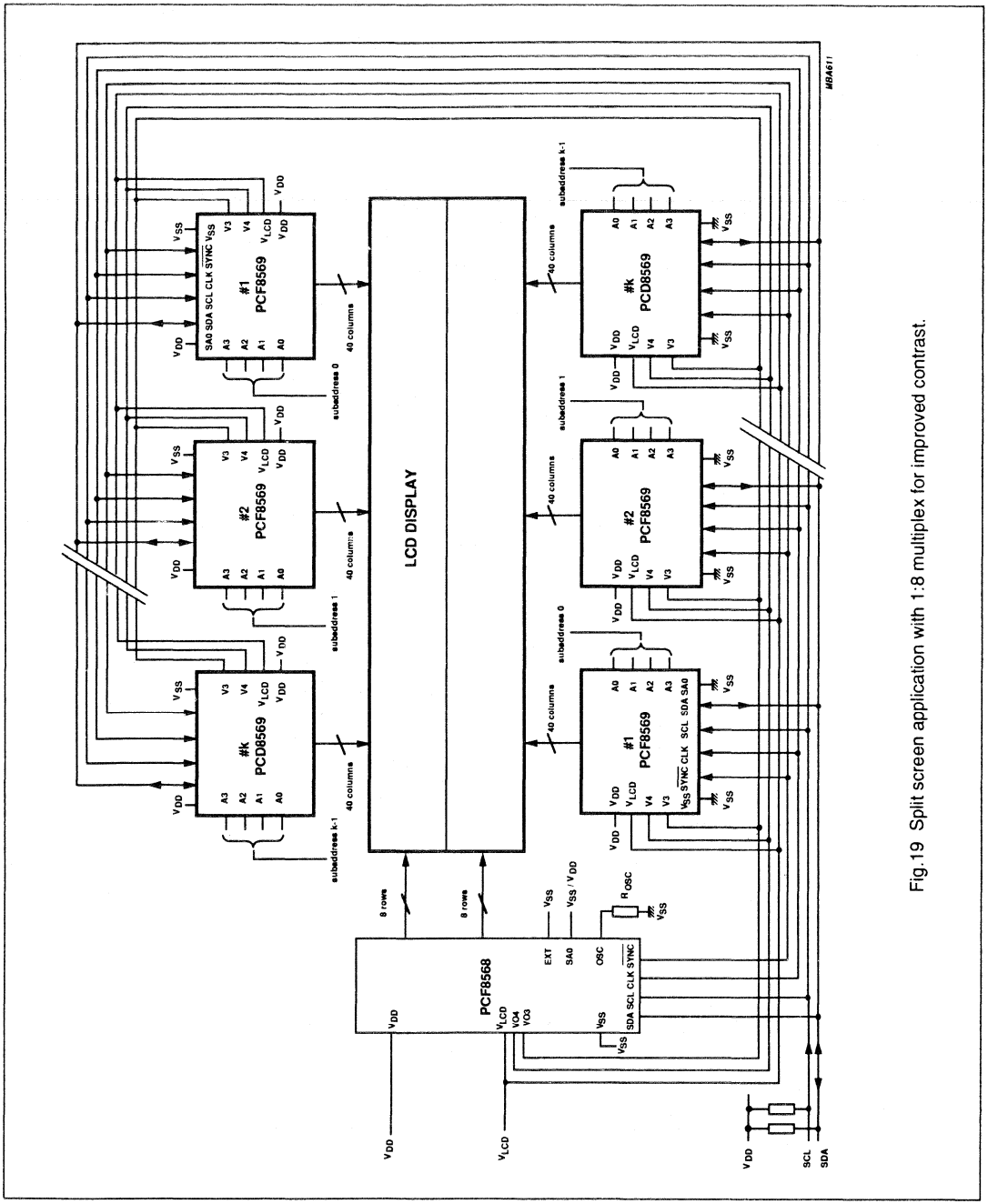


Fig.19 Split screen application with 1:8 multiplex for improved contrast.

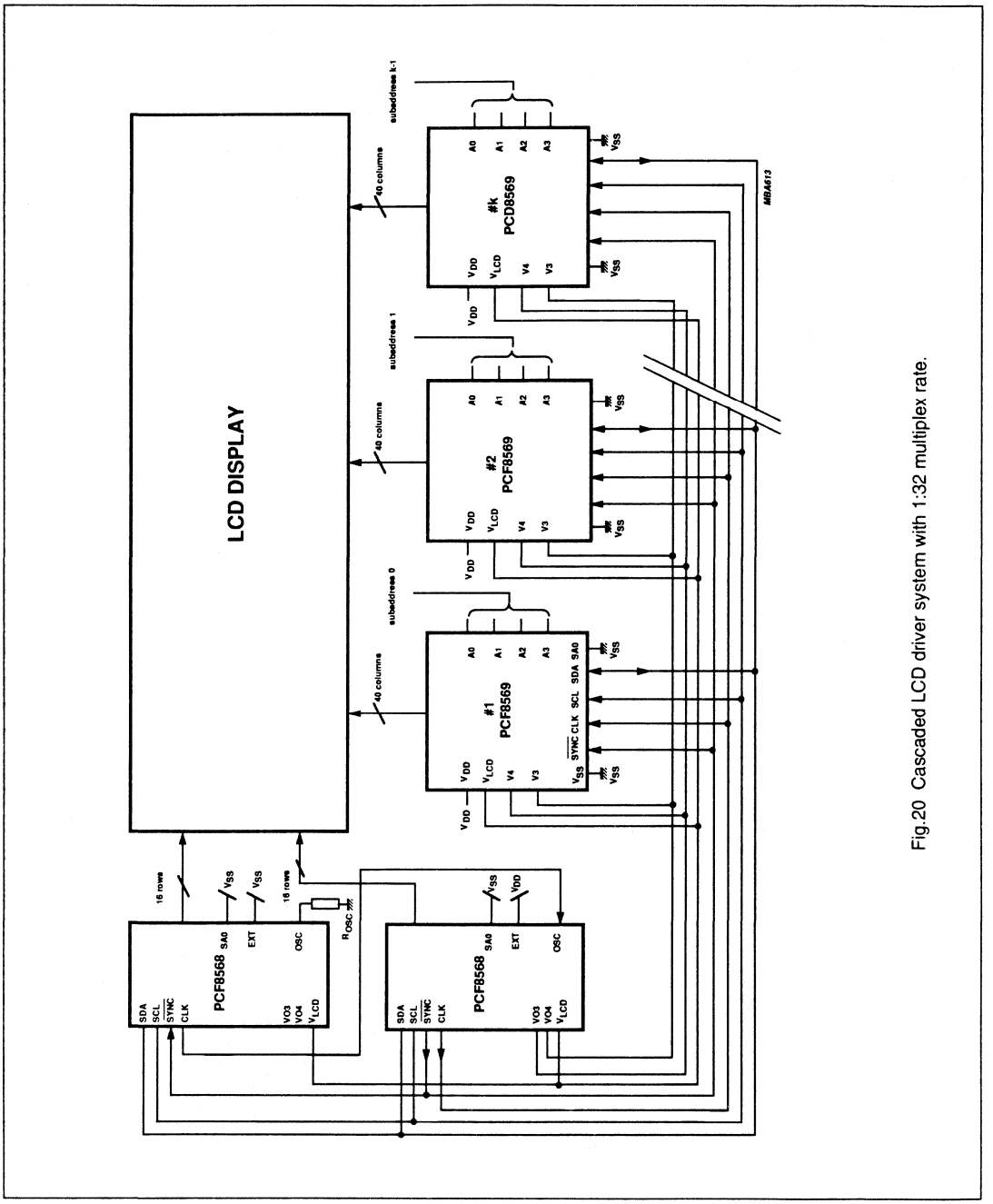


Fig.20 Cascaded LCD driver system with 1:32 multiplex rate.

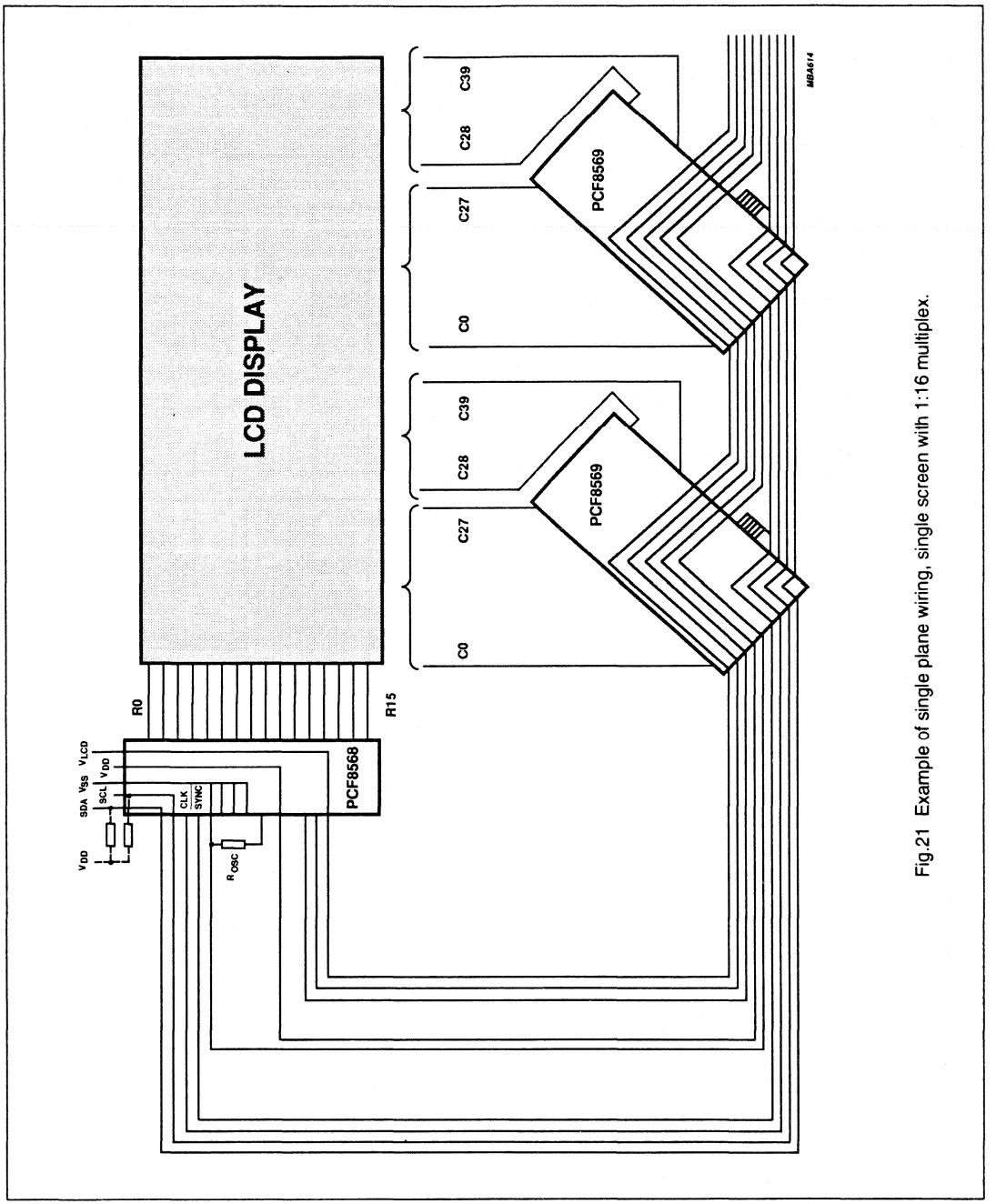


Fig.21 Example of single plane wiring, single screen with 1:16 multiplex.

LCD column driver for dot matrix graphic displays PCF8569

GENERAL DESCRIPTION

The PCF8569 is a low power CMOS LCD column driver, designed to drive dot matrix graphic displays at multiplex rates of 1:8 or 1:16. The device has 40 outputs and can drive 16 x 40 dots in a 16 row multiplexed LCD. Up to 16 PCF8569s can be cascaded and up to 32 devices may be used on the same I²C-bus (using the two slave addresses). The device is optimized for use with the PCF8568/78/79 family of LCD row/column drivers. Together the PCF8568, PCF8578 and PCF8569 form a general LCD dot matrix driver chip set, capable of driving displays of up to 20 480 dots. The PCF8569 is compatible with most microcontrollers and communicates via a two-line bidirectional bus (I²C-bus). Communication overheads are minimized by a display RAM with auto-incremented addressing and display bank switching.

Features

- LCD column driver
- Used in conjunction with the PCF8568 or PCF8578, this device forms part of a chip set capable of driving up to 20 480 dots.
- 40 column outputs
- Selectable multiplex rates; 1:8 or 1:16
- Externally selectable bias configuration, 5 or 6 levels
- Easily cascadable for large applications
- 640-bit RAM for display data storage
- Display memory bank switching
- Auto-incremented data loading across hardware subaddress boundaries
- Power-on reset blanks display
- Logic voltage supply range 2.5 V to 6.0 V
- Maximum LCD supply voltage 9 V
- Low power consumption
- I²C-bus interface
- TTL/CMOS compatible
- Compatible with most microcontrollers
- Optimized pinning for single plane wiring in multiple device applications
- Space saving 56-lead plastic mini-pack or 64-lead tab module

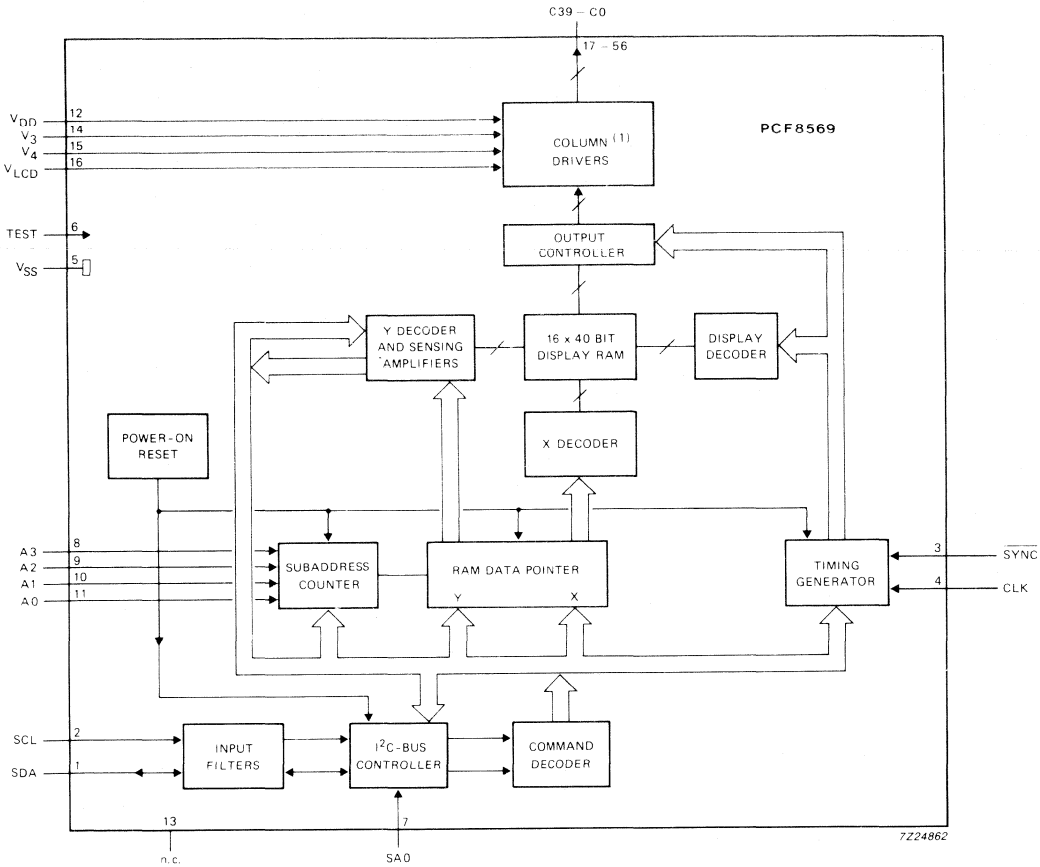
APPLICATIONS

- Automotive information systems
- Telecommunication systems
- Point-of-sale terminals
- Computer terminals
- Instrumentation

PACKAGE OUTLINES

PCF8569T: 56-lead mini-pack; plastic (VSO56; SOT190).
PCF8569V: 64-lead tape-automated-bonding (tab) module (SOT267).

LCD column driver for dot matrix graphic displays PCF8569



(1) LCD voltage levels, all other blocks operate at logic levels.

Fig.1 Block diagram (pin numbers shown for VSO56; SOT190).

128 × 8-bit/256 × 8-bit static RAMs with I²C-bus interface

PCF8570/8570C/8571

GENERAL DESCRIPTION

The PCF8570, PCF8570C and PCF8571 are low-power static CMOS RAMs. The PCF8570 and PCF8570C are organized as 256 words by 8-bits and the PCF8571 is organized as 128 words by 8-bits. Addresses and data are transferred serially via a two-line bidirectional bus (I²C). The built-in word address register is incremented automatically after each written or read data byte. Three address pins A0, A1 and A2 are used for hardware address, allowing the use of up to eight devices connected to the bus without additional hardware. For system expansion over 8 devices the PCF8570/71 can be used in conjunction with the PCF8750C which has an alternative slave address for memory extension up to 16 devices.

Features

- Operating supply voltage 2.5 V to 6 V
- Low data retention voltage min. 1.0 V
- Low standby current max. 15 μA
- Power saving mode typ. 50 nA
- Serial input/output bus (I²C)
- Address by 3 hardware address pins
- Automatic word address incrementing
- 8-lead DIL package

Applications

- Telephony — RAM expansion for stored numbers in repertory dialling (e.g. PCD3343 applications)
- Radio and television — channel presets
- Video cassette recorder — channel presets
- General purpose — RAM expansion for the microcontroller families MAB8400, PCF84CXX and most other microcontrollers

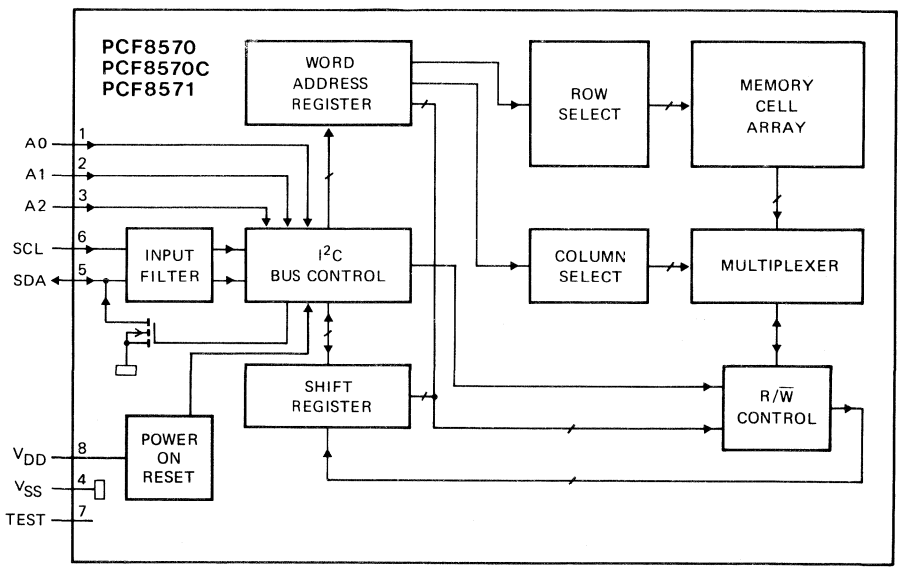


Fig.1 Block diagram.

PACKAGE OUTLINES

PCF8570/PCF8570C/PCF8571/P: 8-lead DIL; plastic (SOT97).
PCF8570/PCF8570C/PCF8571/T: 8-lead mini-pack (SO8L; SOT176C).

PINNING

1 to 3	A0 to A2	address inputs
4	V_{SS}	negative supply
5	SDA	serial data line } I²C-bus
6	SCL	serial clock line } I²C-bus
7	TEST	test input for test speed-up; must be connected to V_{SS} when not in use (power saving mode, see Figs 12 and 13)
8	V_{DD}	positive supply

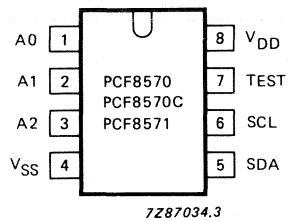


Fig.2 Pinning diagram.

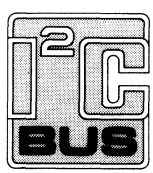
RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage range	V_{DD}	−0.8	+8.0	V
Input voltage range	V_I	−0.8	V_{DD} + 0.8	V
DC input current	$\pm I_I$	–	10	mA
DC output current	$\pm I_O$	–	10	mA
V_{DD} or V_{SS} current	$\pm I_{DD}$; $\pm I_{SS}$	–	50	mA
Total power dissipation	P_{tot}	–	300	mW
Power dissipation per output	P_O	–	50	mW
Operating ambient temperature range	T_{amb}	−40	+85	°C
Storage temperature range	T_{stg}	−65	+150	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is good practice to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').



Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

CHARACTERISTICS

V_{DD} = 2.5 to 6 V; V_{SS} = 0 V; T_{amb} = −40 to +85 °C unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage		V_{DD}	2.5	–	6.0	V
Supply current	$V_I = V_{DD}$ or V_{SS}					
operating	f_{SCL} = 100 kHz	I_{DD}	–	–	200	μA
standby	f_{SCL} = 0 Hz	I_{DDO}	–	–	15	μA
	T_{amb} = −25 to +70 °C	I_{DDO}	–	–	5	μA
Power-on reset level	note 1	V_{POR}	1.5	1.9	2.3	V
Inputs, input/output SDA						
Input voltage LOW	note 2	V_{IL}	−0.8	–	0.3 V_{DD}	V
Input voltage HIGH	note 2	V_{IH}	0.7 V_{DD}	–	V_{DD} + 0.8	V
Output current LOW	V_{OL} = 0.4 V	I_{OL}	3	–	–	mA
Leakage current	$V_I = V_{DD}$ or V_{SS}	$\|I_{LI}\|$	–	–	1	μA
Inputs A0 to A2; TEST						
Input leakage current	$V_I = V_{DD}$ or V_{SS}	$\pm I_{LI}$	–	–	250	nA
Inputs SCL; SDA						
Input capacitance	$V_I = V_{SS}$	C_I	–	–	7	pF
LOW V_{DD} data retention						
Supply voltage for data retention		V_{DDR}	1	–	6	V
Supply current	V_{DDR} = 1 V	I_{DDR}	–	–	5	μA
Supply current	V_{DDR} = 1 V; T_{amb} = −25 to +70 °C	I_{DDR}	–	–	2	μA
Power saving mode	see Figs 12 and 13					
Supply current	TEST = V_{DD}; T_{amb} = 25 °C					
PCF8570/PCF8570C		I_{DDR}	–	50	400	nA
PCF8571		I_{DDR}	–	50	200	nA
Recovery time		t_{HD2}	–	50	–	μs

Notes to the characteristics

1. The power-on reset circuit resets the I²C-bus logic when $V_{DD} < V_{POR}$. The status of the device after a power-on reset condition can be tested by sending the slave address and testing the acknowledge bit.
2. If the input voltages are a diode voltage above or below the supply voltage V_{DD} or V_{SS} an input current will flow: this current must not exceed ± 0.5 mA.

CHARACTERISTICS OF THE I²C-BUS

The I²C-bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

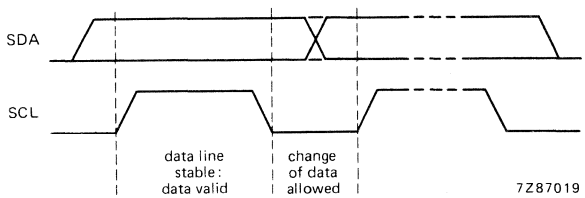


Fig.3 Bit transfer.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

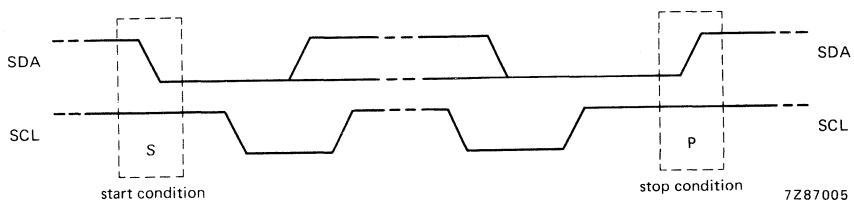


Fig.4 Definition of start and stop conditions.

System configuration

A device generating a message is a "transmitter", a device receiving a message is the "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

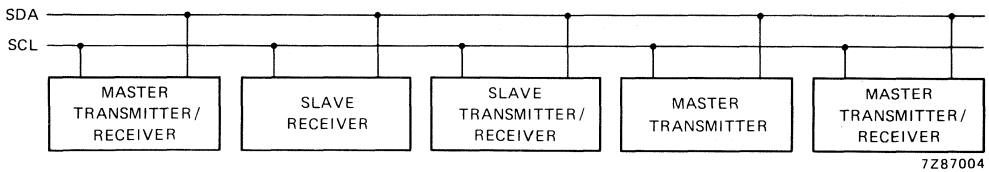


Fig.5 System configuration.

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set-up and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

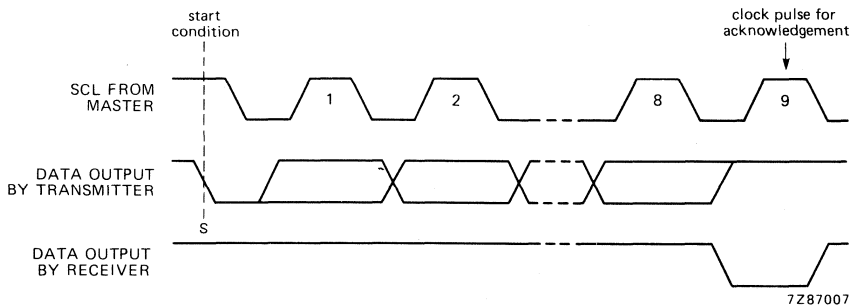


Fig.6 Acknowledgement on the I²C-bus.

Timing specifications

All the timing values are valid within the operating supply voltage and ambient temperature range and refer to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.

parameter	symbol	min.	typ.	max.	unit
SCL clock frequency	f_{SCL}	–	–	100	kHz
Tolerable spike width on bus	t_{SW}	–	–	100	ns
Bus free time	t_{BUF}	4.7	–	–	μs
Start condition set-up time	$t_{SU;STA}$	4.7	–	–	μs
Start condition hold time	$t_{HD;STA}$	4.0	–	–	μs
SCL LOW time	t_{LOW}	4.7	–	–	μs
SCL HIGH time	t_{HIGH}	4.0	–	–	μs
SCL and SDA rise time	t_r	–	–	1.0	μs
SCL and SDA fall time	t_f	–	–	0.3	μs
Data set-up time	$t_{SU;DAT}$	250	–	–	ns
Data hold time	$t_{HD;DAT}$	0	–	–	ns
SCL LOW to data out valid	$t_{VD;DAT}$	–	–	3.4	μs
Stop condition set-up time	$t_{SU;STO}$	4.0	–	–	μs

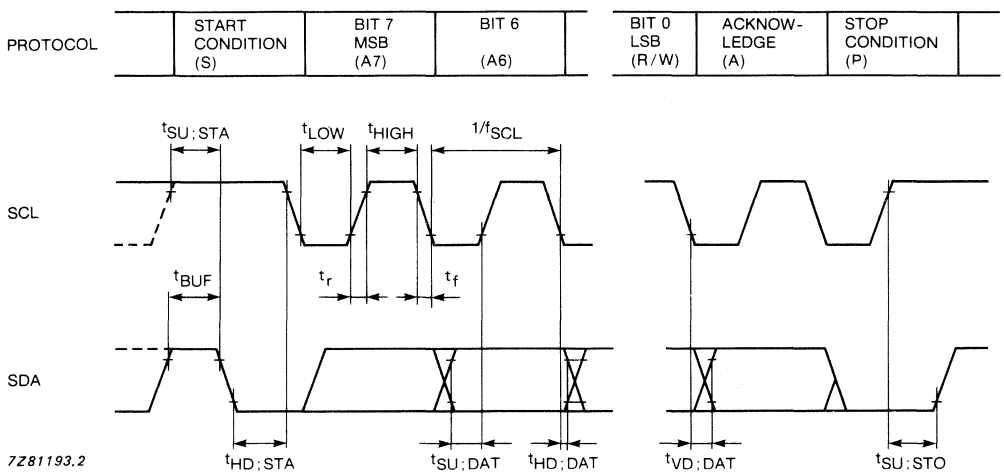


Fig.7 I²C-bus timing diagram.

Bus protocol

Before any data is transmitted on the I²C-bus, the device which should respond is addressed first. The addressing is always done with the first byte transmitted after the start procedure. The I²C-bus configuration for different PCF8570/PCF8570C/PCF8571 READ and WRITE cycles is shown in Fig.8.

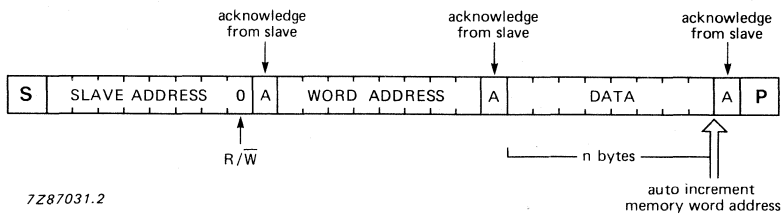


Fig.8(a) Master transmits to slave receiver (WRITE mode).

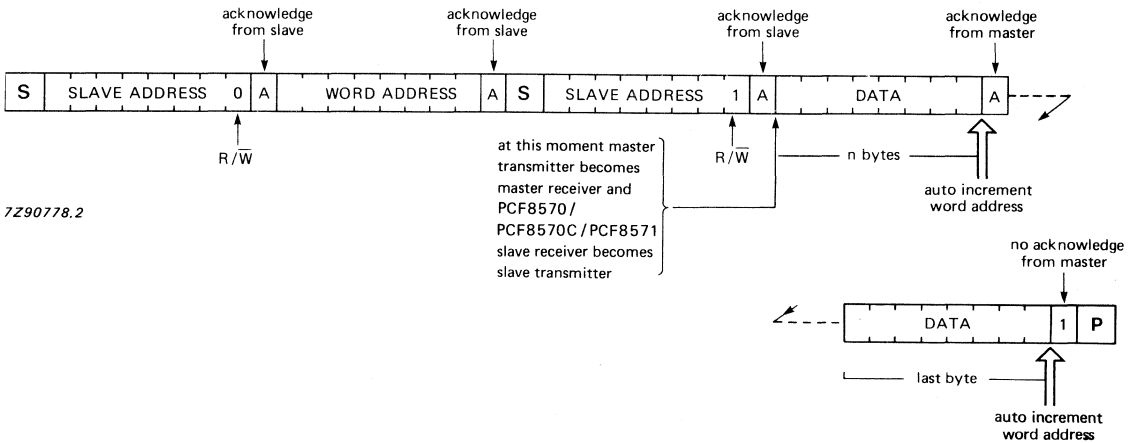


Fig.8(b) Master reads after setting word address (WRITE word address; READ data).

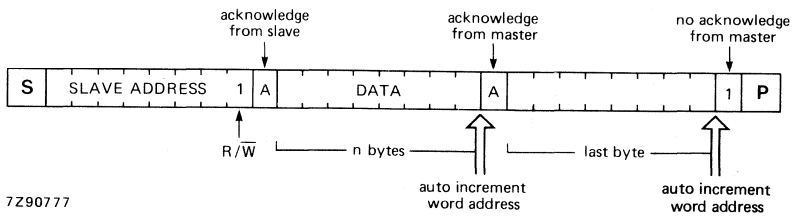


Fig.8(c) Master reads slave immediately after first byte (READ mode).

APPLICATION INFORMATION

The PCF8570/PCF8571 slave address has a fixed combination 1010 as group 1, while group 2 is fully programmable (see Fig.9). The PCF8570C has slave address 1011 as group 1, while group 2 is fully programmable (see Fig.10).

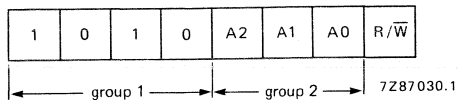


Fig.9 PCF8570 and PCF8571 address.

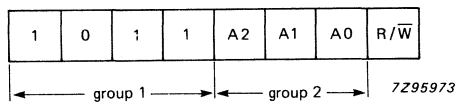
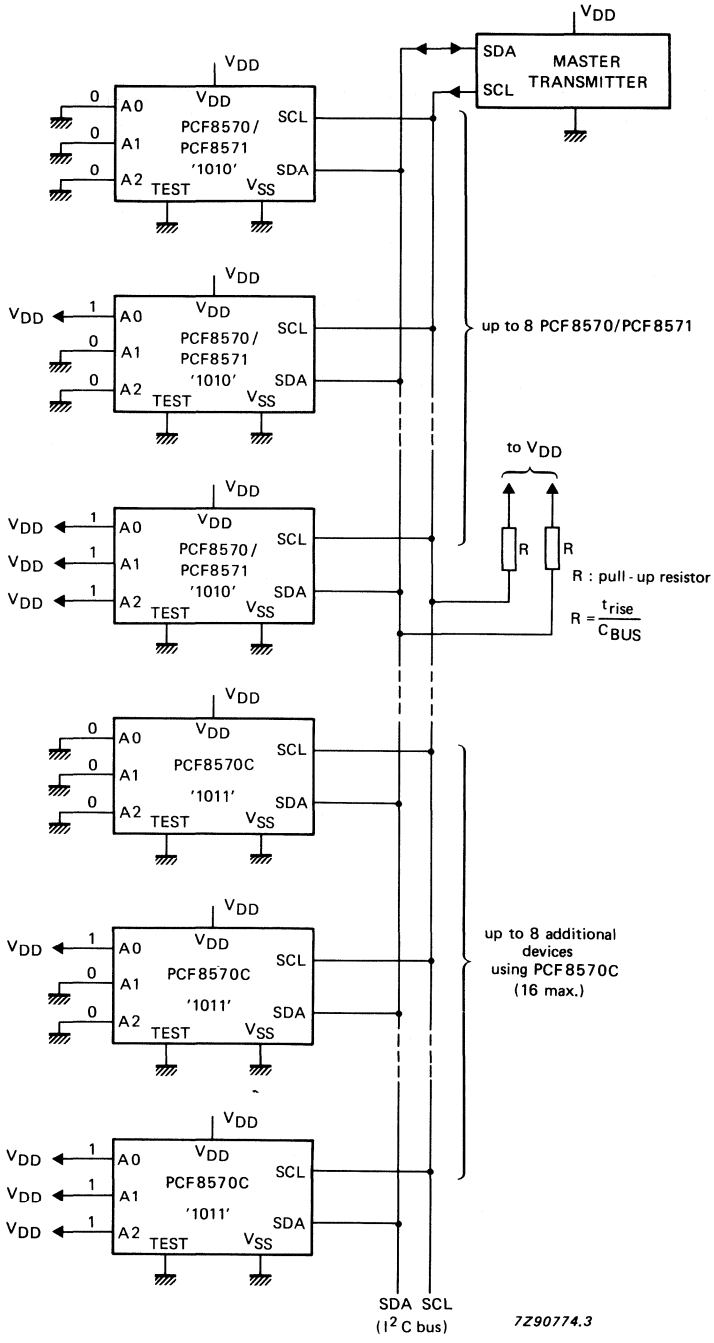


Fig.10 PCF8570C address.

Note

A0, A1, and A2 inputs must be connected to V_{DD} or V_{SS} but not left open-circuit.

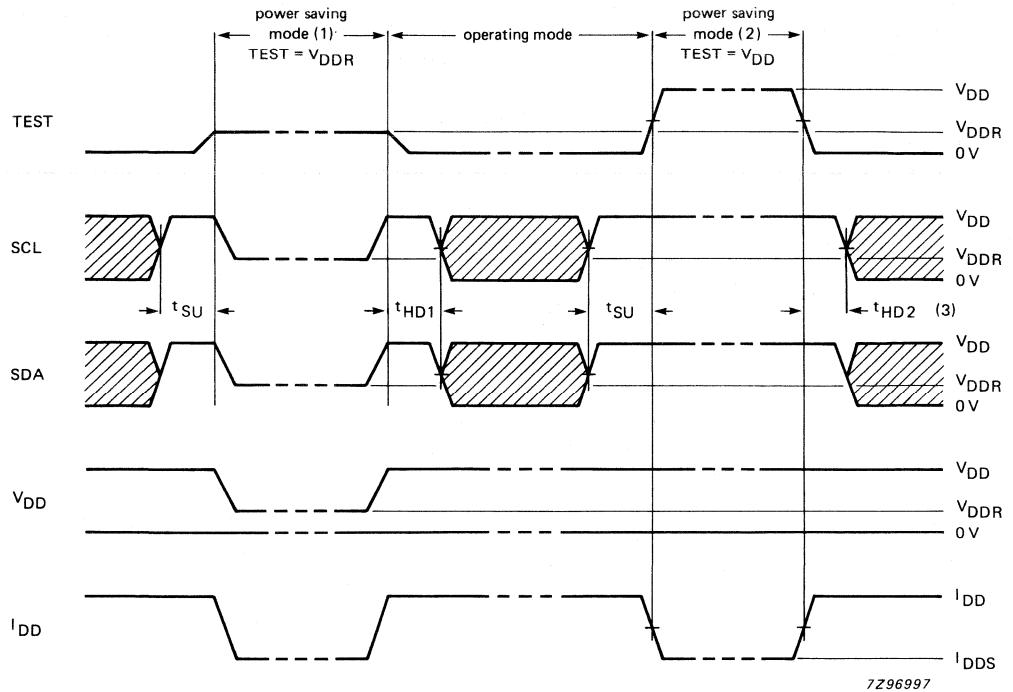


It is recommended that a 4.7 μF/10 V solid aluminium capacitor (SAL) be connected between V_{DD} and V_{SS}.

Fig.11 Application diagram.

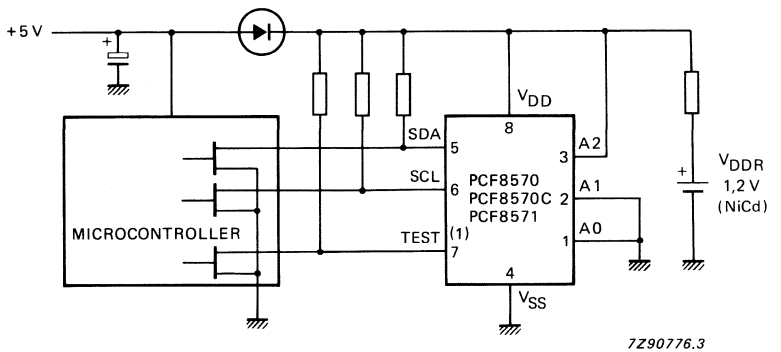
POWER SAVING MODE

With the condition **TEST** = V_{DD} or V_{DDR} the PCF8570/PCF8570C/PCF8571 goes into the power saving mode and I²C-bus logic is reset.



(1) Power saving mode without 5 V supply voltage.
(2) Power saving mode with 5 V supply voltage.
(3) t_{SU} and $t_{HD1} \geqslant 4\ \mu s$ and $t_{HD2} \geqslant 50\ \mu s$.

Fig.12 Timing for power saving mode.



(1) In the operating mode TEST = 0; In the power saving mode TEST = V_{DDR}.

It is recommended that a 4.7 μF/10 V solid aluminium capacitor (SAL) be connected between V_{DD} and V_{SS}.

Fig.13 Application example for power saving mode.

Clock/calendar with serial I/O PCF8573

GENERAL DESCRIPTION

The PCF8573 is a low threshold, CMOS circuit that functions as a real time clock/calendar with an I²C-bus interface.
The IC incorporates an addressable time counter and an addressable alarm register for minutes, hours, days and months. Three special control/status flags, COMP, POWF and NODA, are also available. Information is transferred via a serial two-line bidirectional bus (I²C). Back-up for the clock during supply interruptions is provided by a 1.2 V nickel cadium battery. The time base is generated from a 32.768 kHz crystal-controlled oscillator.

Features

- Serial input/output I²C-bus interface for minutes, hours, days and months
- Additional pulse outputs for seconds and minutes
- Alarm register for presetting a time for alarm or remote switching functions
- Battery back-up for clock function during supply interruption
- Crystal oscillator control (32.768 kHz)

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage range					
clock (pin 16 to pin 15)	$V_{DD}-V_{SS1}$	1.1	–	6.0	V
I²C interface (pin 16 to pin 8)	$V_{DD}-V_{SS2}$	2.5	–	6.0	V
Crystal oscillator frequency	f_{osc}	–	32.768	–	kHz

PACKAGE OUTLINES

PCF8573P: 16-lead DIL; plastic (SOT38).
PCF8573T: 16-lead mini-pack; plastic (SO16L; SOT162A).

Clock/calendar with serial I/O PCF8573

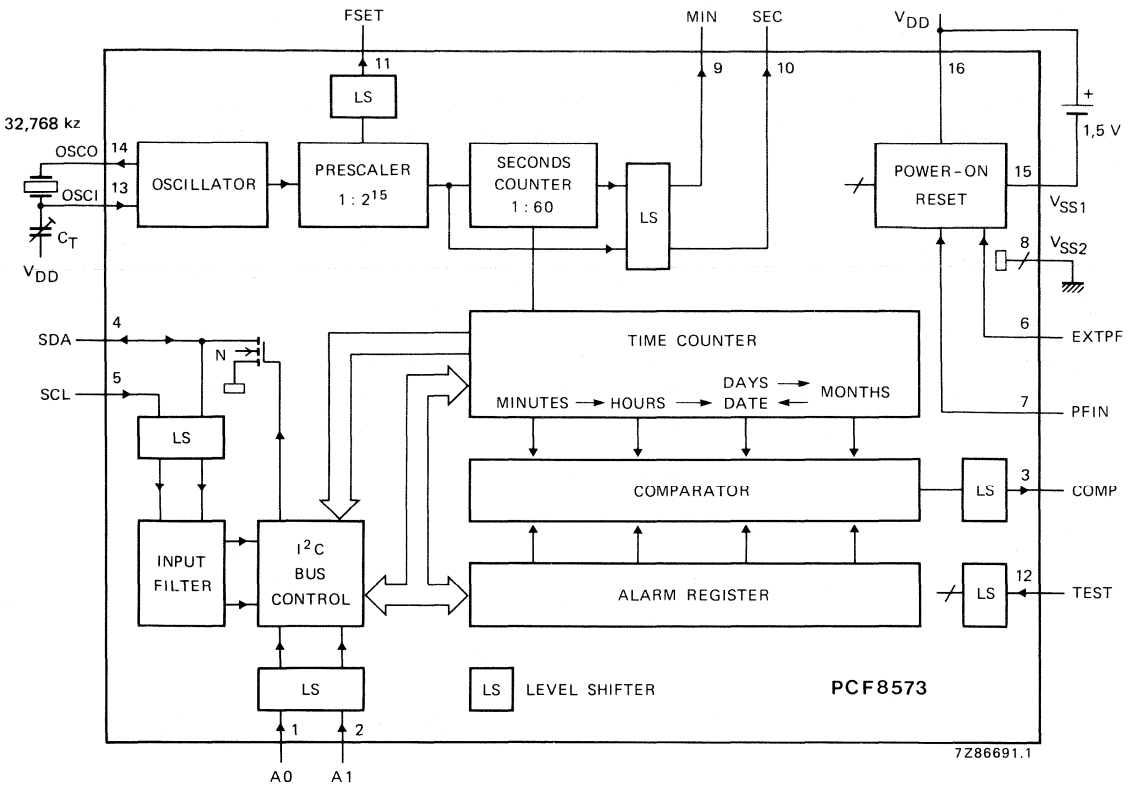


Fig.1 Block diagram.

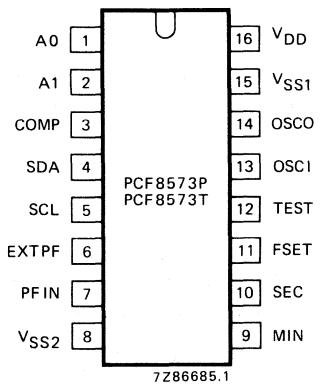


Fig.2 Pinning diagram.

PINNING

1	A0	address input	
2	A1	address input	
3	COMP	comparator output	
4	SDA	serial data line	I²C-bus
5	SCL	serial clock line	I²C-bus
6	EXTPF	enable power fail flag input	
7	PFIN	power fail flag input	
8	V_{SS2}	negative supply 2 (I²C interface)	
9	MIN	one pulse per minute output	
10	SEC	one pulse per second output	
11	FSET	oscillator tuning output	
12	TEST	test input; must be connected to V_{SS2} when not in use	
13	OSCI	oscillator input	
14	OSCO	oscillator input/output	
15	V_{SS1}	negative supply 1 (clock)	
16	V_{DD}	common positive supply	

FUNCTIONAL DESCRIPTION

Oscillator

The PCF8573 has an integrated crystal-controlled oscillator which provides the timebase for the prescaler. The frequency is determined by a single 32.768 kHz crystal connected between OSCI and OSCO. A trimmer is connected between OSCI and V_{DD}.

Prescaler and time counter

The prescaler provides a 128 Hz signal at the FSET output for fine adjustment of the crystal oscillator without loading it. The prescaler also generates a pulse once a second to advance the seconds counter. The carry of the prescaler and the seconds counter are available at the outputs SEC, MIN respectively, and are also readable via the I²C-bus. The mark-to-space ratio of both signals is 1 : 1. The time counter is advanced one count by the falling edge of output signal MIN. A transition from HIGH-to-LOW of output signal SEC triggers MIN to change state. The time counter counts minutes, hours, days and months, and provides a full calendar function which needs to be corrected once every four years. Cycle lengths are shown in Table 1.

Table 1 Cycle length of the time counter

unit	number of bits	counting cycle	carry for following unit	content of month counter
minutes	7	00 to 59	59 → 00	
hours	6	00 to 23	23 → 00	
days	6	01 to 28	28 → 01	2 (note 1)
			or 29 → 01	2 (note 1)
		01 to 30	30 → 01	4, 6, 9, 11
		01 to 31	31 → 01	1, 3, 5, 7, 8, 10, 12
months	5	01 to 12	12 → 01	

Note to Table 1

1. Day counter may be set to 29 by a write transmission with EXECUTE ADDRESS.

Alarm register

The alarm register is a 24-bit memory. It stores the time-point for the next setting of the status flag COMP. Details of writing and reading of the alarm register are included in the description of the characteristics of the I²C-bus.

Comparator

The comparator compares the contents of the alarm register and the time counter, each with a length of 24 bits. When these contents are equal the flag COMP will be set 4 ms after the falling edge of MIN. This set condition occurs once at the beginning of each minute. This information is latched, but can be cleared by an instruction via the I²C-bus. A clear instruction may be transmitted immediately after the flag is set and will be executed. Flag COMP information is also available at the output COMP. The comparison may be based upon hours and minutes only if the internal flag NODA (no date) is set. Flag NODA can be set and cleared by separate instructions via the I²C-bus, but it is undefined until the first set or clear instruction has been received. Both COMP and NODA flags are readable via the I²C-bus.

FUNCTIONAL DESCRIPTION (continued)

Power on/power fail detection

If the voltage $V_{DD}-V_{SS1}$ falls below a certain value the operation of the clock becomes undefined. Thus a warning signal is required to indicate that faultless operation of the clock is not guaranteed. This information is latched in a flag called POWF (Power Fail) and remains latched after restoration of the correct supply voltage until a write procedure with EXECUTE ADDRESS has been received. The flag POWF can be set by an internally generated power fail level-discriminator signal for application with ($V_{DD}-V_{SS1}$) greater than V_{TH1}, or by an externally generated power fail signal for application with ($V_{DD}-V_{SS1}$) less than V_{TH1}. The external signal must be applied to the input PFIN. The input stage operates with signals of any slow rise and fall times. Internally or externally controlled POWF can be selected by input EXTPF as shown in Table 2.

Table 2 Power fail selection

EXTPF	PFIN	function
0	0	power fail is sensed internally
0	1	test mode
1	0	power fail is sensed externally
1	1	no power fail sensed

0 : connected to V_{SS1} (LOW)
1 : connected to V_{DD} (HIGH)

The external power fail control operates by absence of the $V_{DD}-V_{SS2}$ supply. Therefore the input levels applied to PFIN and EXTPF must be within the range of $V_{DD}-V_{SS1}$. A LOW level at PFIN indicates a power fail. POWF is readable via the I²C-bus. A power on reset for the I²C-bus control is generated on-chip when the supply voltage $V_{DD}-V_{SS2}$ is less than V_{TH2}.

Interface level shifters

The level shifters adjust the 5 V operating voltage ($V_{DD}-V_{SS2}$) of the microcontroller to the internal supply voltage ($V_{DD}-V_{SS1}$) of the clock/calendar. The oscillator and counter are not influenced by the $V_{DD}-V_{SS2}$ supply voltage. If the voltage $V_{DD}-V_{SS2}$ is absent ($V_{DD} = V_{SS2}$) the output signal of the level shifter is HIGH because V_{DD} is the common node of the $V_{DD}-V_{SS2}$ and the $V_{DD}-V_{SS1}$ supplies. Because the level shifters invert the input signal, the internal circuit behaves as if a LOW signal is present on the inputs. FSET, SEC, MIN and COMP are CMOS push-pull output stages. The driving capability of these outputs is lost when the supply voltage $V_{DD}-V_{SS2} = 0$.

CHARACTERISTICS OF THE I²C-BUS

The I²C-bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer (see Fig.3)

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

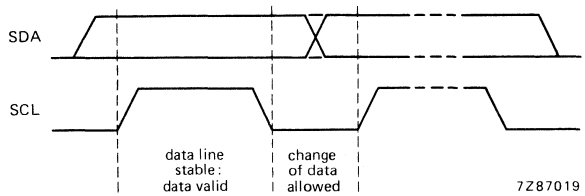


Fig.3 Bit transfer.

Start and stop conditions (see Fig. 4)

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

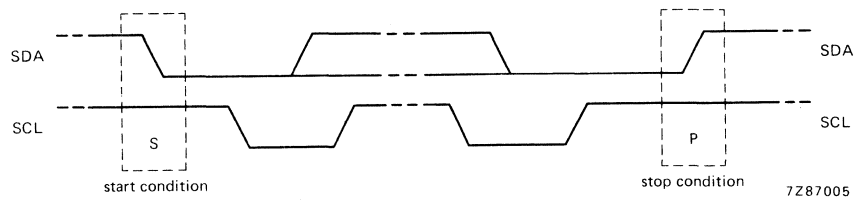


Fig.4 Definition of start and stop conditions.

System configuration (see Fig.5)

A device generating a message is a "transmitter", a device receiving a message is the "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

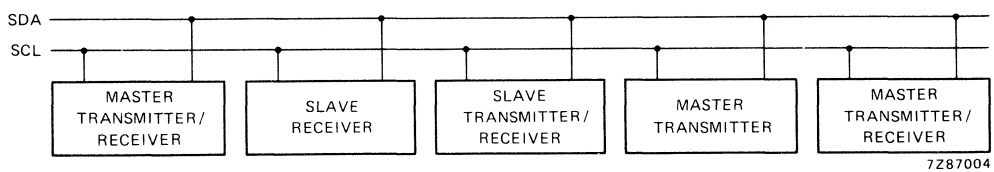


Fig.5 System configuration.

CHARACTERISTICS OF THE I²C-bus (continued)

Acknowledge (see Fig.6)

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set up and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition. (See Fig.10 and Fig.11).

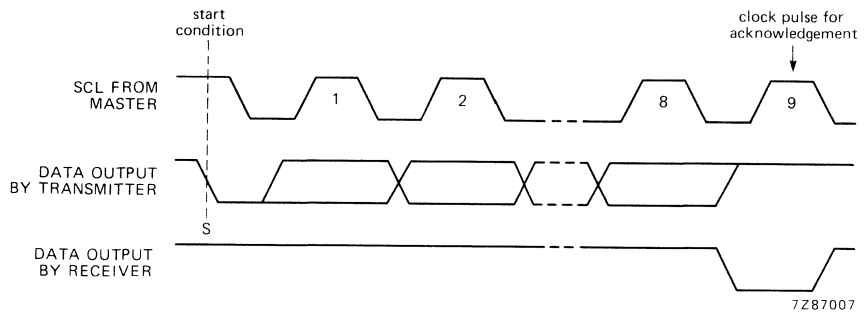


Fig.6 Acknowledgement on the I²C-bus.

Timing specifications

All the timing values are valid within the operating supply voltage and ambient temperature range and refer to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.

parameter	symbol	min.	typ.	max.	unit
SCL clock frequency	f_{SCL}	–	–	100	kHz
Tolerable spike width on bus	t_{SW}	–	–	100	ns
Bus free time	t_{BUF}	4.7	–	–	μs
Start condition set-up time	$t_{SU;STA}$	4.7	–	–	μs
Start condition hold time	$t_{HD;STA}$	4.0	–	–	μs
SCL LOW time	t_{LOW}	4.7	–	–	μs
SCL HIGH time	t_{HIGH}	4.0	–	–	μs
SCL and SDA rise time	t_r	–	–	1.0	μs
SCL and SDA fall time	t_f	–	–	0.3	μs
Data set-up time	$t_{SU;DAT}$	250	–	–	ns
Data hold time	$t_{HD;DAT}$	0	–	–	ns
SCL LOW to data out valid	$t_{VD;DAT}$	–	–	3.4	μs
Stop condition set-up time	$t_{SU;STO}$	4.0	–	–	μs

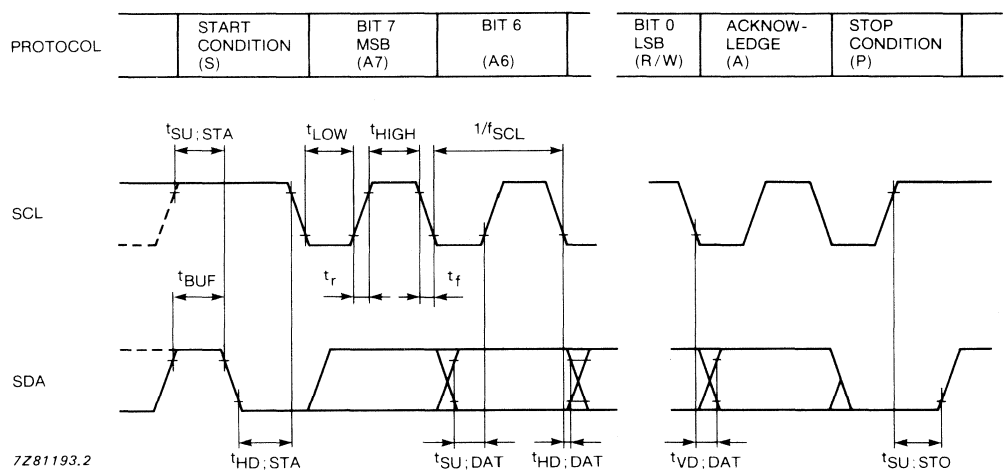


Fig.7 I²C-bus timing diagram.

ADDRESSING

Before any data is transmitted on the I²C-bus, the device which should respond is addressed first. The addressing is always done with the first byte transmitted after the start procedure.

Slave address

The clock/calendar acts as a slave receiver or slave transmitter. Therefore the clock signal SCL is only an input signal, but the data signal SDA is a bidirectional line. The clock calendar slave address is shown in Fig.8.

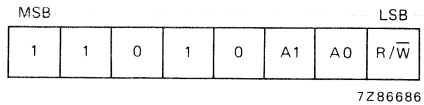


Fig.8 Slave address.

The subaddress bits A0 and A1 correspond to the two hardware address pins A0 and A1 which allows the device to have 1 of 4 different addresses.

Clock/calendar READ/WRITE cycles

The I²C-bus configuration for different clock/calendar READ and WRITE cycles is shown in Figs 9, 10 and 11.

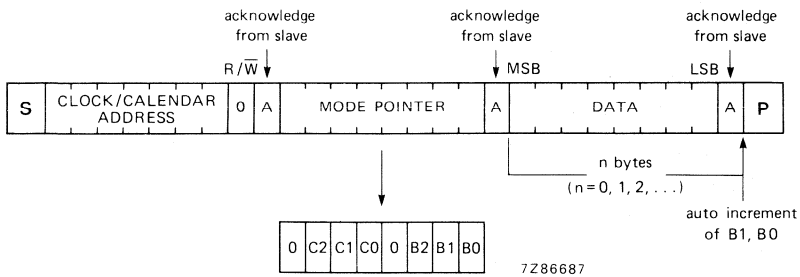


Fig.9 Master transmitter transmits to clock/calendar slave receiver.

The write cycle is used to set the time counter, the alarm register and the flags. The transmission of the clock/calendar address is followed by the MODE-POINTER-WORD which contains a CONTROL-nibble (Table 3) and an ADDRESS-nibble (Table 4). The ADDRESS-nible is valid only if the preceding CONTROL-nibble is set to EXECUTE ADDRESS. The third transmitted word contains the data to be written into the time counter or alarm register.

Table 3 CONTROL-nibble

	C2	C1	C0	function
0	0	0	0	execute address
0	0	0	1	read control/status flags
0	0	1	0	reset prescaler, including seconds counter; without carry for minute counter
0	0	1	1	time adjust, with carry for minute counter (see note)
0	1	0	0	reset NODA flag
0	1	0	1	set NODA flag
0	1	1	0	reset COMP flag

Note

If the seconds counter is below 30 there is no carry. This causes a time adjustment of max. −30 s. From the count 30 there is a carry which adjusts the time by max. + 30 s.

Table 4 ADDRESS-nibble

	B2	B1	B0	addressed to:
0	0	0	0	time counter hours
0	0	0	1	time counter minutes
0	0	1	0	time counter days
0	0	1	1	time counter months
0	1	0	0	alarm register hours
0	1	0	1	alarm register minutes
0	1	1	0	alarm register days
0	1	1	1	alarm register months

At the end of each data word the address bits B1, B0 will be incremented automatically provided the preceding CONTROL-nibble is set to EXECUTE ADDRESS. There is no carry to B2.

Table 5 shows the placement of the BCD upper and lower digits in the DATA byte for writing into the addressed part of the time counter and alarm register respectively.

Table 5 Placement of BCD digits in the DATA byte

MSB DATA LSB								
upper digit				lower digit				
UD	UC	UB	UA	LD	LC	LB	LA	addressed to:
X	X	D	D	D	D	D	D	hours
X	D	D	D	D	D	D	D	minutes
X	X	D	D	D	D	D	D	days
X	X	X	D	D	D	D	D	months

Where:

"X" is the don't care bit
"D" is the data bit
Acknowledgement response of the clock calendar as slave receiver is shown in Table 6.

ADDRESSING (continued)

Table 6 Slave receiver acknowledgement

mode pointer								acknowledge on byte		
								address	mode pointer	data
	C2	C1	C0		B2	B1	B0			
0	0	0	0	0	X	X	X	yes	yes	yes
0	0	0	0	1	X	X	X	yes	no	no
0	0	0	1	X	X	X	X	yes	yes	no
0	0	1	0	X	X	X	X	yes	yes	no
0	0	1	1	X	X	X	X	yes	yes	no
0	1	0	0	X	X	X	X	yes	yes	no
0	1	0	1	X	X	X	X	yes	yes	no
0	1	1	0	X	X	X	X	yes	yes	no
0	1	1	1	X	X	X	X	yes	no	no
1	X	X	X	X	X	X	X	yes	no	no

Where:

"X" is the don't care bit.

Table 7 Organization of the BCD digits in the DATA byte

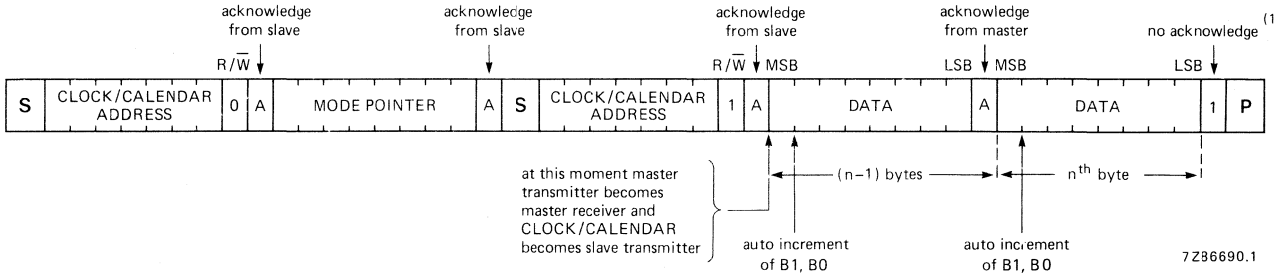
MSB DATA LSB								
upper digit				lower digit				
UD	UC	UB	UA	LD	LC	LB	LA	addressed to
0	0	D	D	D	D	D	D	hours
0	D	D	D	D	D	D	D	minutes
0	0	D	D	D	D	D	D	days
0	0	0	D	D	D	D	D	months
0	0	0	*	**	NODA	COMP	POWF	control/status flags

Where:

"D" is the data bit

* = minutes

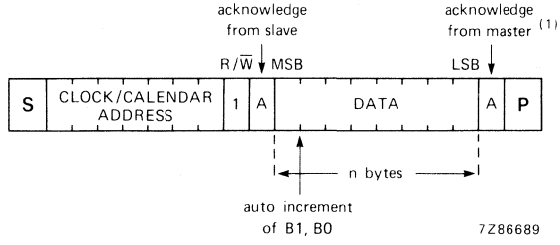
** = seconds.



(1) The master receiver must signal an end of data to the slave transmitter by *not* generating an acknowledge on the *last byte* that has been clocked out of the slave.

Fig.10 Master transmitter reads clock/calendar after setting mode pointer.

To read the addressed part of the time counter and alarm register, plus information from specified control/status flags, the BCD digits in the DATA byte are organized as shown in Table 7.



(1) The master receiver must signal an end of data to the slave transmitter by *not* generating an acknowledge on the *last byte* that has been clocked out of the slave.

Fig.11 Master reads clock/calendar immediately after first byte.

The status of the MODE-POINTER-WORD concerning the CONTROL-nibble remains unchanged until a write to MODE POINTER condition occurs.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	condition	symbol	min.	max.	unit
Supply voltage range					
pin 16 to pin 15		$V_{DD}-V_{SS1}$	−0.3	8.0	V
pin 16 to pin 8		$V_{DD}-V_{SS2}$	−0.3	8.0	V
Voltage input					
pins 4 and 5	note 1	V_I	$V_{SS2}-0.8$	$V_{DD}+0.8$	V
pins 6, 7, 13 and 14		V_I	$V_{SS1}-0.6$	$V_{DD}+0.6$	V
any other pin		V_I	$V_{SS2}-0.6$	$V_{DD}+0.6$	V
Input current		I_I	–	10	mA
Output current		I_O	–	10	mA
Power dissipation per output		P_O	–	100	mW
Total power dissipation		P_{tot}	–	200	mW
Operating ambient temperature range		T_{amb}	−40	+85	°C
Storage temperature range		T_{stg}	−55	+125	°C

Note to the Ratings

1. With input impedance of minimum 500 Ω.

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS devices').

CHARACTERISTICS

V_{SS2} = 0 V; T_{amb} = −40 to +85 °C unless otherwise specified. Typical values at T_{amb} = +25 °C

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage						
I²C interface		$V_{DD}-V_{SS2}$	2.5	5.0	6.0	V
clock	$t_{HD;DAT} \geqslant$ 300 ns	$V_{DD}-V_{SS1}$	1.1	1.5	$V_{DD}-V_{SS2}$	V
Supply current						
V_{SS1} (pin 15)	$V_{DD}-V_{SS1}$ = 1.5 V	$-I_{SS1}$	–	3	10	μA
	$V_{DD}-V_{SS1}$ = 5 V	$-I_{SS1}$	–	12	50	μA
V_{SS2} (pin 8)	$V_{DD}-V_{SS2}$ = 5 V; I_O = 0 all outputs	$-I_{SS2}$	–	–	50	μA
Input SCL; input/output SDA						
Input voltage LOW		V_{IL}	–	–	0.3 V_{DD}	V
Input voltage HIGH		V_{IH}	0.7 V_{DD}	–	–	V
Leakage current	$V_I = V_{SS2}$ or V_{DD}	$\|I_L\|$	–	–	1	μA
Input capacitance		C_I	–	–	7	pF
Inputs A0, A1, TEST						
Input voltage LOW		V_{IL}	–	–	0.2 V_{DD}	V
Input voltage HIGH		V_{IH}	0.7 V_{DD}	–	–	V
Input leakage current	$V_I = V_{SS2}$ or V_{DD}	$\pm I_{LI}$	–	–	250	nA
Inputs EXTPF, PFIN						
Input voltage LOW		V_{IL}	0	–	0.2 $V_{DD}-V_{SS1}$	V
Input voltage HIGH		V_{IH}	0.7 $V_{DD}-V_{SS1}$	–	–	V
Input leakage current	$V_I = V_{SS1}$ to V_{DD} T_{amb} = 25 °C;	$\pm I_{LI}$	–	–	1.0	μA
	$V_I = V_{SS1}$ to V_{DD}	$\pm I_{LI}$	–	–	0.1	μA

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Output SDA						
(n channel open drain)						
Output "ON"	I_O = 3 mA; $V_{DD}-V_{SS2}$ = 2.5 to to 6 V	V_{OL}	–	–	0.4	V
Leakage current	$V_{DD}-V_{SS2}$ = 6 V; V_O = 6 V	$\|I_L\|$	–	–	1	μA
Outputs						
Outputs SEC, MIN, COMP, FSET (normal buffer outputs)						
Output voltage LOW	$V_{DD}-V_{SS2}$ = 2.5 V; I_O = 0.3 mA	V_{OL}	–	–	0.4	V
	$V_{DD}-V_{SS2}$ = 4 to 6 V; I_O = 1.6 mA	V_{OL}	–	–	0.4	V
Output voltage HIGH	$V_{DD}-V_{SS2}$ = 2.5 V; $-I_O$ = 0.1 mA	V_{OH}	$V_{DD}-0.4$	–	–	V
	$V_{DD}-V_{SS2}$ = 4 to 6 V; $-I_O$ = 0.5 mA	V_{OH}	$V_{DD}-0.4$	–	–	V
Internal threshold voltage						
Power failure detection		V_{TH1}	1	1.2	1.4	V
Power "ON" reset		V_{TH2}	1.5	2.0	2.5	V
Rise and fall times of input signals						
Input EXTPF		t_r, t_f	–	–	1	μs
Input PFIN		t_r, t_f	–	–	∞	μs
Input signals except EXTPF and PFIN between V_{IL} and V_{IH} levels						
rise time		t_r	–	–	1	μs
fall time		t_f	–	–	0.3	μs

parameter	conditions	symbol	min.	typ.	max.	unit
Oscillator						
Integrated oscillator capacitance		C_{OUT}	–	40	–	pF
Oscillator feedback resistance		R_f	–	3	–	MΩ
Oscillator stability	$\Delta(V_{DD}-V_{SS1})$ = 100 mV; at $V_{DD}-V_{SS1}$ = 1.55 V; T_{amb} = 25 °C	f/f_{osc}	–	2×10^{-7}	–	–
Quartz crystal parameters	f = 32.768 kHz					
Series resistance		R_S	–	–	40	kΩ
Parallel capacitance		C_L	–	10	–	pF
Trimmer capacitance		C_T	5	–	25	pF

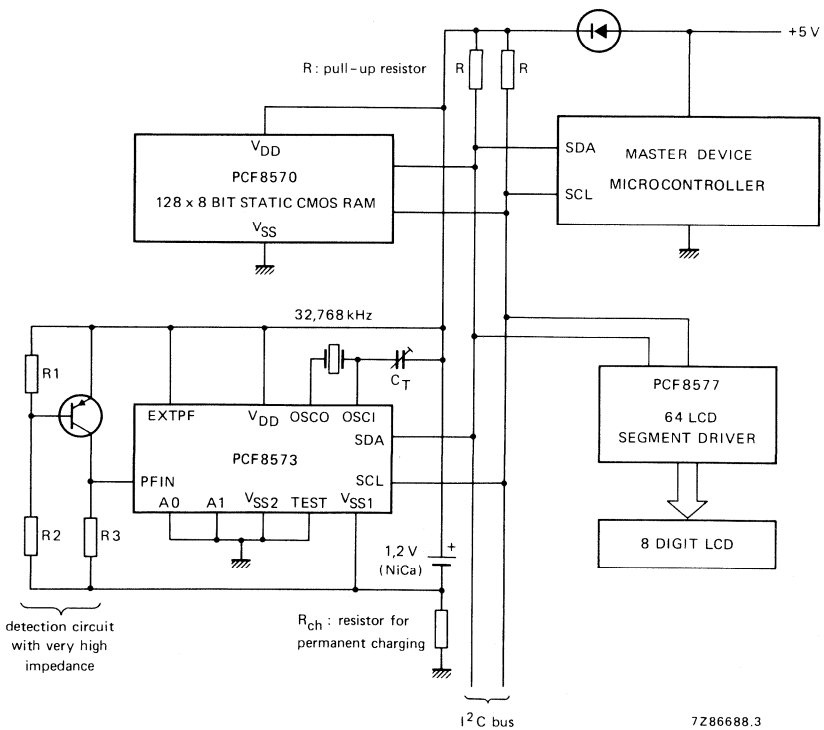


Fig.12 Application example of the PCF8573 clock/calendar.

APPLICATION INFORMATION

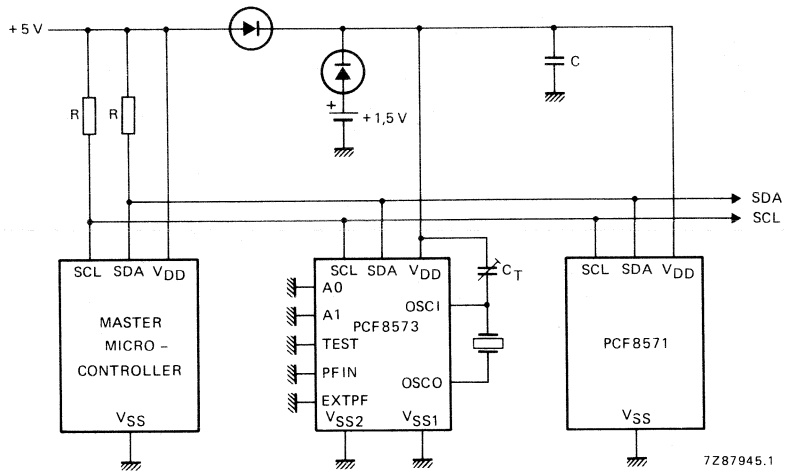


Fig.13 Application example of the PCF8573 with common V_{SS1} and V_{SS2} supply.

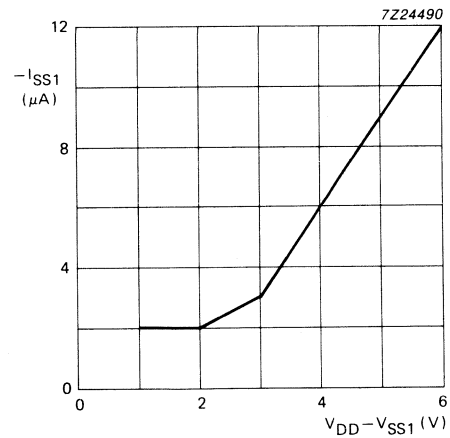


Fig.14 Typical supply current ($-I_{SS1}$) as a function of clock supply voltage ($V_{DD}-V_{SS1}$) at $T_{amb} = -40$ to $+85$ °C.

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

Remote 8-bit I/O expander for I²C-bus | PCF8574 / PCF8574A

GENERAL DESCRIPTION

The PCF8574 is a single-chip silicon gate CMOS circuit. It provides remote I/O expansion for the MAB8400 and PCF84CXX microcontroller families via the two-line serial bidirectional bus (I²C). It can also interface microcomputers without a serial interface to the I²C-bus (as a slave function only). The device consists of an 8-bit quasi-bidirectional port and an I²C interface.
The PCF8574 has low current consumption and includes latched outputs with high current drive capability for directly driving LEDs. It also possesses an interrupt line (INT) which is connected to the interrupt logic of the microcomputer on the I²C-bus. By sending an interrupt signal on this line, the remote I/O can inform the microcomputer if there is incoming data on its ports without having to communicate via the I²C-bus. This means that the PCF8574 can remain a simple slave device.

The PCF8574 and the PCF8574A versions differ only in their slave address as shown in Fig.9.

Features

- Operating supply voltage 2.5 V to 6 V
- Low stand-by current consumption max. 10 μA
- Bidirectional expander
- Open drain interrupt output
- 8-bit remote I/O port for the I²C-bus
- Peripheral for the MAB8400 and PCF84CXX microcontroller families
- Latched outputs with high current drive capability for directly driving LEDs
- Address by 3 hardware address pins for use of up to 8 devices (up to 16 with PCF8574A)

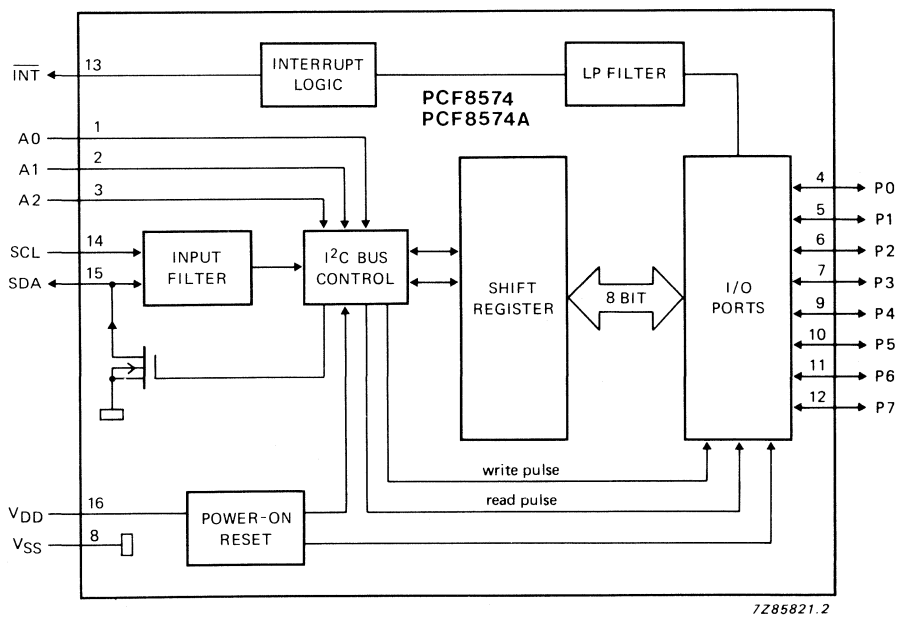


Fig.1 Block diagram.

PACKAGE OUTLINES

PCF8574P, PCF8574AP: 16-lead DIL; plastic (SOT38).
PCF8574T, PCF8574AT: 16-lead mini-pack; plastic (SO16L; SOT162A).

PINNING

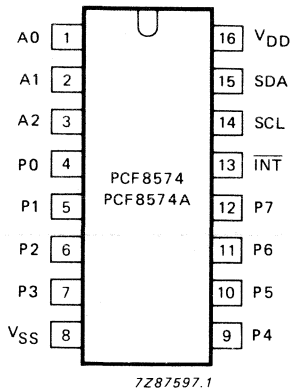


Fig.2 Pinning diagram.

1 to 3	A0 to A2	address inputs
4 to 7 9 to 12	P0 to P3 P4 to P7	8-bit quasi-bidirectional I/O port
8	V_{SS}	negative supply
13	$\overline{INT}$	interrupt output
14	SCL	serial clock line
15	SDA	serial data line
16	V_{DD}	positive supply

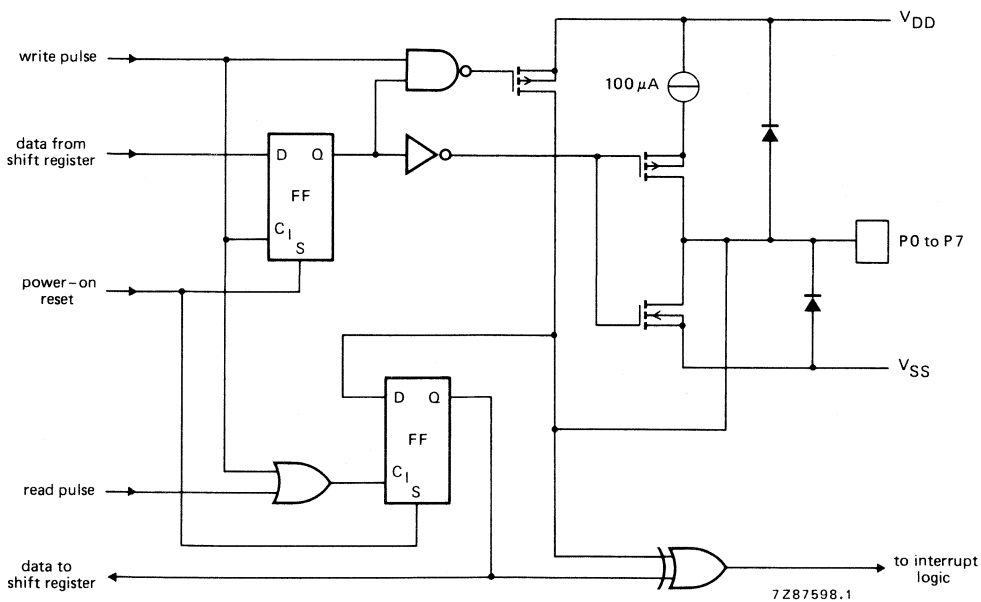


Fig.3 Simplified schematic diagram of each port.

CHARACTERISTICS OF THE I²C-BUS

The I²C-bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

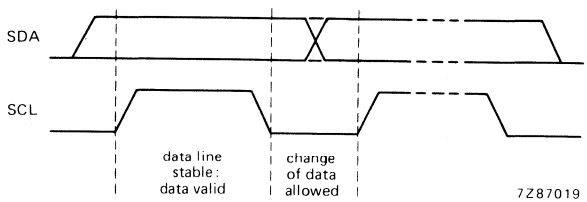


Fig.4 Bit transfer.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

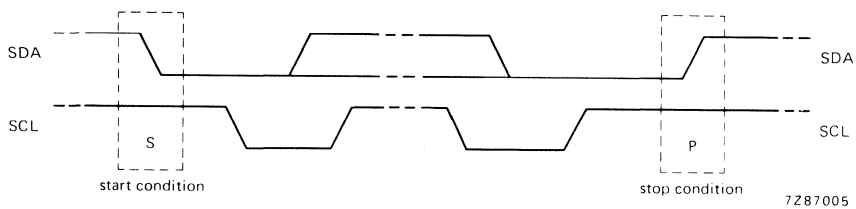


Fig.5 Definition of start and stop conditions.

CHARACTERISTICS OF THE I²C-BUS (continued)

System configuration

A device generating a message is a "transmitter", a device receiving a message is the "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

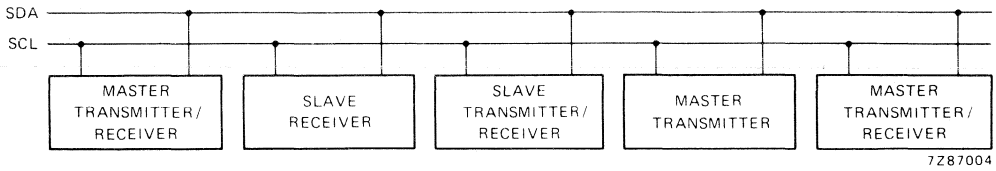


Fig.6 System configuration.

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set up and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

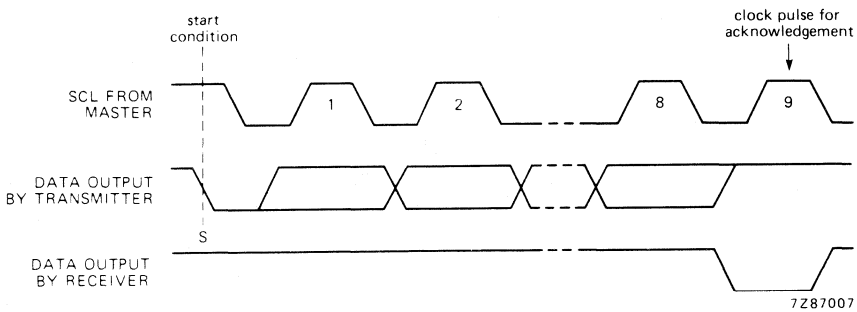


Fig.7 Acknowledgement on the I²C-bus.

Timing specifications

All the timing values are valid within the operating supply voltage and ambient temperature range and refer to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.

parameter	symbol	min.	typ.	max.	unit
SCL clock frequency	f_{SCL}	–	–	100	kHz
Tolerable spike width on bus	t_{SW}	–	–	100	ns
Bus free time	t_{BUF}	4.7	–	–	μs
Start condition set-up time	$t_{SU;STA}$	4.7	–	–	μs
Start condition hold time	$t_{HD;STA}$	4.0	–	–	μs
SCL LOW time	t_{LOW}	4.7	–	–	μs
SCL HIGH time	t_{HIGH}	4.0	–	–	μs
SCL and SDA rise time	t_r	–	–	1.0	μs
SCL and SDA fall time	t_f	–	–	0.3	μs
Data set-up time	$t_{SU;DAT}$	250	–	–	ns
Data hold time	$t_{HD;DAT}$	0	–	–	ns
SCL LOW to data out valid	$t_{VD;DAT}$	–	–	3.4	μs
Stop condition set-up time	$t_{SU;STO}$	4.0	–	–	μs

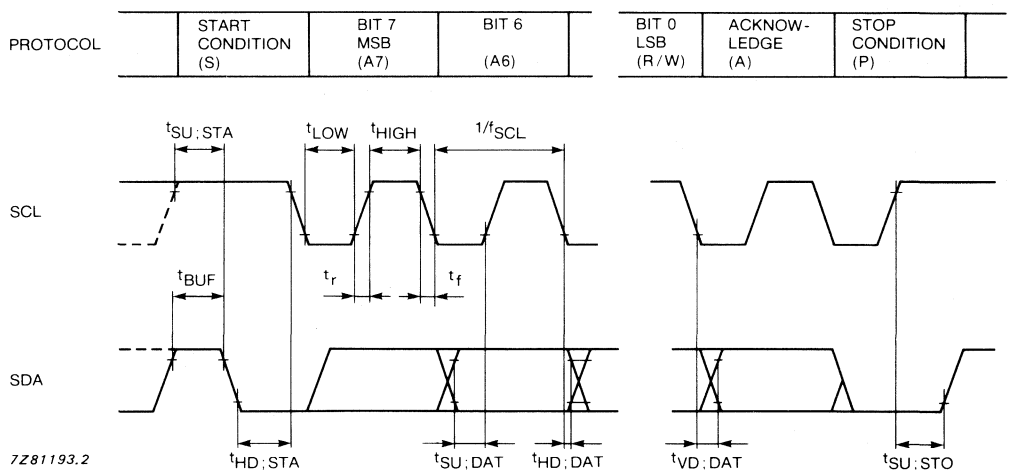
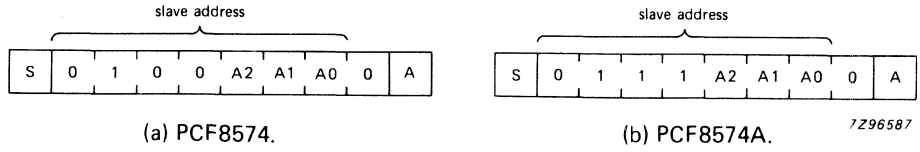


Fig.8 I²C-bus timing diagram.

FUNCTIONAL DESCRIPTION

Addressing (see Figs 9, 10 and 11)



(a) PCF8574. (b) PCF8574A.

Fig.9 PCF8574 and PCF8574A slave addresses.

Each bit of the PCF8574 I/O port can be independently used as an input or an output. Input data is transferred from the port to the microcomputer by the READ mode. Output data is transmitted to the port by the WRITE mode.

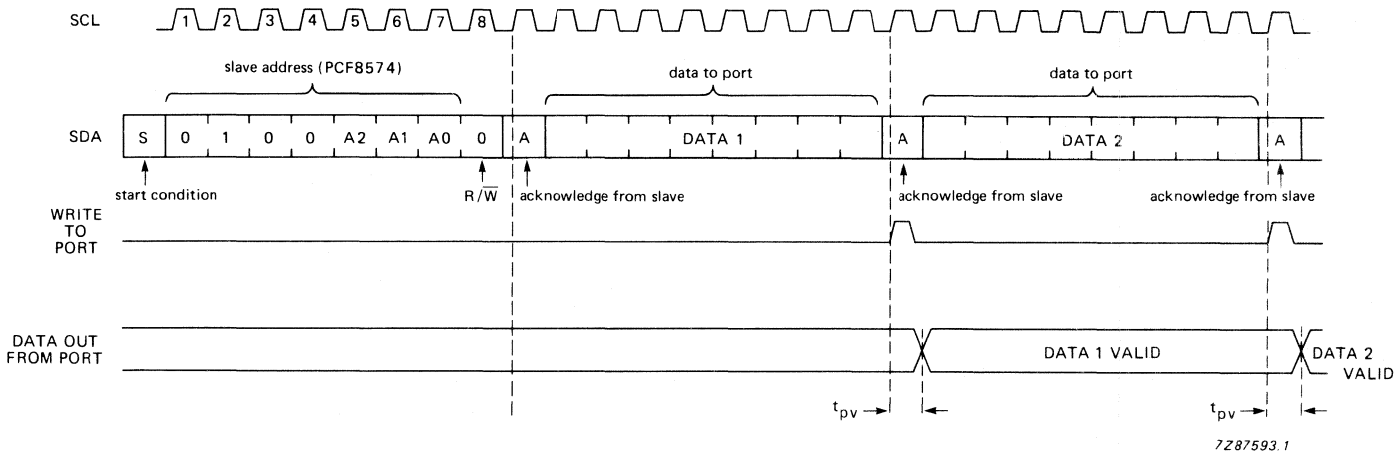


Fig.10 WRITE mode (output port).

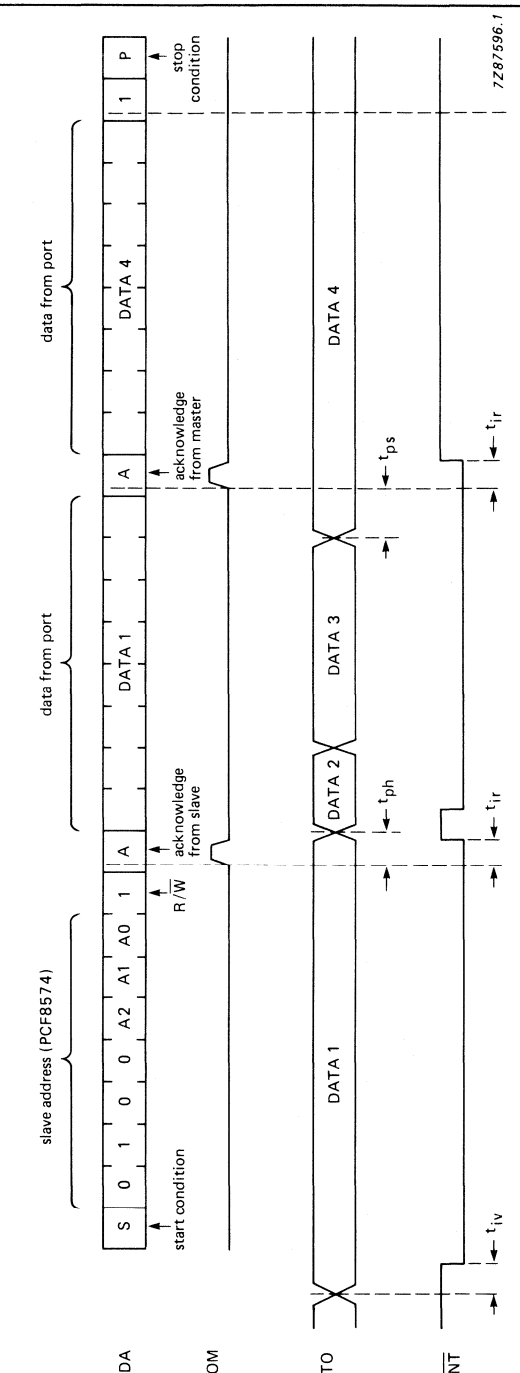


Fig.11 READ mode (input port).

Note

A LOW-to-HIGH transition of SDA, while SCL is HIGH is defined as the stop condition (P). Transfer of data can be stopped at any moment by a stop condition. When this occurs, data present at the last acknowledge phase is valid (output mode). Input data is lost.

Interrupt (see Figs 12 and 13)

The PCF8574/PCF8574A provides an open drain output ($\overline{INT}$) which can be fed to a corresponding input of the microcomputer. This gives these chips a type of master function which can initiate an action elsewhere in the system.

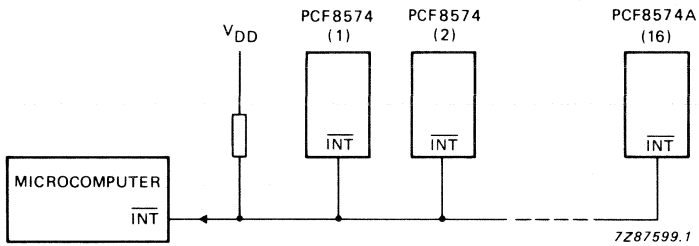


Fig.12 Application of multiple PCF8574s with interrupt.

An interrupt is generated by any rising or falling edge of the port inputs in the input mode. After time t_{iv} the signal $\overline{INT}$ is valid.
Resetting and reactivating the interrupt circuit is achieved when data on the port is changed to the original setting or data is read from or written to the port which has generated the interrupt.
Resetting occurs as follows:

- In the READ mode at the acknowledge bit after the rising edge of the SCL signal.
- In the WRITE mode at the acknowledge bit after the HIGH-to-LOW transition of the SCL signal.

Each change of the ports after the resettings will be detected and after the next rising clock edge, will be transmitted as $\overline{INT}$.
Reading from or writing to another device does not affect the interrupt circuit.

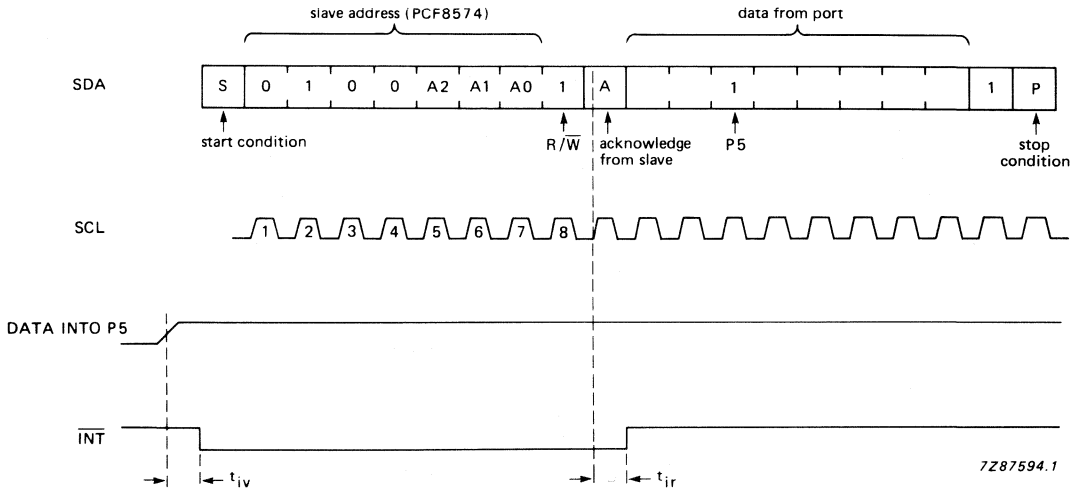


Fig.13 Interrupt generated by a change of input to port P5.

FUNCTIONAL DESCRIPTION (continued)

Quasi-bidirectional I/O ports (see Fig.14)

A quasi-bidirectional port can be used as an input or output without the use of a control signal for data direction. At power-on the ports are HIGH. In this mode only a current source to V_{DD} is active. An additional strong pull-up to V_{DD} allows fast rising edges into heavily loaded outputs. These devices turn on when an output is written HIGH, and are switched off by the negative edge of SCL. The ports should be HIGH before being used as inputs.

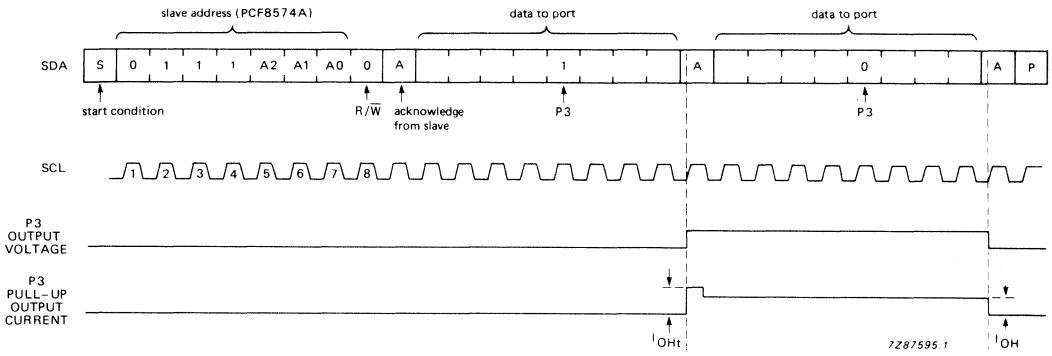


Fig.14 Transient pull-up current I_{OHt} while P3 changes from LOW-to-HIGH and back to LOW.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage range	V_{DD}	−0.5	+ 7.0	V
Input voltage range	V_I	V_{SS} −0.5	V_{DD} + 0.5	V
DC input current	$\pm I_I$	–	20	mA
DC output current	$\pm I_O$	–	25	mA
V_{DD} or V_{SS} current	$\pm I_{DD}$; $\pm I_{SS}$	–	100	mA
Total power dissipation	P_{tot}	–	400	mW
Power dissipation per output	P_O	–	100	mW
Operating ambient temperature range	T_{amb}	−40	+ 85	°C
Storage temperature range	T_{stg}	−65	+ 150	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

CHARACTERISTICS

V_{DD} = 2.5 to 6 V; V_{SS} = 0 V; T_{amb} = −40 to + 85 °C unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage		V_{DD}	2.5	–	6.0	V
Supply current	V_{DD} = 6 V; no load; $V_I = V_{DD}$ or V_{SS}					
operating	f_{SCL} = 100 kHz	I_{DD}	–	40	100	μA
standby		I_{DDO}	–	2.5	10	μA
Power-on reset level	note 1	V_{POR}	–	1.3	2.4	V
Input SCL; input/output SDA						
Input voltage LOW		V_{IL}	−0.5	–	$0.3V_{DD}$	V
Input voltage HIGH		V_{IH}	$0.7V_{DD}$	–	V_{DD} + 0.5	V
Output current LOW	V_{OL} = 0.4 V	I_{OL}	3	–	–	mA
Leakage current	$V_I = V_{DD}$ or V_{SS}	$\|I_L\|$	–	–	1	μA
Input capacitance (SCL, SDA)	$V_I = V_{SS}$	C_I	–	–	7	pF
I/O ports						
Input voltage LOW		V_{IL}	−0.5	–	$0.3V_{DD}$	V
Input voltage HIGH		V_{IH}	$0.7V_{DD}$	–	V_{DD} + 0.5	V
Maximum allowed input current through protection diode	$V_I \geqslant V_{DD}$ or $\leqslant V_{SS}$	$\pm I_{IHL}$	–	–	400	μA
Output current LOW	V_{OL} = 1 V; V_{DD} = 5 V	I_{OL}	10	25	–	mA
Output current HIGH	$V_{OH} = V_{SS}$	I_{OH}	30	–	300	μA
Transient pull-up current HIGH during acknowledge (see Fig.14)	$V_{OH} = V_{SS}$; V_{DD} = 2.5 V	$-I_{OHt}$	–	1	–	mA
Input/Output capacitance		$C_{I/O}$	–	–	10	pF
Port timing (see Figs 10 and 11)	$C_L = \leqslant 100$ pF					
Output data valid		t_{pv}	–	–	4	μs
Input data set-up		t_{ps}	0	–	–	μs
Input data hold		t_{ph}	4	–	–	μs

parameter	conditions	symbol	min.	typ.	max.	unit
Interrupt $\overline{INT}$						
Output current LOW	V_{OL} = 0.4 V	I_{OL}	1.6	–	–	mA
Leakage current	$V_I = V_{DD}$ or V_{SS}	$\|I_L\|$	–	–	1	μA
$\overline{INT}$ timing (see Figs 11 and 13)	$C_L \leqslant 100$ pF					
Input data valid		t_{iv}	–	–	4	μs
Reset delay		t_{ir}	–	–	4	μs
Select inputs A0, A1, A2						
Input voltage LOW		V_{IL}	−0.5	–	$0.3V_{DD}$	V
Input voltage HIGH		V_{IH}	$0.7V_{DD}$	–	V_{DD} + 0.5	V
Input leakage current	pin at V_{DD} or V_{SS}	$\|I_L\|$	–	–	250	nA

Note to the characteristics

1. The power-on reset circuit resets the I²C-bus logic with $V_{DD} < V_{POR}$ and sets all ports to logic 1 (with current source to V_{DD}).

Universal LCD driver for low multiplex rates PCF8576

GENERAL DESCRIPTION

The PCF8576 is a peripheral device which interfaces to almost any liquid crystal display (LCD) having low multiplex rates. It generates the drive signals for any static or multiplexed LCD containing up to four backplanes and up to 40 segments and can easily be cascaded for larger LCD applications. The PCF8576 is compatible with most microprocessors/microcontrollers and communicates via a two-line bidirectional bus (I²C). Communication overheads are minimized by a display RAM with auto-incremented addressing, by hardware subaddressing and by display memory switching (static and duplex drive modes).

Features

- Single-chip LCD controller/driver
- Selectable backplane drive configuration: static or 2/3/4 backplane multiplexing
- Selectable display bias configuration: static, 1/2 or 1/3
- Internal LCD bias generation with voltage-follower buffers
- 40 segment drives: up to twenty 8-segment numeric characters; up to ten 15-segment alphanumeric characters; or any graphics of up to 160 elements
- 40 x 4-bit RAM for display data storage
- Auto-incremented display data loading across device subaddress boundaries
- Display memory bank switching in static and duplex drive modes
- Versatile blinking modes
- LCD and logic supplies may be separated
- Wide power supply range: from 2 V for low-threshold LCDs and up to 9 V for guest-host LCDs and high-threshold (automobile) twisted nematic LCDs
- Low power consumption
- Power-saving mode for extremely low power consumption in battery-operated and telephone applications
- I²C-bus interface
- TTL/CMOS compatible
- Compatible with any 4-bit, 8-bit or 16-bit microprocessors/microcontrollers
- May be cascaded for large LCD applications (up to 2560 segments possible)
- Cascadable with the 24-segment LCD driver PCF8566
- Optimized pinning for single plane wiring in both single and multiple PCF8576 applications
- Space-saving 56-lead plastic mini-pack (VSO56) or 64-lead tape-automated-bonding (TAB) module (SOT267A)
- Very low external component count (at most one resistor, even in multiple device applications)
- Compatible with chip-on-glass technology
- Manufactured in silicon gate CMOS process

PACKAGE OUTLINES

PCF8576T: 56-lead mini-pack; plastic (VSO56; SOT190).
PCF8576U: uncased chip in tray.
PCF8576U/10: chip-on-film frame carrier (FFC).
PCF8576V: 64-lead tape-automated-bonding module (SOT267A).

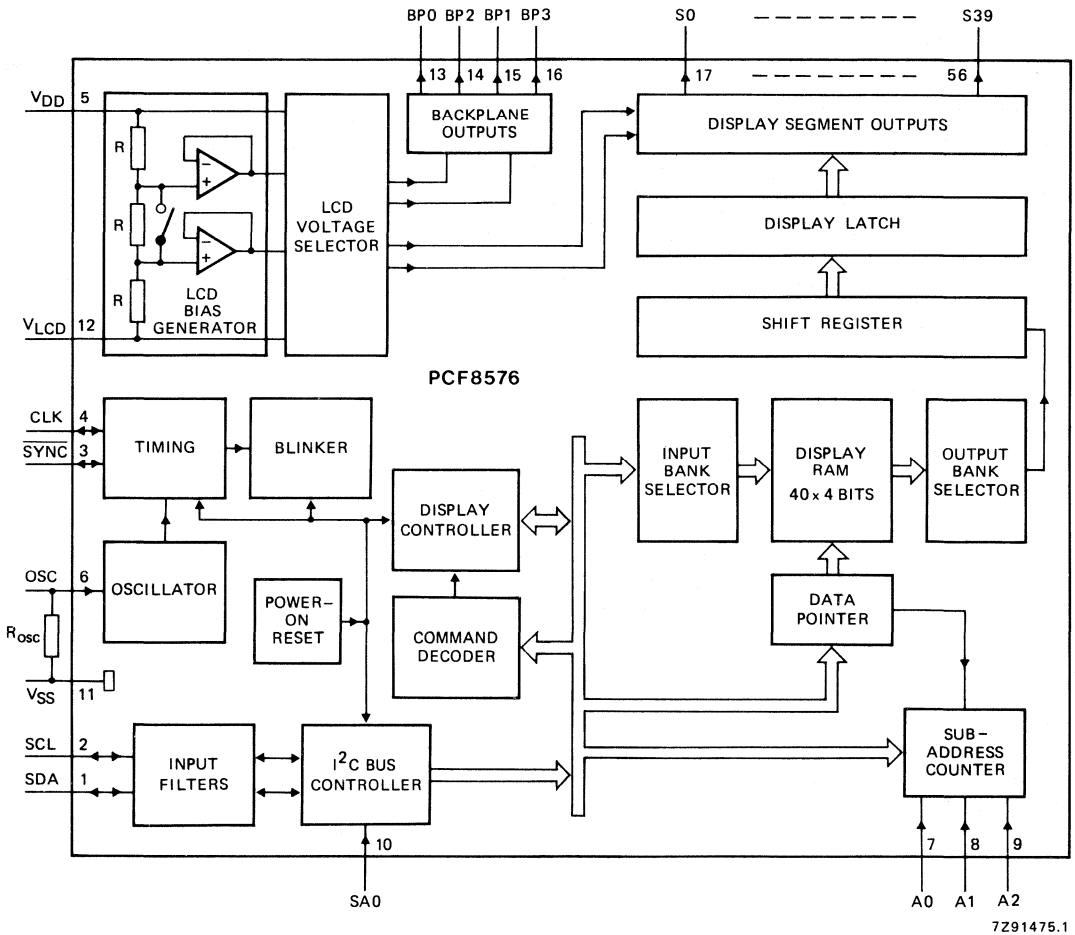


Fig.1 Block diagram; VSO56; SOT190.

PINNING

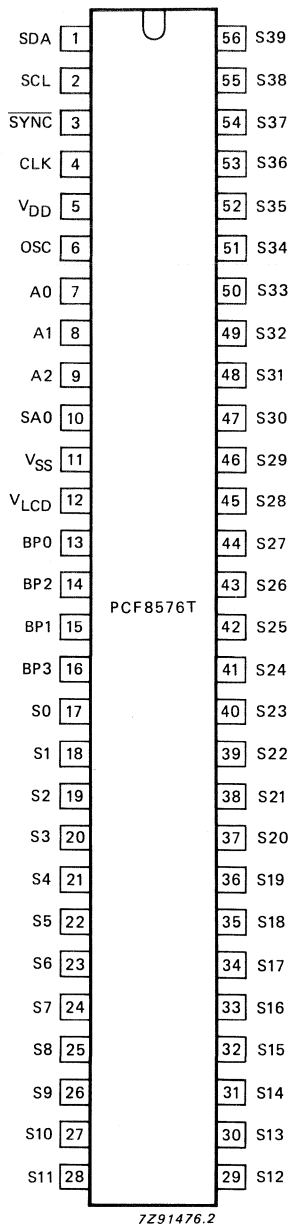
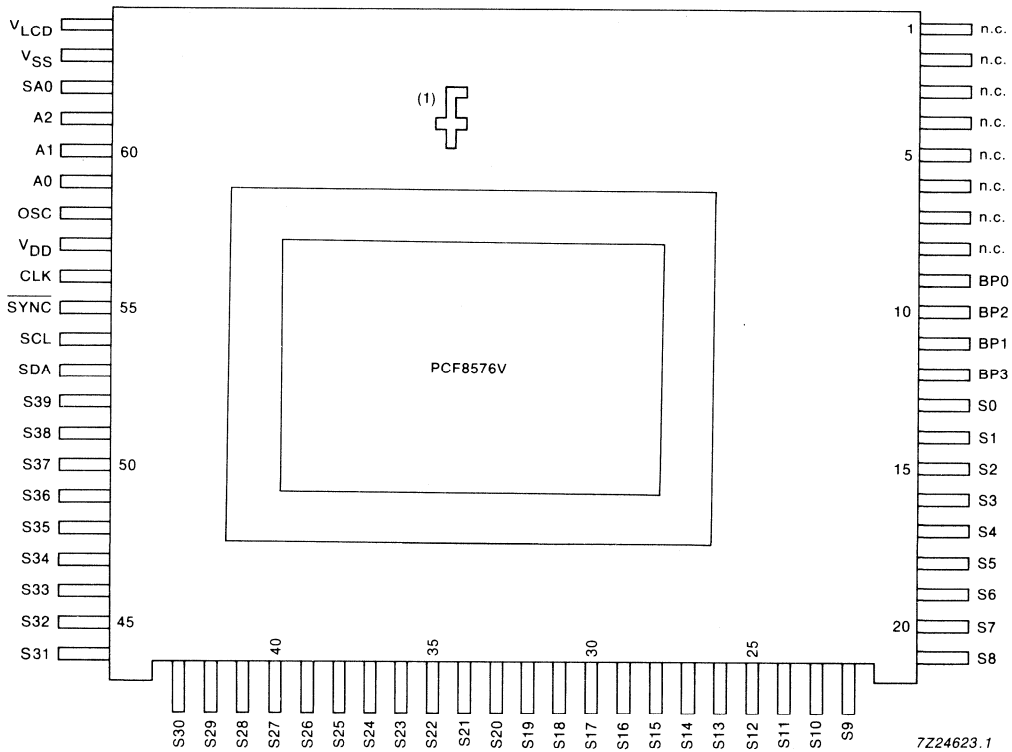


Fig.2(a) Pinning diagram: VSO56; SOT190.

PINNING (continued)



(1) Orientation mark.

Fig.2(b) Pinning diagram; SOT267A.

mnemonic	pin no.		description
	SOT190	SOT267A	
SDA	1	53	I²C-bus serial data line
SCL	2	54	I²C-bus serial clock line
$\overline{SYNC}$	3	55	cascade synchronization input
CLK	4	56	external clock input
V_{DD}	5	57	positive supply voltage
OSC	6	58	oscillator input
A0 to A2	7 - 9	59 - 61	I²C-bus subaddress inputs
SA0	10	62	I²C-bus slave address input (bit 0)
V_{SS}	11	63	ground (logic)
V_{LCD}	12	64	LCD supply voltage
n.c.		1 - 8	not connected
BP0 to BP3	13 - 16	9 - 12	LCD backplane outputs
S0 to S39	17 - 56	13 - 52	LCD segment outputs

FUNCTIONAL DESCRIPTION

The PCF8576 is a versatile peripheral device designed to interface any microprocessor/microcontroller to a wide variety of LCDs. It can directly drive any static or multiplexed LCD containing up to four backplanes and up to 40 segments. The display configurations possible with the PCF8576 depend on the number of active backplane outputs required; a selection of display configurations is given in Table 1.

Table 1 Selection of display configurations

active backplane outputs	no. of segments	7-segment numeric	14-segment alphanumeric	dot matrix
4	160	20 digits + 20 indicator symbols	10 characters + 20 indicator symbols	160 dots (4 x 40)
3	120	15 digits + 15 indicator symbols	8 characters + 8 indicator symbols	120 dots (3 x 40)
2	80	10 digits + 10 indicator symbols	5 characters + 10 indicator symbols	80 dots (2 x 40)
1	40	5 digits + 5 indicator symbols	2 characters + 12 indicator symbols	40 dots

All of the display configurations given in Table 1 can be implemented in the typical system shown in Fig.3. The host microprocessor/microcontroller maintains the 2-line I²C-bus communication channel with the PCF8576. A resistor connected between OSC (pin 6) and V_{SS} (pin 11) controls the device clock frequency. The appropriate biasing voltages for the multiplexed LCD waveforms are generated internally. The only other connections required to complete the system are to the power supplies (V_{DD}, V_{SS} and V_{LCD}) and to the LCD panel chosen for the application.

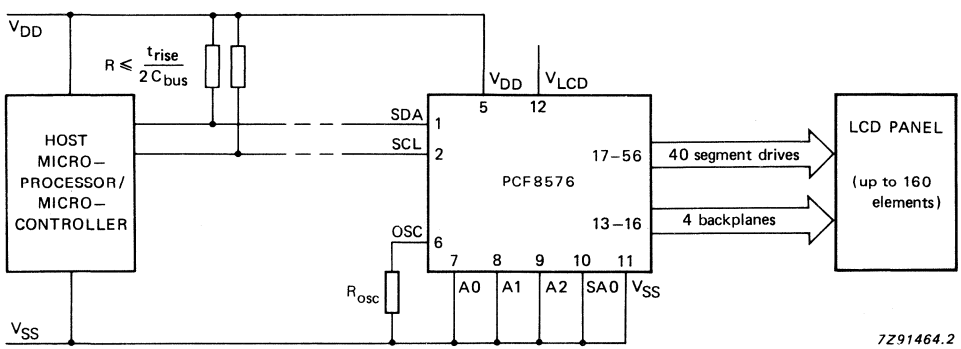


Fig.3 Typical system configuration.

Power-on reset

At power-on the PCF8576 resets to a defined starting condition as follows:

1. All backplane outputs are set to V_{DD}.
2. All segment outputs are set to V_{DD}.
3. The drive mode '1 : 4 multiplex with 1/3 bias' is selected.
4. Blinking is switched off.
5. Input and output bank selectors are reset (as defined in Table 5).
6. The I²C-bus interface is initialized.
7. The data pointer and the subaddress counter are cleared.

Data transfers on the I²C-bus should be avoided for 1 ms following power-on to allow completion of the reset action.

LCD bias generator

The full-scale LCD voltage (V_{op}) is obtained from $V_{DD} - V_{LCD}$. The LCD voltage may be temperature compensated externally through the V_{LCD} supply to pin 12. Fractional LCD biasing voltages are obtained from an internal voltage divider of three series resistors connected between V_{DD} and V_{LCD}. The centre resistor can be switched out of circuit to provide a ½ bias voltage level for the 1 : 2 multiplex configuration.

LCD voltage selector

The LCD voltage selector coordinates the multiplexing of the LCD according to the selected LCD drive configuration. The operation of the voltage selector is controlled by MODE SET commands from the command decoder. The biasing configurations that apply to the preferred modes of operation, together with the biasing characteristics as functions of $V_{op} = V_{DD} - V_{LCD}$ and the resulting discrimination ratios (D), are given in Table 2.

Table 2 Preferred LCD drive modes: summary of characteristics

LCD drive mode	LCD bias configuration	$\frac{V_{off\ (rms)}}{V_{op}}$	$\frac{V_{on\ (rms)}}{V_{op}}$	$D = \frac{V_{on\ (rms)}}{V_{off\ (rms)}}$
static (1 BP)	static (2 levels)	0	1	∞
1 : 2 MUX (2 BP)	1/2 (3 levels)	$\sqrt{2}/4 = 0.354$	$\sqrt{10}/4 = 0.791$	$\sqrt{5} = 2.236$
1 : 2 MUX (2 BP)	1/3 (4 levels)	$1/3 = 0.333$	$\sqrt{5}/3 = 0.745$	$\sqrt{5} = 2.236$
1 : 3 MUX (3 BP)	1/3 (4 levels)	$1/3 = 0.333$	$\sqrt{33}/9 = 0.638$	$\sqrt{33}/3 = 1.915$
1 : 4 MUX (4 BP)	1/3 (4 levels)	$1/3 = 0.333$	$\sqrt{3}/3 = 0.577$	$\sqrt{3} = 1.732$

LCD voltage selector (continued)

A practical value for V_{op} is determined by equating $V_{off\ (rms)}$ with a defined LCD threshold voltage (V_{th}), typically when the LCD exhibits approximately 10% contrast. In the static drive mode a suitable choice is $V_{op} \gtrapprox 3\ V_{th}$.
Multiplex drive ratios of 1 : 3 and 1 : 4 with 1/2 bias are possible but the discrimination and hence the contrast ratios are smaller ($\sqrt{3} = 1.732$ for 1: 3 multiplex or $\sqrt{21}/3 = 1.528$ for 1 : 4 multiplex).
The advantage of these modes is a reduction of the LCD full scale voltage V_{op} as follows:

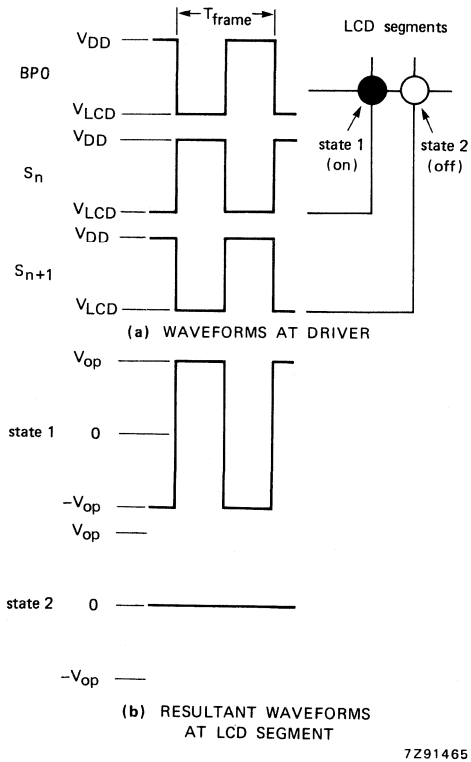
1 : 3 multiplex (1/2 bias) : $V_{op} = \sqrt{6}\ V_{off\ (rms)} = 2.449\ V_{off\ (rms)}$

1 : 4 multiplex (1/2 bias) : $V_{op} = 4\sqrt{3}/3\ V_{off\ (rms)} = 2.309\ V_{off\ (rms)}$

These compare with $V_{op} = 3\ V_{off\ (rms)}$ when 1/3 bias is used.

LCD drive mode waveforms

The static LCD drive mode is used when a single backplane is provided in the LCD. Backplane and segment drive waveforms for this mode are shown in Fig.4.



At any instant (t):

$V_{state\ 1}(t) = V_{S_n}(t) - V_{BP0}(t)$

$V_{on\ (rms)} = V_{op}$

$V_{state\ 2}(t) = V_{S_{n+1}}(t) - V_{BP0}(t)$

$V_{off\ (rms)} = 0\ V$

Fig.4 Static drive mode waveforms: $V_{op} = V_{DD} - V_{LCD}$.

When two backplanes are provided in the LCD the 1 : 2 multiplex drive mode applies. The PCF8576 allows use of 1/2 or 1/3 bias in this mode as shown in Figs 5 and 6.

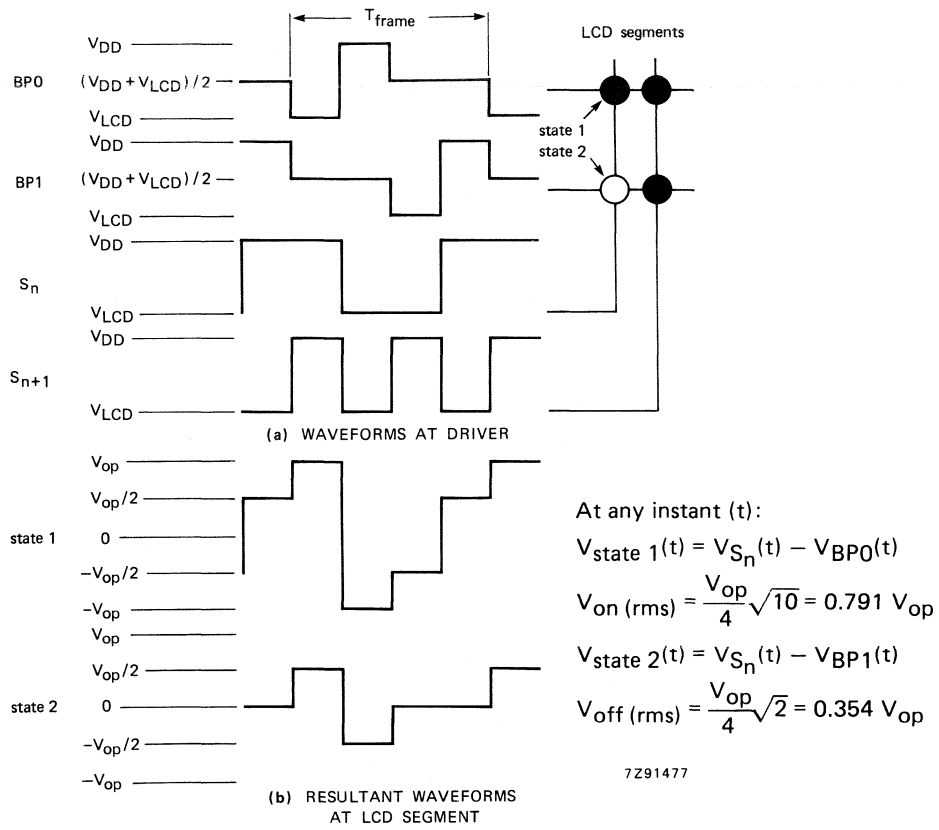


Fig.5 Waveforms for 1 : 2 multiplex drive mode with 1/2 bias: $V_{op} = V_{DD} - V_{LCD}$.

LCD drive mode waveforms (continued)

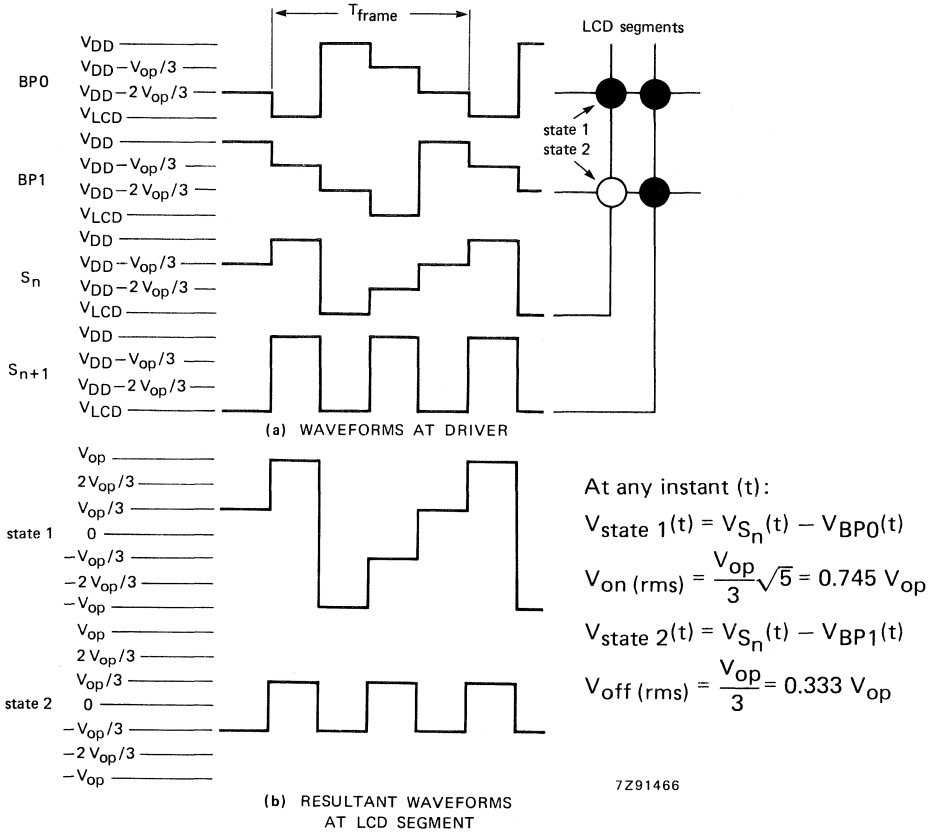


Fig.6 Waveforms for 1 : 2 multiplex drive mode with 1/3 bias: $V_{op} = V_{DD} - V_{LCD}$.

The backplane and segment drive waveform for the 1 : 3 multiplex drive mode (three LCD backplanes) and for the 1 : 4 multiplex drive mode (four LCD backplanes) are shown in Figs 7 and 8 respectively.

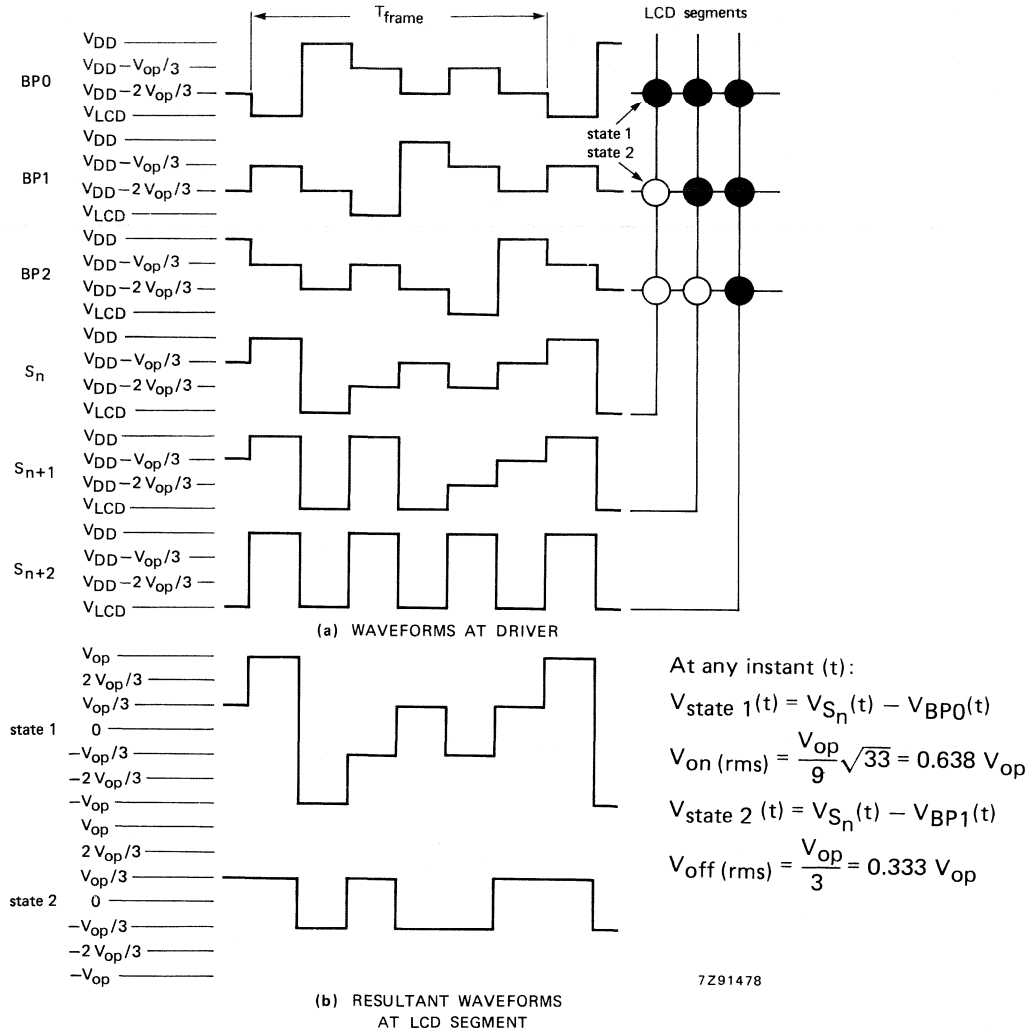
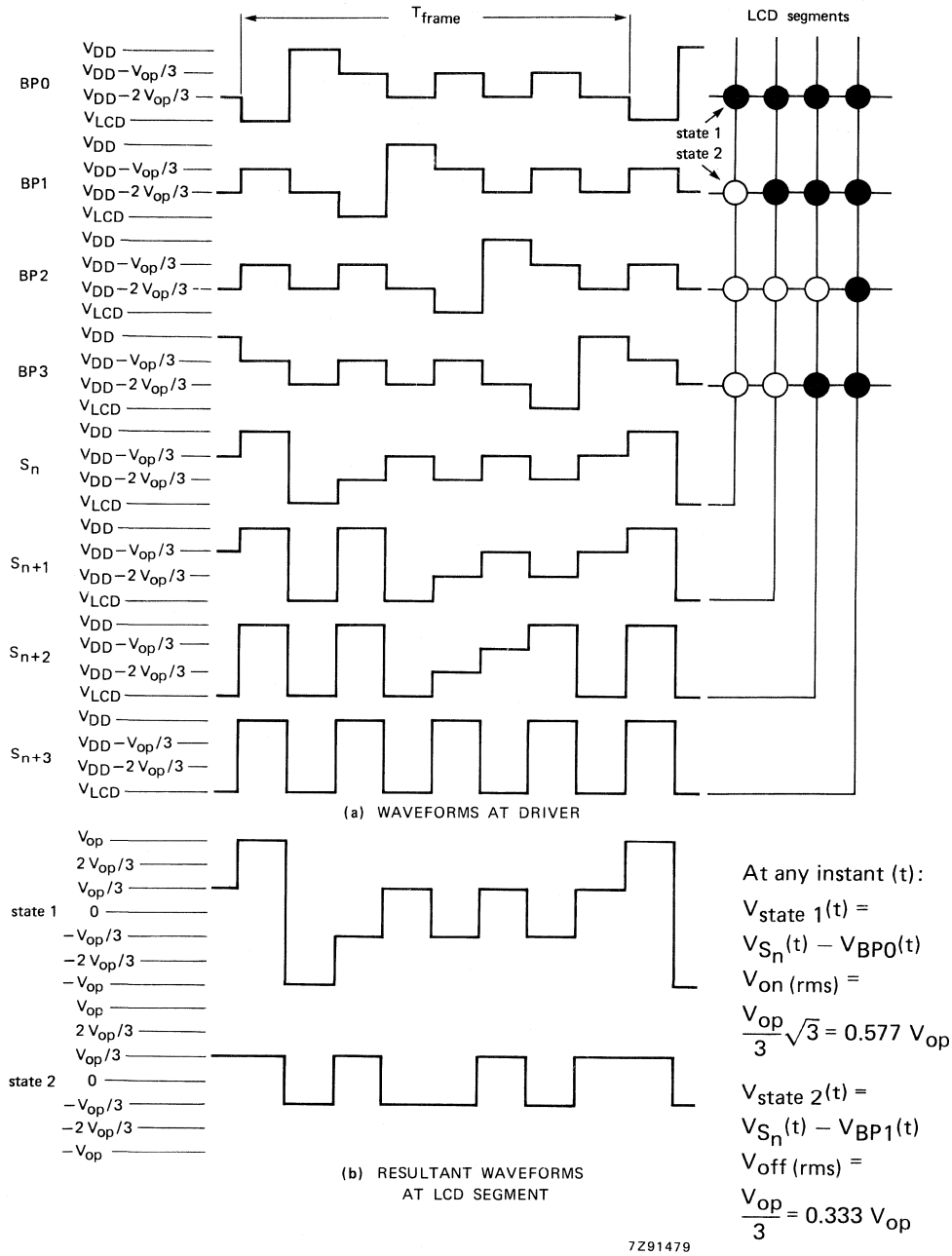


Fig.7 Waveforms for 1 : 3 multiplex drive mode: $V_{op} = V_{DD} - V_{LCD}$.

LCD drive mode waveforms (continued)



At any instant (t):

$V_{state\ 1}(t) = V_{S_n}(t) - V_{BP0}(t)$

$V_{on\ (rms)} = \frac{V_{op}}{3}\sqrt{3} = 0.577\ V_{op}$

$V_{state\ 2}(t) = V_{S_n}(t) - V_{BP1}(t)$

$V_{off\ (rms)} = \frac{V_{op}}{3} = 0.333\ V_{op}$

Fig.8 Waveforms for 1 : 4 multiplex drive mode: $V_{op} = V_{DD} - V_{LCD}$.

Oscillator

Internal clock

The internal logic and the LCD drive signals of the PCF8576 are timed either by the built-in oscillator or from an external clock. When the internal oscillator is used, frequency control is performed by a single resistor connected between OSC (pin 6) and V_{SS} (pin 11) as shown in Fig.9. In this application, the output from CLK (pin 4) provides the clock signal for cascaded PCF8576s in the system.

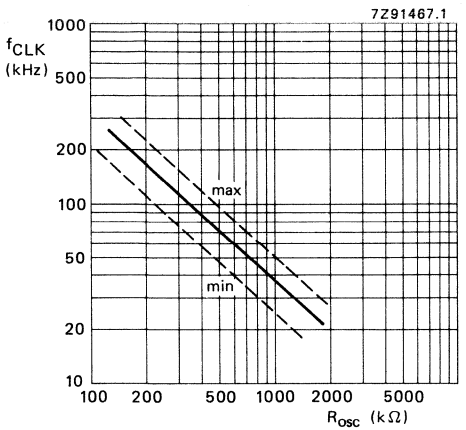


Fig.9 Oscillator frequency as a function of R_{OSC}: $f_{CLK} \approx (3.4 \times 10^7/R_{osc})$ kHz·Ω.

External clock

The condition for external clock is made by tying OSC (pin 6) to V_{DD}; CLK (pin 4) then becomes the external clock input.

The clock frequency (f_{CLK}) determines the LCD frame frequency and the maximum rate for data reception from the I²C-bus. To allow I²C-bus transmissions at their maximum data rate of 100 kHz, f_{CLK} should be chosen to be above 125 kHz.

A clock signal must always be supplied to the device; removing the clock may freeze the LCD in a DC state.

Timing

The timing of the PCF8576 organizes the internal data flow of the device. This includes the transfer of display data from the display RAM to the display segment outputs. In cascaded applications, the synchronization signal $\overline{SYNC}$ maintains the correct timing relationship between the PCF8576s in the system. The timing also generates the LCD frame frequency which it derives as an integer multiple of the clock frequency (Table 3). The frame frequency is set by the choice of value for R_{osc} when internal clock is used, or by the frequency applied to pin 4 when external clock is used.

Table 3 LCD frame frequencies

PCF8576 mode	recommended R_{osc} (kΩ)	f_{frame}	nominal f_{frame} (Hz)
normal mode	180	$f_{CLK}/2880$	64
power-saving mode	1200	$f_{CLK}/480$	64

Timing (continued)

The ratio between the clock frequency and the LCD frame frequency depends on the mode in which the device is operating. In the normal mode, R_{OSC} = 180 kΩ will result in the nominal frame frequency. In the power-saving mode the reduction ratio is six times smaller; this allows the clock frequency to be reduced by a factor of six and for the same frame frequency R_{OSC} will be 1.2 MΩ. The reduced clock frequency and the increased value of R_{OSC} together contribute to a significant reduction in power dissipation. The lower clock frequency has the disadvantage of increasing the response time when large amounts of display data are transmitted on the I²C-bus. When a device is unable to 'digest' a display data byte before the next one arrives, it holds the SCL line LOW until the first display data byte is stored. This slows down the transmission rate of the I²C-bus but no data loss occurs.

Display latch

The display latch holds the display data while the corresponding multiplex signals are generated. There is a one-to-one relationship between the data in the display latch, the LCD segment outputs and one column of the display RAM.

Shift register

The shift register serves to transfer display information from the display RAM to the display latch while previous data is displayed.

Segment outputs

The LCD drive section includes 40 segment outputs S0 to S39 (pins 17 to 56) which should be connected directly to the LCD. The segment output signals are generated in accordance with the multiplexed backplane signals and with the data resident in the display latch. When less than 40 segment outputs are required the unused segment outputs should be left open.

Backplane outputs

The LCD drive section includes four backplane outputs BP0 to BP3 which should be connected directly to the LCD. The backplane output signals are generated in accordance with the selected LCD drive mode. If less than four backplane outputs are required the unused outputs can be left open. In the 1 : 3 multiplex drive mode BP3 carries the same signal as BP1, therefore these two adjacent outputs can be tied together to give enhanced drive capabilities. In the 1 : 2 multiplex drive mode BP0 and BP2, BP1 and BP3 respectively carry the same signals and may also be paired to increase the drive capabilities. In the static drive mode the same signal is carried by all four backplane outputs and they can be connected in parallel for very high drive requirements.

Display RAM

The display RAM is a static 40 x 4-bit RAM which stores LCD data. A logic 1 in the RAM bit-map indicates the 'on' state of the corresponding LCD segment; similarly, a logic 0 indicates the 'off' state. There is a one-to-one correspondence between the RAM addresses and the segment outputs, and between the individual bits of a RAM word and the backplane outputs. The first RAM column corresponds to the 40 segments operated with respect to backplane BP0 (Fig.10). In multiplexed LCD applications the segment data of the second, third and fourth column of the display RAM are time-multiplexed with BP1, BP2 and BP3 respectively.

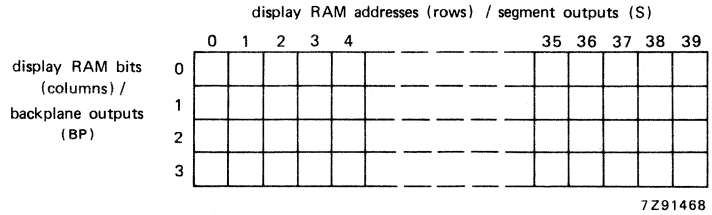


Fig.10 Display RAM bit-map showing direct relationship between display RAM addresses and segment outputs, and between bits in a RAM word and backplane outputs.

When display data are transmitted to the PCF8576 the display bytes received are stored in the display RAM according to the selected LCD drive mode. To illustrate the filling order, an example of a 7-segment numeric display showing all drive modes is given in Fig.11; the RAM filling organization depicted applies equally to other LCD types.

With reference to Fig.11, in the static drive mode the eight transmitted data bits are placed in bit 0 of eight successive display RAM addresses. In the 1 : 2 multiplex drive mode the eight transmitted data bits are placed in bits 0 and 1 of four successive display RAM addresses. In the 1 : 3 multiplex drive mode these bits are placed in bits 0, 1 and 2 of three successive addresses, with bit 2 of the third address left unchanged. This last bit may, if necessary, be controlled by an additional transfer to this address but care should be taken to avoid overriding adjacent data because full bytes are always transmitted. In the 1 : 4 multiplex drive mode the eight transmitted data bits are placed in bits 0, 1, 2 and 3 of two successive display RAM addresses.

Data pointer

The addressing mechanism for the display RAM is realized using the data pointer. This allows the loading of an individual display data byte, or a series of display data bytes, into any location of the display RAM. The sequence commences with the initialization of the data pointer by the LOAD DATA POINTER command. Following this, an arriving data byte is stored starting at the display RAM address indicated by the data pointer thereby observing the filling order shown in Fig.11. The data pointer is automatically incremented according to the LCD configuration chosen. That is, after each byte is stored, the contents of the data pointer are incremented by eight (static drive mode), by four (1 : 2 multiplex drive mode), by three (1 : 3 multiplex drive mode) or by two (1 : 4 multiplex drive mode).

Subaddress counter

The storage of display data is conditioned by the contents of the subaddress counter. Storage is allowed to take place only when the contents of the subaddress counter agree with the hardware subaddress applied to A0, A1 and A2 (pins 7, 8, and 9). The subaddress counter value is defined by the DEVICE SELECT command. If the contents of the subaddress counter and the hardware subaddress do not agree then data storage is inhibited but the data pointer is incremented as if data storage had taken place. The subaddress counter is also incremented when the data pointer overflows.

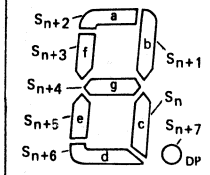
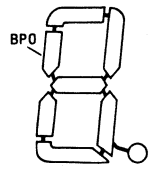
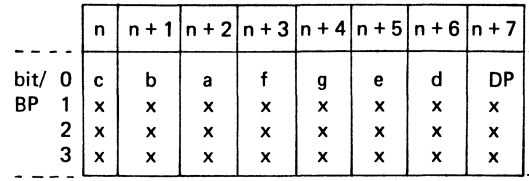
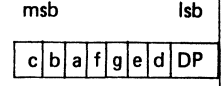
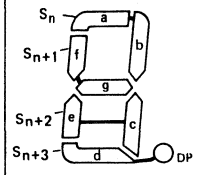
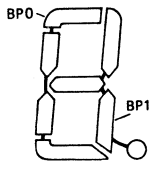
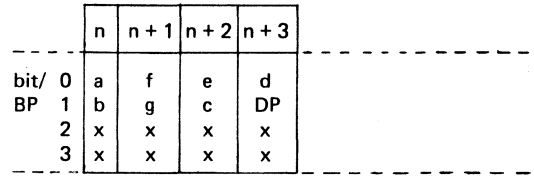
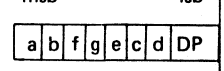
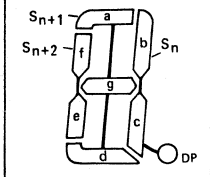
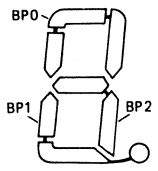
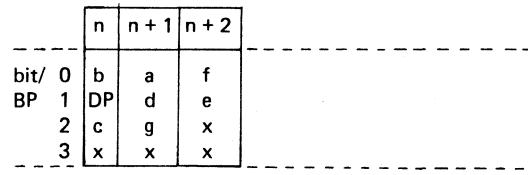
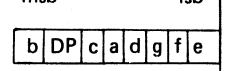
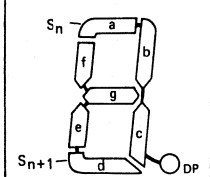
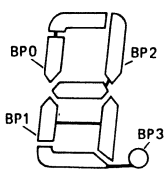
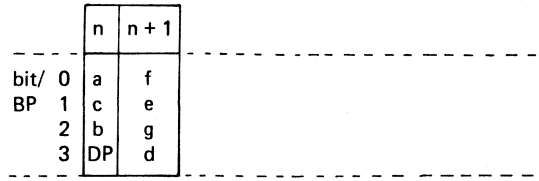
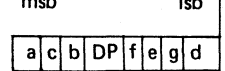
drive mode	LCD segments	LCD backplanes	display RAM filling order	transmitted display byte
static				
1 : 2 multiplex				
1 : 3 multiplex				
1 : 4 multiplex				

Fig. 11 Relationships between LCD layout, drive mode, display RAM filling order and display data transmitted over the I²C bus (x = data bit unchanged).

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Subaddress counter (continued)

The storage arrangements described lead to extremely efficient data loading in cascaded applications. When a series of display bytes are being sent to the display RAM, automatic wrap-over to the next PCF8576 occurs when the last RAM address is exceeded. Subaddressing across device boundaries is successful even if the change to the next device in the cascade occurs within a transmitted character (such as during the 14th display data byte transmitted in 1 : 3 multiplex mode).

Output bank selector

This selects one of the four bits per display RAM address for transfer to the display latch. The actual bit chosen depends on the particular LCD drive mode in operation and on the instant in the multiplex sequence. In 1 : 4 multiplex, all RAM addresses of bit 0 are the first to be selected, these are followed by the contents of bit 1, bit 2 and then bit 3. Similarly in 1 : 3 multiplex, bits 0, 1 and 2 are selected sequentially. In 1 : 2 multiplex, bits 0 then 1 are selected and, in the static mode, bit 0 is selected.

The PCF8576 includes a RAM bank switching feature in the static and 1 : 2 multiplex drive modes. In the static drive mode, the BANK SELECT command may request the contents of bit 2 to be selected for display instead of bit 0 contents. In the 1 : 2 drive mode, the contents of bits 2 and 3 may be selected instead of bits 0 and 1. This gives the provision for preparing display information in an alternative bank and to be able to switch to it once it is assembled.

Input bank selector

The input bank selector loads display data into the display RAM according to the selected LCD drive configuration. Display data can be loaded in bit 2 in static drive mode or in bits 2 and 3 in 1 : 2 drive mode by using the BANK SELECT command. The input bank selector functions independently of the output bank selector.

Blinker

The display blinking capabilities of the PCF8576 are very versatile. The whole display can be blinked at frequencies selected by the BLINK command. The blinking frequencies are integer multiples of the clock frequency; the ratios between the clock and blinking frequencies depend on the mode in which the device is operating, as shown in Table 4.

An additional feature is for an arbitrary selection of LCD segments to be blinked. This applies to the static and 1 : 2 LCD drive modes and can be implemented without any communication overheads. By means of the output bank selector, the displayed RAM banks are exchanged with alternate RAM banks at the blinking frequency. This mode can also be specified by the BLINK command.

In the 1 : 3 and 1 : 4 multiplex modes, where no alternate RAM bank is available, groups of LCD segments can be blinked by selectively changing the display RAM data at fixed time intervals.

If the entire display is to be blinked at a frequency other than the nominal blinking frequency, this can be effectively performed by resetting and setting the display enable bit E at the required rate using the MODE SET command.

Blinker (continued)

Table 4 Blinking frequencies

blinking mode	normal operating mode ratio	power-saving mode ratio	nominal blinking frequency f_{blink} (Hz)
off	–	–	blinking off
2 Hz	$f_{CLK}/92160$	$f_{CLK}/15360$	2
1 Hz	$f_{CLK}/184320$	$f_{CLK}/30720$	1
0.5 Hz	$f_{CLK}/368640$	$f_{CLK}/61440$	0.5

CHARACTERISTICS OF THE I²C-BUS

The I²C-bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

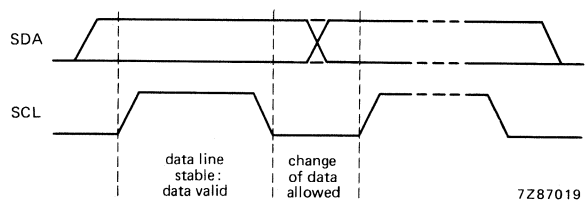


Fig.12 Bit transfer.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

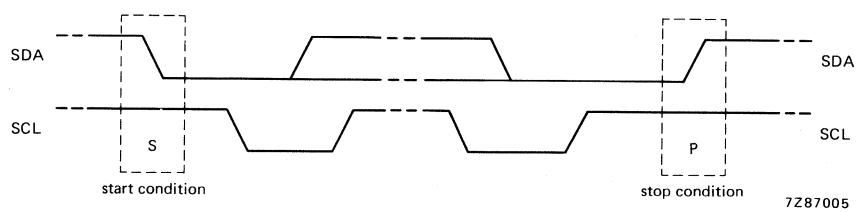


Fig.13 Definition of start and stop conditions.

System configuration

A device generating a message is a "transmitter", a device receiving a message is a "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

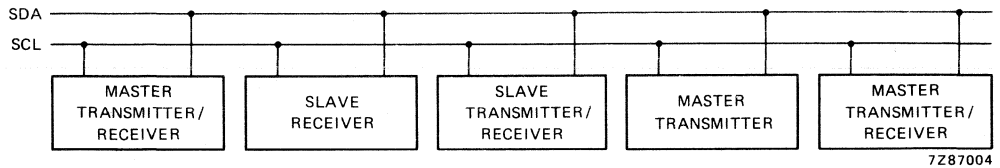


Fig.14 System configuration.

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set up and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

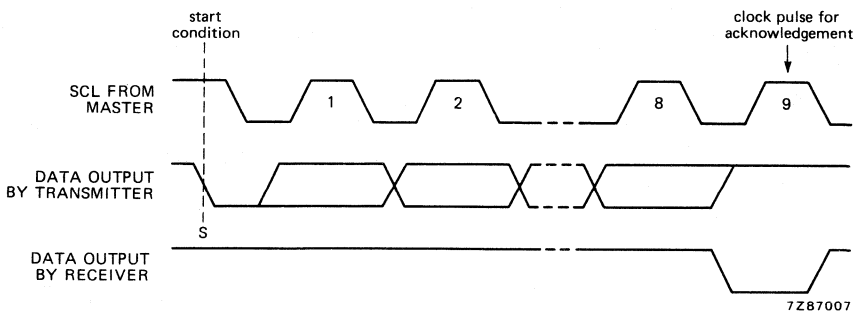


Fig.15 Acknowledgement on the I²C-bus.

Note

The general characteristics and detailed specification of the I²C-bus are described in Handbook IC12: I²C-bus compatible ICs.

PCF8576 I²C-bus controller

The PCF8576 acts as an I²C slave receiver. It does not initiate I²C-bus transfers or transmit data to an I²C master receiver. The only data output from the PCF8576 are the acknowledge signals of the selected devices. Device selection depends on the I²C-bus slave address, on the transferred command data and on the hardware subaddress.

In single device applications, the hardware subaddress inputs A0, A1 and A2 are normally tied to V_{SS} which defines the hardware subaddress 0. In multiple device applications A0, A1 and A2 are tied to V_{SS} or V_{DD} according to a binary coding scheme such that no two devices with a common I²C slave address have the same hardware subaddress.

In the power-saving mode it is possible that the PCF8576 is not able to keep up with the highest transmission rates when large amounts of display data are transmitted. If this situation occurs, the PCF8576 forces the SCL line LOW until its internal operations are completed. This is known as the 'clock synchronization feature' of the I²C-bus and serves to slow down fast transmitters. Data loss does not occur.

Input filters

To enhance noise immunity in electrically adverse environments, RC low-pass filters are provided on the SDA and SCL lines.

I²C-bus protocol

Two I²C-bus slave addresses (0111000 and 0111001) are reserved for PCF8576. The least-significant bit of the slave address that a PCF8576 will respond to is defined by the level tied at its input SA0 (pin 10). Therefore, two types of PCF8576 can be distinguished on the same I²C-bus which allows:

(a) up to 16 PCF8576s on the same I²C-bus for very large LCD applications;

(b) the use of two types of LCD multiplex on the same I²C-bus.

The I²C-bus protocol is shown in Fig.16. The sequence is initiated with a start condition (S) from the I²C-bus master which is followed by one of the two PCF8576 slave addresses available. All PCF8576s with the corresponding SA0 level acknowledge in parallel the slave address but all PCF8576s with the alternative SA0 level ignore the whole I²C-bus transfer. After acknowledgement, one or more command bytes (m) follow which define the status of the addressed PCF8576s. The last command byte is tagged with a cleared mist significant bit, the continuation bit C. The command bytes are also acknowledged by all addressed PCF8576s on the bus.

After the last command byte, a series of display data bytes (n) may follow. These display data bytes are stored in the display RAM at the address specified by the data pointer and the subaddress counter. Both data pointer and subaddress counter are automatically updated and the data are directed to the intended PCF8576 device. The acknowledgement after each byte is made only by the (A0, A1, A2) addressed PCF8576. After the last display byte, the I²C-bus master issues a stop condition (P).

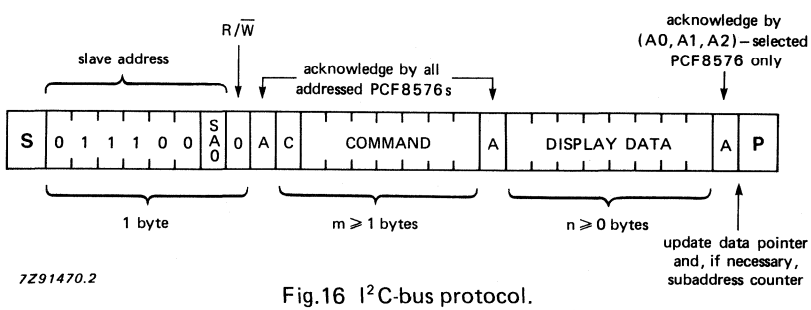


Fig.16 I²C-bus protocol.

Command decoder

The command decoder identifies command bytes that arrive on the I²C-bus. All available commands carry a continuation bit C in their most-significant bit position (Fig.17). When this bit is set, it indicates that the next byte of the transfer to arrive will also represent a command. If the bit is reset, it indicates the last command byte of the transfer. Further bytes will be regarded as display data.

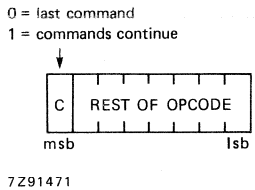


Fig.17 General format of command byte.

The five commands available to the PCF8576 are defined in Table 5.

Command decoder (continued)

Table 5 Definition of PCF8576 commands

command/opcode	options	description
MODE SET C 1 0 LP E B M1 M0	LCD drive mode: bits M1 M0 static (1 BP): 0 1 1 : 2 MUX (2 BP): 1 0 1 : 3 MUX (3 BP): 1 1 1 : 4 MUX (4 BP): 0 0 LCD bias: bit B 1/3 bias: 0 1/2 bias: 1 display status: bit E disabled (blank): 0 enabled: 1 mode: bit LP normal mode: 0 power-saving mode: 1	Defines LCD drive mode Defines LCD bias configuration Defines display status The possibility to disable the display allows implementation of blinking under external control Defines power dissipation mode
LOAD DATA POINTER C 0 P5 P4 P3 P2 P1 P0	bits P5 P4 P3 P2 P1 P0 6-bit binary value of 0 to 39	Six bits of immediate data, bits P5 to P0, are transferred to the data pointer to define one of forty display RAM addresses
DEVICE SELECT C 1 1 0 0 A2 A1 A0	bits A0 A1 A2 3-bit binary value of 0 to 7	Three bits of immediate data, bits A0 to A2, are transferred to the subaddress counter to define one of eight hardware subaddresses

<table>
<tr><th>command/opcode</th><th>options</th><th>description</th></tr>
<tr><td>BANK SELECT

C | 1 1 1 1 0 | I | O</td><td>
<table>
<tr><td>static</td><td>1 : 2 MUX</td><td>bit I</td></tr>
<tr><td>RAM bit 0
RAM bit 2</td><td>RAM bits 0, 1
RAM bits 2, 3</td><td>0
1</td></tr>
</table>
<table>
<tr><td>static</td><td>1 : 2 MUX</td><td>bit O</td></tr>
<tr><td>RAM bit 0
RAM bit 2</td><td>RAM bits 0, 1
RAM bits 2, 3</td><td>0
1</td></tr>
</table>
</td><td>Defines input bank selection (storage of arriving display data)

Defines output bank selection (retrieval of LCD display data)

The BANK SELECT command has no effect in 1 : 3 and 1 : 4 multiplex drive modes</td></tr>
<tr><td>BLINK

C | 1 1 1 0 | A | BF1 BF0</td><td>
<table>
<tr><td>blink frequency</td><td>bits BF1</td><td>BF0</td></tr>
<tr><td>off</td><td>0</td><td>0</td></tr>
<tr><td>2 Hz</td><td>0</td><td>1</td></tr>
<tr><td>1 Hz</td><td>1</td><td>0</td></tr>
<tr><td>0.5 Hz</td><td>1</td><td>1</td></tr>
</table>
<table>
<tr><td>blink mode</td><td>bit A</td></tr>
<tr><td>normal blinking
alternation blinking</td><td>0
1</td></tr>
</table>
</td><td>Defines the blinking frequency

Selects the blinking mode; normal operation with frequency set by bits BF1, BF0, or blinking by alternation of display RAM banks. Alternation blinking does not apply in 1 : 3 and 1 : 4 multiplex drive modes</td></tr>
</table>

Display controller

The display controller executes the commands identified by the command decoder. It contains the status registers of the PCF8576 and coordinates their effects. The controller is also responsible for loading display data into the display RAM as required by the filling order.

Cascaded operation

In large display configurations, up to 16 PCF8576s can be distinguished on the same I²C-bus by using the 3-bit hardware subaddress (A0, A1, A2) and the programmable I²C slave address (SA0). It is also possible to cascade up to 16 PCF8576s. When cascaded, several PCF8576s are synchronized so that they can share the backplane signals from one of the devices in the cascade. Such an arrangement is cost-effective in large LCD applications since the backplane outputs of only one device need to be through-plated to the backplane electrodes of the display. The other PCF8576s of the cascade contribute additional segment outputs but their backplane outputs are left open (Fig.18).

The $\overline{SYNC}$ line is provided to maintain the correct synchronization between all cascaded PCF8576s. This synchronization is guaranteed after the power-on reset. The only time that $\overline{SYNC}$ is likely to be needed is if synchronization is accidently lost (e.g. by noise in adverse electrical environments; or by the definition of a multiplex mode when PCF8576s with differing SA0 levels are cascaded). $\overline{SYNC}$ is organized as an input/output pin; the output section being realized as an open-drain driver with an internal pull-up resistor. A PCF8576 asserts the $\overline{SYNC}$ line at the onset of its last active backplane signal and monitors the $\overline{SYNC}$ line at all other times. Should synchronization in the cascade be lost, it will be restored by the first PCF8576 to assert $\overline{SYNC}$. The timing relationships between the backplane waveforms and the $\overline{SYNC}$ signal for the various drive modes of the PCF8576 are shown in Fig.19.

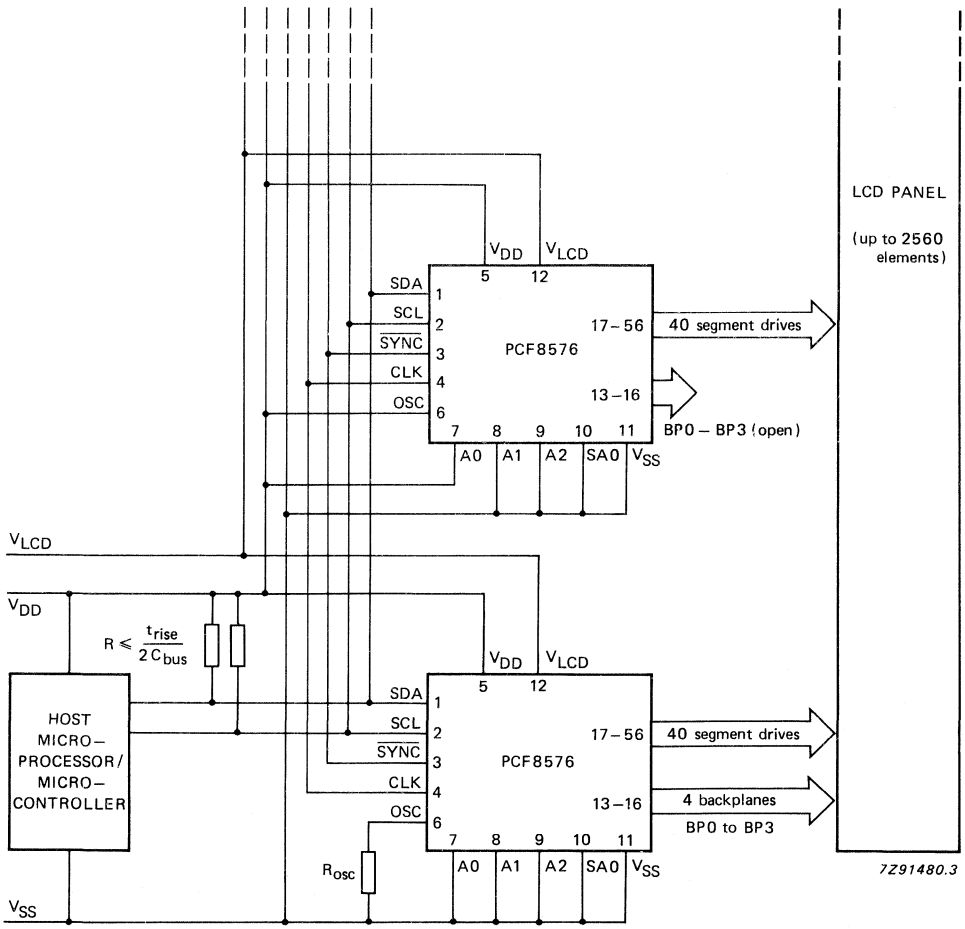
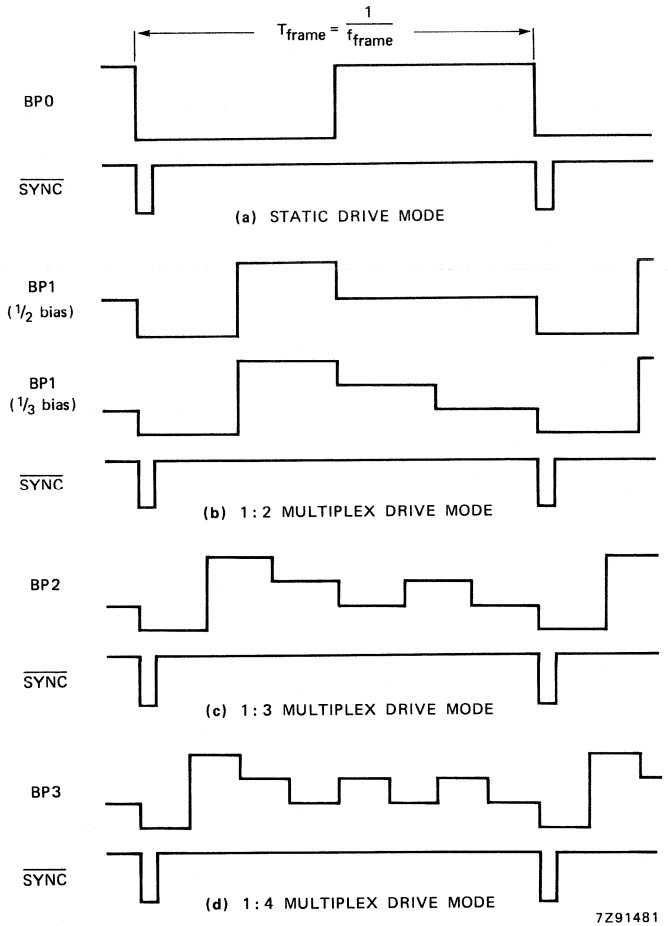


Fig.18 Cascaded PCF8576 configuration.



Note

Excessive capacitive coupling between SCL or CLK and SYNC may cause erroneous synchronization. If this proves to be a problem, the capacitance of the $\overline{SYNC}$ line should be increased (e.g. by an external capacitor between $\overline{SYNC}$ and V_{DD}). Degradation of the positive edge of the $\overline{SYNC}$ pulse may be countered by an external pull-up resistor.

Fig.19 Synchronization of the cascade for the various PCF8576 drive modes.

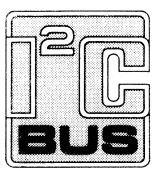
RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage range	V_{DD}	−0.5	+ 11.0	V
LCD supply voltage range	V_{LCD}	V_{DD}−11	V_{DD}	V
Input voltage range SDA; SCL; CLK; $\overline{SYNC}$; SA0; OSC; A0 to A2	V_I	V_{SS}−0.5	V_{DD} + 0.5	V
Output voltage range S0 to S39; BP0 to BP3	V_O	V_{LCD}−0.5	V_{DD} + 0.5	V
DC input current	$\pm I_I$	–	20	mA
DC output current	$\pm I_O$	–	25	mA
V_{DD}, V_{SS} or V_{LCD} current	$\pm I_{DD}$, $\pm I_{SS}$, $\pm I_{LCD}$	–	50	mA
Power dissipation per package	P_{tot}	–	400	mW
Power dissipation per output	P_O	–	100	mW
Storage temperature range	T_{stg}	−65	+ 150	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').



DC CHARACTERISTICS

V_{DD} = 2 V to 9 V; V_{SS} = 0 V; V_{LCD} = V_{DD}−2 V to V_{DD}−9 V; T_{amb} = −40 °C to + 85 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage		V_{DD}	2	–	9	V
LCD supply voltage	note 1	V_{LCD}	V_{DD}−9	–	V_{DD}−2	V
Supply current	note 2;					
normal mode	f_{CLK} = 200 kHz	I_{DD}	–	–	180	μA
power-saving mode	V_{DD} = 3.5 V; V_{LCD} = 0 V; f_{CLK} = 35 kHz	I_{LP}	–	–	60	μA
Logic						
Input voltage LOW		V_{IL}	V_{SS}	–	0.3 V_{DD}	V
Input voltage HIGH		V_{IH}	0.7 V_{DD}	–	V_{DD}	V
Output voltage LOW	I_O = 0 mA	V_{OL}	–	–	0.05	V
Output voltage HIGH	I_O = 0 mA	V_{OH}	V_{DD}−0.05	–	–	V
Output current LOW						
CLK; $\overline{SYNC}$	V_{OL} = 1 V; V_{DD} = 5 V	I_{OL1}	1	–	–	mA
Output current HIGH						
CLK	V_{OH} = 4 V; V_{DD} = 5 V	$-I_{OH}$	1	–	–	mA
Output current LOW						
SDA; SCL	V_{OL} = 0.4 V; V_{DD} = 5 V	I_{OL2}	3	–	–	mA
Leakage current						
SA0; A0 to A2; CLK; SDA; SCL	V_I = V_{SS} or V_{DD}	$\pm I_{L1}$	–	–	1	μA
OSC	V_I = V_{DD}	$\pm I_{L2}$	–	–	1	μA
Pull-up resistor ($\overline{SYNC}$)		R_{SYNC}	20	50	150	kΩ
Power-on reset level	note 3	V_{POR}	–	1.0	1.6	V
Tolerable spike width on bus		t_{SW}	–	–	100	ns
Input capacitance	note 4	C_I	–	–	7	pF
LCD outputs						
DC voltage component						
BP0 to BP3	C_{BP} = 35 nF	$\pm V_{BP}$	–	20	–	mV
S0 to S39	C_S = 5 nF	$\pm V_S$	–	20	–	mV
Output impedance	note 5					
BP0 to BP3	V_{LCD} = V_{DD}−5 V	R_{BP}	–	–	5	kΩ
S0 to S39	V_{LCD} = V_{DD}−5 V	R_S	–	–	7.5	kΩ

AC CHARACTERISTICS (note 6)

V_{DD} = 2 V to 9 V; V_{SS} = 0 V; V_{LCD} = V_{DD}−2 V to V_{DD}−9 V; T_{amb} = −40 to + 85 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Oscillator frequency						
normal mode	V_{DD} = 5 V; note 7 R_{OSC} = 180 kΩ	f_{CLK}	125	185	288	kHz
power-saving mode	V_{DD} = 3.5 V; R_{OSC} = 1.2 MΩ	f_{CLKLP}	21	31	48	kHz
CLK HIGH time		t_{CLKH}	1	–	–	μs
CLK LOW time		t_{CLKL}	1	–	–	μs
$\overline{SYNC}$ propagation delay		t_{PSYNC}	–	–	400	ns
$\overline{SYNC}$ LOW time		t_{SYNCL}	1	–	–	μs
Driver delays						
with test loads	V_{LCD} = V_{DD}−5 V	t_{PLCD}	–	–	30	μs
I²C-bus						
Bus free time		t_{BUF}	4.7	–	–	μs
Start condition hold time		$t_{HD;STA}$	4.0	–	–	μs
SCL LOW time		t_{LOW}	4.7	–	–	μs
SCL HIGH time		t_{HIGH}	4.0	–	–	μs
Start condition set-up time						
(repeated start code only)		$t_{SU;STA}$	4.7	–	–	μs
Data hold time		$t_{HD;DAT}$	0	–	–	μs
Data set-up time		$t_{SU;DAT}$	250	–	–	ns
Rise time		t_r	–	–	1	μs
Fall time		t_f	–	–	300	ns
Stop condition set-up time		$t_{SU;STO}$	4.0	–	–	μs

Notes to the characteristics

1. $V_{LCD} \leqslant V_{DD}$−3 V for 1/3 bias.
2. Outputs open; inputs at V_{SS} or V_{DD}; external clock with 50% duty factor; I²C-bus inactive.
3. Resets all logic when $V_{DD} < V_{POR}$.
4. Periodically sampled, not 100% tested.
5. Outputs measured one at a time.
6. All timing values referred to V_{IH} and V_{IL} levels with an input voltage swing of V_{SS} to V_{DD}.
7. At $f_{CLK} < 125$ kHz, I²C-bus maximum transmission speed is derated.

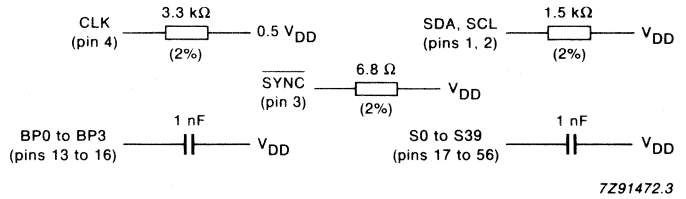


Fig.20 Test loads.

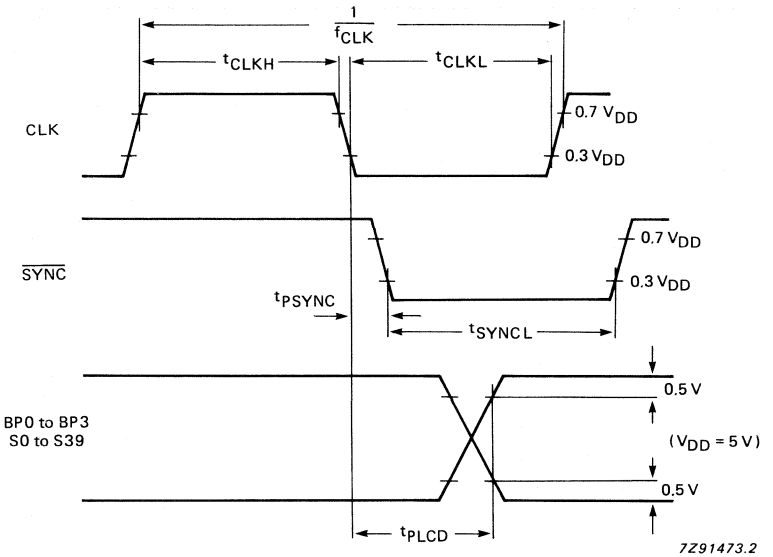


Fig.21 Driver timing waveforms.

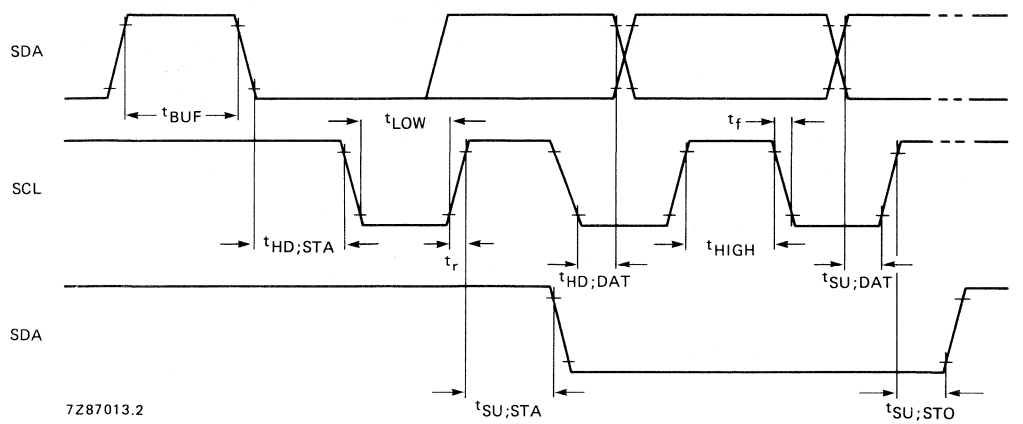
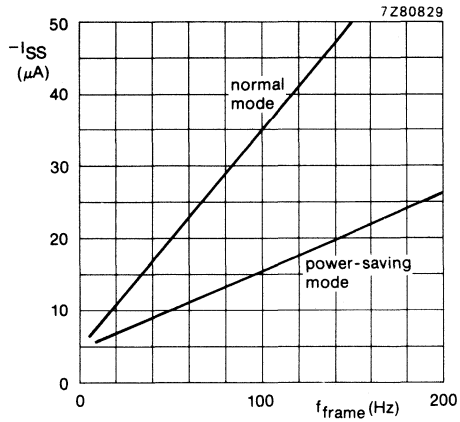
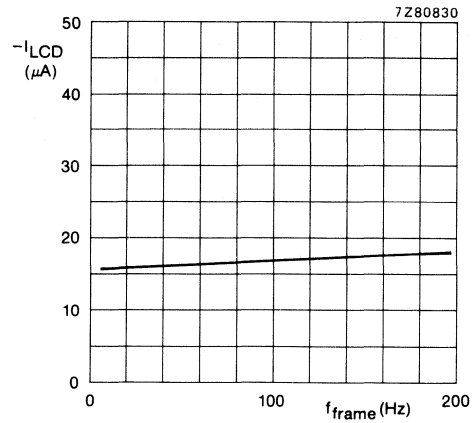


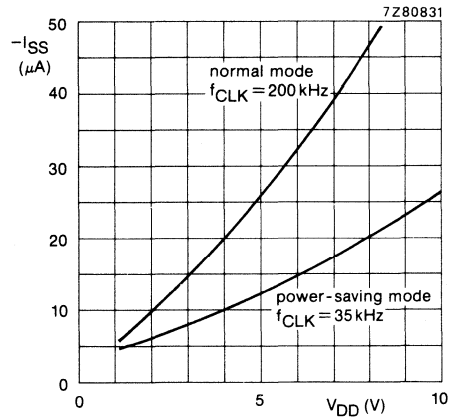
Fig.22 I²C-bus timing waveforms.



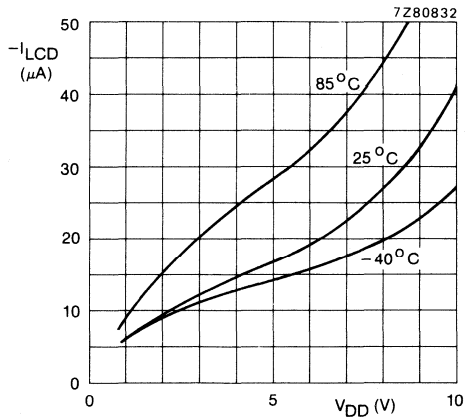
(a) V_{DD} = 5 V; V_{LCD} = 0 V; T_{amb} = 25 °C.



(b) V_{DD} = 5 V; V_{LCD} = 0 V; T_{amb} = 25 °C.

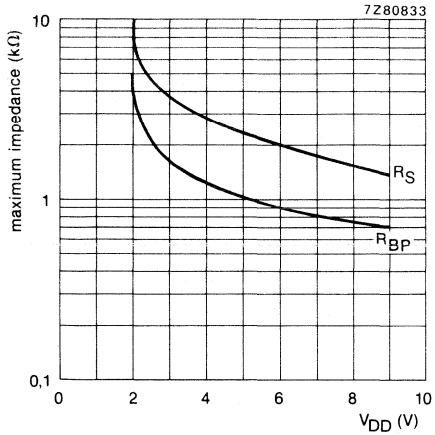


(c) V_{LCD} = 0 V; external clock;
T_{amb} = −40 to 85 °C.

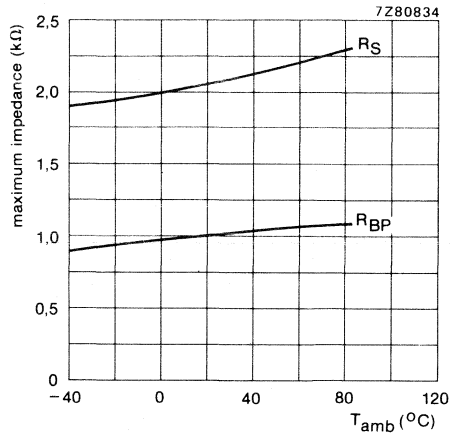


(d) V_{LCD} = 0 V; external clock;
f_{CLK} = nominal frequency.

Fig.23 Typical supply current characteristics.



(a) V_{LCD} = 0 V; T_{amb} = 25 °C.



(b) V_{DD} = 5 V; V_{LCD} = 0 V.

Fig.24 Typical characteristics of LCD outputs.

APPLICATION INFORMATION

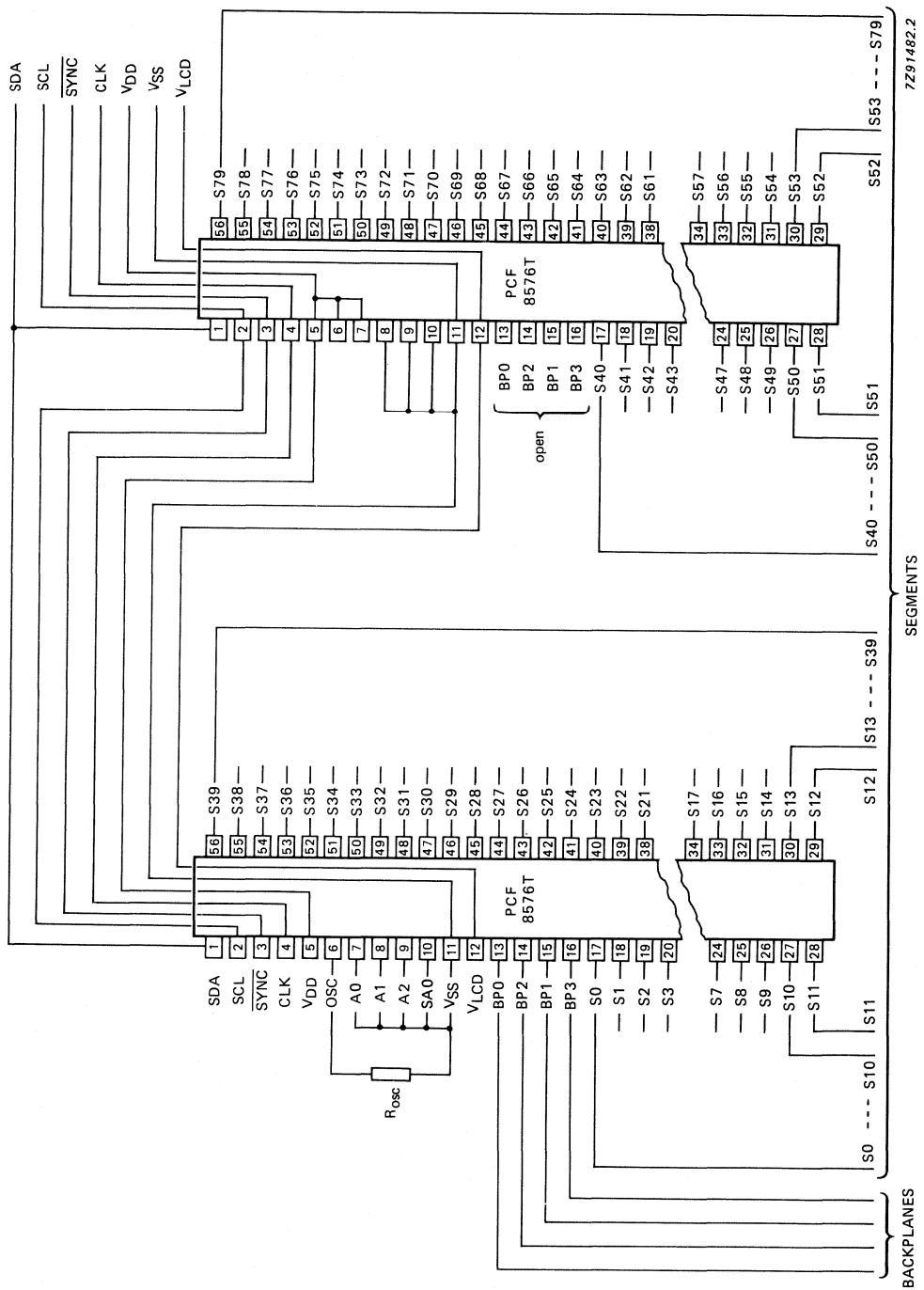


Fig.25 Single plane wiring of packaged PCF8576Ts.

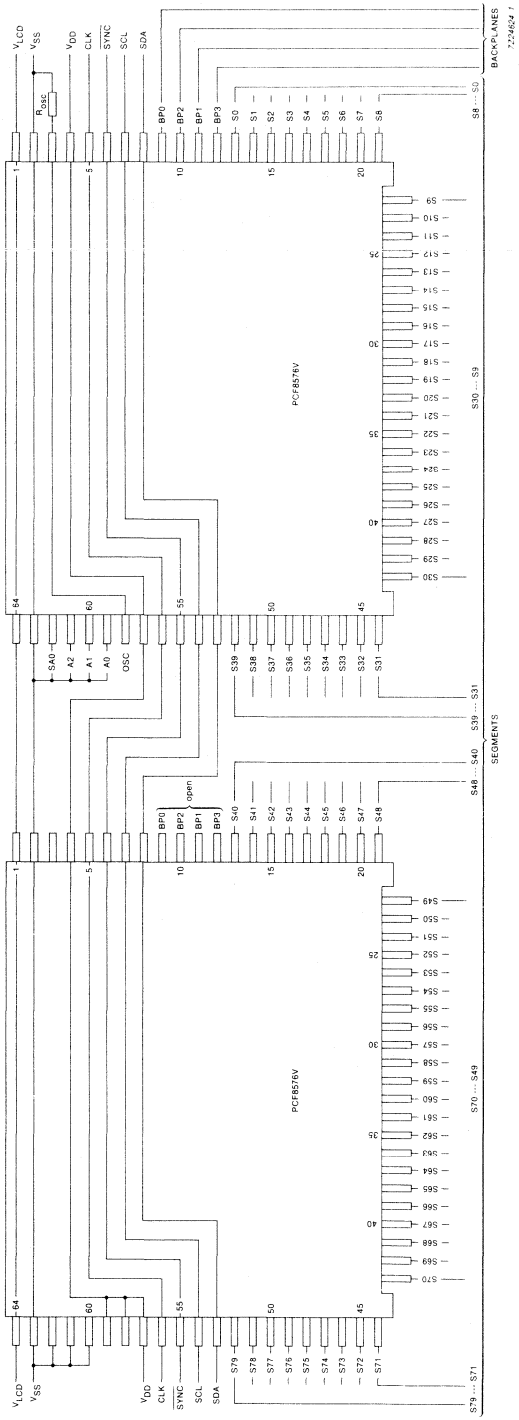


Fig.26 Single plane wiring of packaged PCF8576Vs.

LCD direct /duplex driver with I²C-bus interface

PCF8577/A/C/CA

GENERAL DESCRIPTION

The PCF8577 is a single chip, silicon gate CMOS circuit. It is designed to drive liquid crystal displays with up to 32 segments directly, or 64 segments in a duplex manner.

The two-line I²C-bus interface substantially reduces wiring overheads in remote display applications. Bus traffic is minimized in multiple IC applications by automatic address incrementing, hardware sub-addressing and display memory switching (direct drive mode).
The PCF8577 and PCF8577C differ from the PCF8577A and PCF8577CA only in their slave addresses.
The PCF8577C/77CA is a low-voltage version of the PCF8577/77A.

Features

- Direct/duplex drive modes with up to 32/64 LCD-segment drive capability per device
- Opering supply voltage:
  PCF8577/77A: 2.5 to 9 V
  PCF8577C/77CA: 2.5 to 6 V
- Low power consumption
- I²C-bus interface
- Optimized pinning for single plane wiring
- Single-pin built-in oscillator
- Auto-incremented loading across device subaddress boundaries
- Display memory switching in direct drive mode
- May be used as I²C-bus output expander
- System expansion up to 256 segments (512 segments with PCF8577A/CA)
- Power-on reset blanks display

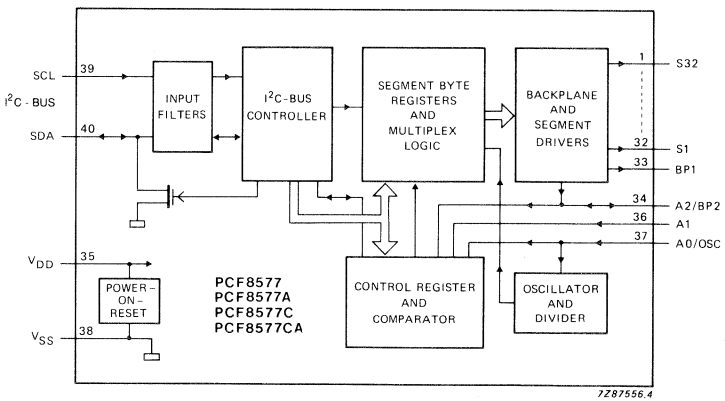


Fig.1 Block diagram.

PAKCAGE OUTLINES

PCF8577P, PCF8577AP	:	40-lead DIL; plastic (SOT129).
PCF8577CP, PCF8577CAP	:	
PCF8577T, PCF8577AT	:	40-lead mini-pack; plastic (VSO40; SOT158A).
PCF8577CT, PCF8577CAT	:	
PCF8577T, PCF8577AT	:	in blister tape.
PCF8577CT, PCF8577CAT	:	
PCF8577U/5	:	wafer unsawn.
PCF8577CU/5	:	
PCF8577U/10	:	chip on film-frame-carrier (FFC).
PCF8577CU/10	:	

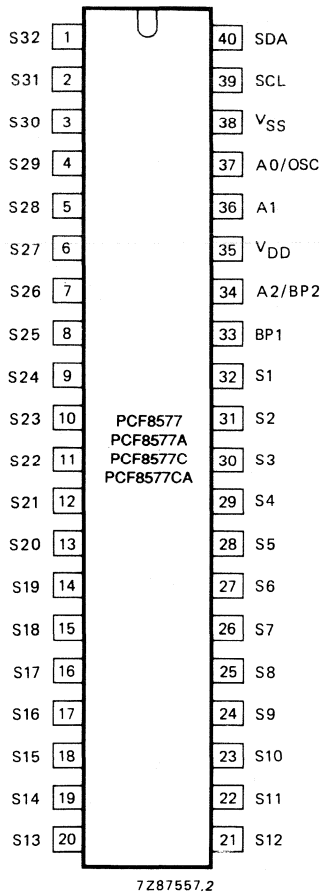


Fig.2 Pinning diagram.

PINNING

Supply

35	V_{DD}	positive supply
38	V_{SS}	negative supply

I²C-bus

40	SDA	I²C-bus data line
39	SCL	I²C-bus clock line

Inputs

36	A1	hardware address line
37	A0/OSC	hardware address line/oscillator pin

Outputs

1 – 32	S32 – S1	segment outputs

Input – Output

34	A2/BP2	harware address line/cascade sync input/backplane output
33	BP1	cascade sync input/backplane output

FUNCTIONAL DESCRIPTION

Hardware subaddress A0, A1, A2

The hardware subaddress lines A0, A1, A2 are used to program the device subaddress for each PCF8577 on the bus. Lines A0 and A2 are shared with OSC and BP2 respectively to reduce pin-out requirements.

A0/OSC Line A0 is defined as LOW (logic 0) when this pin is used for the local oscillator or when connected to V_{SS}. Line A0 is defined as HIGH (logic 1) when connected to V_{DD}.

A1 Line A1 must be defined as LOW (logic 0) or as HIGH (logic 1) by connection to V_{SS} or V_{DD} respectively.

A2/BP2 In the direct drive mode the second backplane signal BP2 is not used and the A2/BP2 pin is exclusively the A2 input. Line A2 is defined as LOW (logic 0) when connected to V_{SS} or, if this is not possible, by leaving it unconnected (internal pull-down). Line A2 is defined as HIGH (logic 1) when connected to V_{DD}.

In the duplex drive mode the second backplane signal BP2 is required and the A2 signal is undefined. In this mode device selection is made exclusively from lines A0 and A1.

DC CHARACTERISTICS

V_{DD} = 2.5 to 9.0 V (PCF8577/77A) or 2.5 to 6.0 V (PCF8577C/77CA); V_{SS} = 0 V; T_{amb} = −40 to + 85 °C unless otherwise specified

parameter	conditions	symbol	min.	typ.*	max.	unit
Supply						
Supply voltage						
PCF8577/77A		V_{DD}	2.5	–	9.0	V
PCF8577C/77CA		V_{DD}	2.5	–	6.0	V
Supply current	non specified inputs at V_{DD} or V_{SS}					
at f_{SCL} = 100 kHz	no load; R_{OSC} = 1 MΩ; C_{OSC} = 680 pF					
PCF8577/77A		I_{DD1}	–	80	250	μA
PCF8577C/77CA		I_{DD1}	–	50	125	μA
at f_{SCL} = 0	no load; R_{OSC} = 1 MΩ; C_{OSC} = 680 pF					
PCF8577/77A		I_{DD2}	–	25	150	μA
PCF8577C/77CA		I_{DD2}	–	25	75	μA
at f_{SCL} = 0	no load; R_{OSC} = 1 MΩ; C_{OSC} = 680 pF; V_{DD} = 5 V; T_{amb} = 25 °C	I_{DD3}	–	25	40	μA
at f_{SCL} = 0	no load; direct mode; A0/OSC = V_{DD}; V_{DD} = 5 V; T_{amb} = 25 °C	I_{DD4}	–	10	20	μA
Power-on reset level	note 1	V_{POR}	–	1.1	2.0	V
Input A0						
Input voltage LOW		V_{IL1}	0	–	0.05	V
Input voltage HIGH		V_{IH1}	V_{DD}−0.05	–	V_{DD}	V
Input A1						
Input voltage LOW		V_{IL2}	0	–	0.3 V_{DD}	V
Input voltage HIGH		V_{IH2}	0.7 V_{DD}	–	V_{DD}	V
Input A2						
Input voltage LOW		V_{IL3}	0	–	0.10	V
Input voltage HIGH		V_{IH3}	V_{DD}−0.10	–	V_{DD}	V

* Typical conditions: V_{DD} = 5 V; T_{amb} = 25 °C.

DC CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.*	max.	unit
Inputs SCL; SDA						
Input voltage LOW		V_{IL4}	0	–	0.8	V
Input voltage HIGH						
PCF8577/77A		V_{IH4}	2.0	–	9.0	V
PCF8577C/77CA		V_{IH4}	2.0	–	6.0	V
Input capacitance	note 2	C_I	–	–	7	pF
Output SDA						
Output current LOW	V_{OL} = 0.4 V; V_{DD} = 5 V	I_{OL}	3.0	–	–	mA
A1; SCL; SDA						
Leakage current	$V_I = V_{DD}$ or V_{SS}	$\pm I_{L1}$	–	–	1	μA
A2/BP2; BP1						
Leakage current	$V_I = V_{DD}$ or V_{SS}	$\pm I_{L2}$	–	–	5	μA
A2/BP2						
Pull-down current	$V_I = V_{DD}$	$-I_{L2}$	–	1.5	5	μA
A0/OSC						
Leakage current	$V_I = V_{DD}$	$-I_{L3}$	–	–	1	μA
Oscillator						
Start-up current	$V_I = V_{SS}$	I_{OSC}	–	1.2	5	μA
LCD outputs						
DC component of LCD driver		$\pm V_{BP}$	–	20	–	mV
Segment output current	V_{DD} = 5 V; note 6					
PCF8577/77A	V_{OL} = 0.4 V	I_{OL1}	0.3	–	–	mA
PCF8577C/77CA	V_{OL} = 0.8 V	I_{OL1}	0.3	–	–	mA
PCF8577/77A	$V_{OH} = V_{DD}-0.4$ V	$-I_{OH1}$	0.3	–	–	mA
PCF8577C/77CA	$V_{OH} = V_{DD}-0.8$ V	$-I_{OH1}$	0.3	–	–	mA
Backplane output resistance (BP1; BP2)	$V_O = V_{SS}$, V_{DD}, $(V_{SS}+V_{DD})/2$; note 3	R_{BP}	–	0.4	5	kΩ

* Typical conditions: V_{DD} = 5 V; T_{amb} = 25 °C.

AC CHARACTERISTICS (note 4)

V_{DD} = 2.5 to 9.0 V (PCF8577/77A) or 2.5 to 6.0 V (PCF8577C/77CA);
T_{amb} = −40 to + 85 °C unless otherwise specified

parameter	conditions	symbol	min.	typ.*	max.	unit
Display frequency	C_{OSC} = 680 pF; R_{OSC} = 1 MΩ	f_{LCD}	65	90	120	Hz
Driver delays with test loads	V_{DD} = 5 V	t_{BS}	–	20	100	μs
I²C-bus						
SCL clock frequency		f_{SCL}	–	–	100	kHz
Tolerable spike width on bus	note 5	t_{SW}	–	–	100	ns
Bus free time		t_{BUF}	4.7	–	–	μs
Start condition set-up time		$t_{SU;STA}$	4.0	–	–	μs
Start condition hold time		$t_{HD;STA}$	4.0	–	–	μs
SCL LOW time		t_{LOW}	4.7	–	–	μs
SCL HIGH time		t_{HIGH}	4.0	–	–	μs
SCL and SDA rise time		t_r	–	–	1.0	μs
SCL and SDA fall time		t_f	–	–	0.3	μs
Data set-up time		$t_{SU;DAT}$	250	–	–	ns
Data hold time		$t_{HD;DAT}$	0	–	–	ns
Stop condition set-up time		$t_{SU;STO}$	4.0	–	–	μs

Notes to the characteristics

1. Resets all logic when $V_{DD} < V_{POR}$.
2. Periodically sampled, not 100% tested.
3. Outputs measured one at a time; V_{DD} = 5 V; I_{load} = 100 μA.
4. All the timing values are valid within the operating supply voltage and ambient temperature range and refer to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.
5. PCF8577C/CA 25 °C only.
6. Outputs measured one at a time.

* Typical conditions: V_{DD} = 5 V; T_{amb} = 25 °C.

LCD row/column driver for dot matrix graphic displays

PCF8578

GENERAL DESCRIPTION

The PCF8578 is a low power CMOS LCD row/column driver, designed to drive dot matrix graphic displays at multiplex rates of 1:8, 1:16, 1:24 or 1:32. The device has 40 outputs, of which 24 are programmable, configurable as 32/8, 24/16, 16/24 or 8/32 rows/columns. The PCF8578 can function as a stand-alone LCD controller/driver for use in small systems, or for larger systems can be used in conjunction with up to 32 PCF8579s for which it has been optimized. Together these two devices form a general purpose LCD dot matrix driver chip set, capable of driving displays of up to 40,960 dots. The PCF8578 is compatible with most microcontrollers and communicates via a two-line bidirectional bus (I²C-bus). Communication overheads are minimized by a display RAM with auto-incremented addressing and display bank switching.

Features

- Single chip LCD controller/driver
- Stand-alone or may be used with up to 32 PCF8579s (40,960 dots possible)
- 40 driver outputs, configurable as 32/8, 24/16, 16/24 or 8/32 rows/columns
- Selectable multiplex rates; 1:8, 1:16, 1:24 or 1:32
- Externally selectable bias configuration, 5 or 6 levels
- 1280-bit RAM for display data storage and scratch pad
- Display memory bank switching
- Auto-incremented data loading across hardware subaddress boundaries (with PCF8579)
- Provides display synchronization for PCF8579
- On-chip oscillator, requires only 1 external resistor
- Power-on reset blanks display
- Logic voltage supply range 2.5 V to 6.0 V
- Maximum LCD supply voltage 9 V
- Low power consumption
- I²C-bus interface
- TTL/CMOS compatible
- Compatible with most microcontrollers
- Optimized pinning for single plane wiring in multiple device applications (with PCF8579)
- Space saving 56-lead plastic mini-pack
- Compatible with chip-on-glass technology

APPLICATIONS

- Automotive information systems
- Telecommunication systems
- Point-of-sale terminals
- Computer terminals
- Instrumentation

PACKAGE OUTLINES

PCF8578T: 56-lead mini-pack; plastic (VSO56; SOT190).
PCF8578V: 64-lead tape-automated-bonding module (SOT267A).
PCF8578U: chip with bumps on-tape.

LCD row/column driver for dot matrix graphic displays

PCF8578

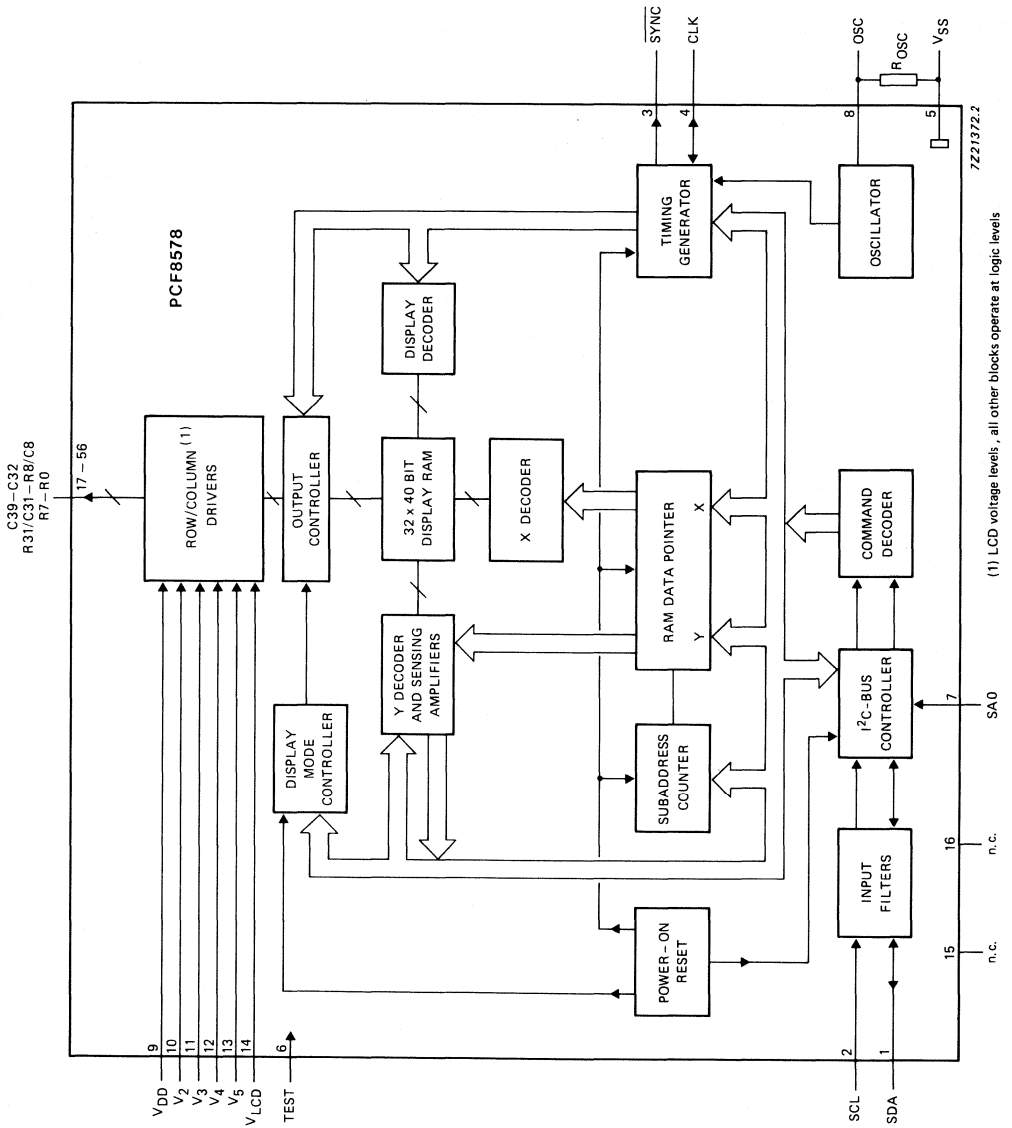


Fig.1 Block diagram.

PINNING

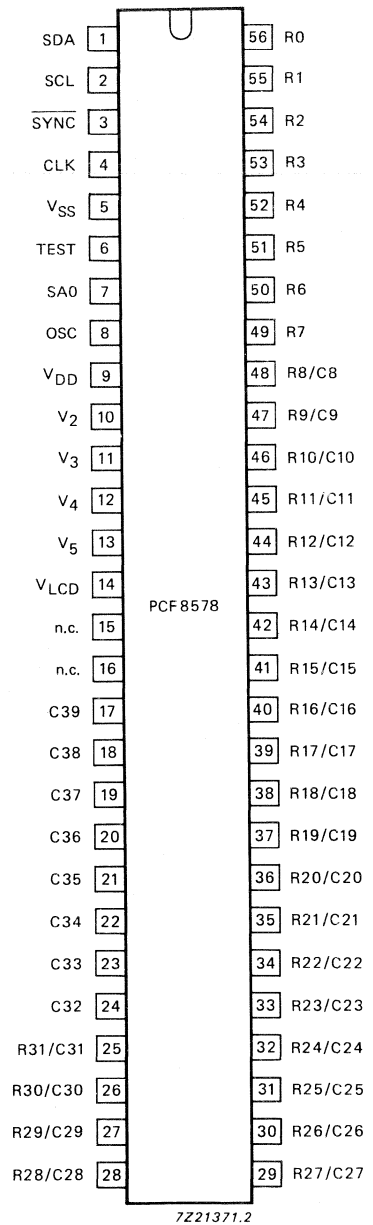
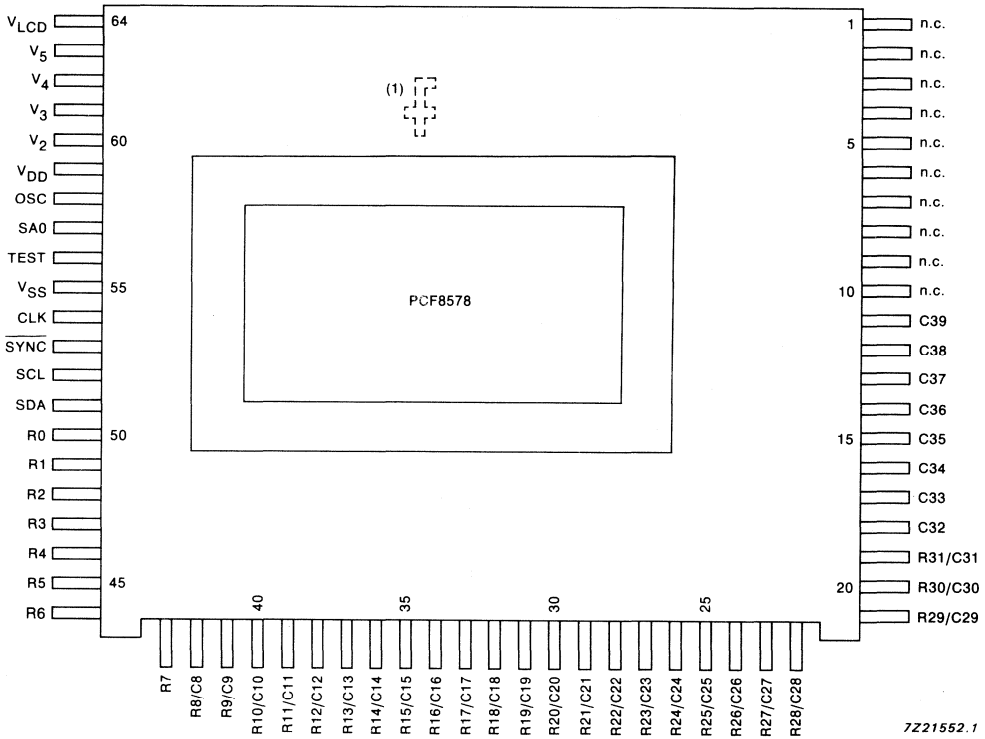


Fig.2 (a) Pinning diagram: VSO56; SOT190.

PINNING (continued)



(1) Orientation mark.

Fig.2 (b) Pinning diagram; SO121.

mnemonic	pin no.		description
	SOT190	SO121	
SDA	1	51	I²C-bus serial data line
SCL	2	52	I²C-bus serial clock line
$\overline{SYNC}$	3	53	cascade synchronization output
CLK	4	54	external clock input/output
V_{SS}	5	55	ground (logic)
TEST	6	56	test pin (connect to V_{SS})
SA0	7	57	I²C-bus slave address input (bit 0)
OSC	8	58	oscillator input
V_{DD}	9	59	positive supply voltage
V_2 to V_5	10 - 13	60 - 63	LCD bias voltage inputs
V_{LCD}	14	64	LCD supply voltage
n.c.	15 - 16	1 - 10	not connected
C39 to C32	17 - 24	11 - 18	LCD column driver outputs
R31/C31 to R8/C8	25 - 48	19 - 42	LCD row/column driver outputs
R7 to R0	49 - 56	43 - 50	LCD row driver outputs

FUNCTIONAL DESCRIPTION

The PCF8578 row/column driver is designed for use in one of three ways:

- Stand-alone row/column driver for small displays (mixed mode)
- Row/column driver with cascaded PCF8579s (mixed mode)
- Row driver with cascaded PCF8579s (row mode)

Mixed mode

In mixed mode, the device functions as both a row and column driver. It can be used in small stand-alone applications, or for larger displays with up to 15 PCF8579s (31 PCF8579s when two slave addresses are used). See table 1 for common display configurations.

Row mode

In row mode, the device functions as a row driver with up to 32 row outputs and provides the clock and synchronization signals for the PCF8579. Up to 16 PCF8579s can normally be cascaded (32 when two slave addresses are used).

Table 1 Possible display configurations

application	multiplex rate	mixed mode		row mode		typical applications
		rows	columns	rows	columns	
stand-alone	1:8	8	32	–	–	small digital or alphanumeric displays
	1:16	16	24	–	–	
	1:24	24	16	–	–	
	1:32	32	8	–	–	
with PCF8579	1:8	8	632	8 x 4	640	alphanumeric displays and dot matrix graphic displays
	1:16	16	624	16 x 2	640	
	1:24	24	616	24	640	
	1:32	32	608	32	640	
		using 15 PCF8579s		using 16 PCF8579s		

Timing signals are derived from the on-chip oscillator, whose frequency is determined by the value of the resistor connected between OSC and V_{SS}.

Commands sent on the I²C-bus from the host microprocessor set the mode (row or mixed), configuration (multiplex rate and number of rows and columns) and control the operation of the device. The device may have one of two slave addresses. The only difference between these slave addresses is the least significant bit, which is set by the logic level applied to SA0. The PCF8578 and PCF8579 also have subaddresses. The subaddress of the PCF8578 is only defined in mixed mode and is fixed at 0. The RAM may only be accessed in mixed mode and data is loaded as described for the PCF8579.

Bias levels may be generated by an external potential divider with appropriate decoupling capacitors. For large displays, bias sources with high drive capability should be used. A typical mixed mode system operating with up to 15 PCF8579s is shown in Fig.3 (a stand-alone system would be identical but without the PCF8579s).

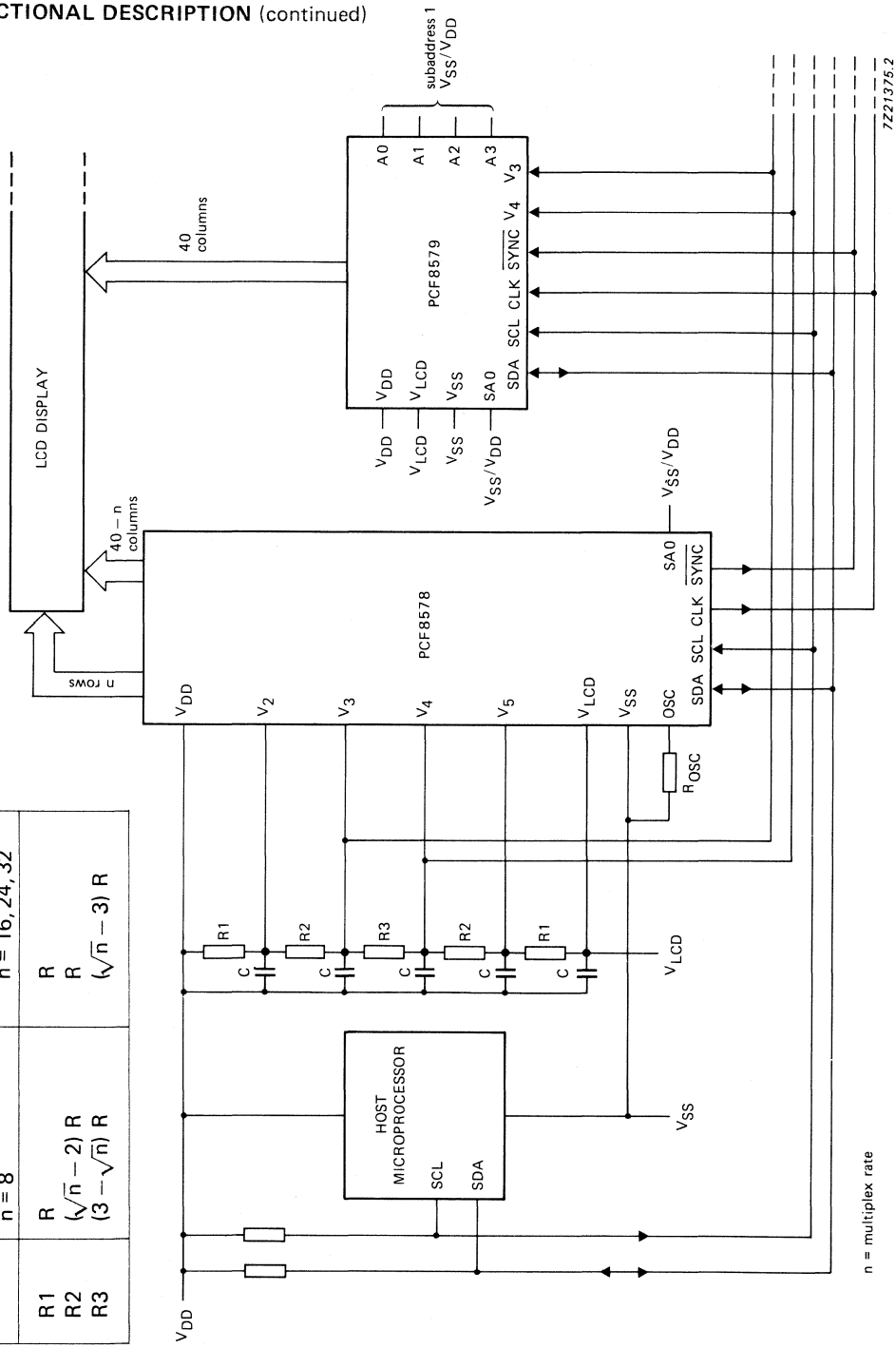
Multiplexed LCD bias generation

The bias levels required to produce maximum contrast depend on the multiplex rate and the LCD threshold voltage (V_{th}). V_{th} is typically defined as the RMS voltage at which the LCD exhibits 10% contrast. Table 2 shows the optimum voltage bias levels for the PCF8578 as functions of V_{op} ($V_{op} = V_{DD} - V_{LCD}$), together with the discrimination ratios (D) for the different multiplex rates. A practical value for V_{op} is obtained by equating $V_{off(rms)}$ with V_{th}.

Table 2 Optimum LCD bias voltages

parameter	multiplex rate			
	1:8	1:16	1:24	1:32
$\frac{V_2}{V_{op}}$	0.739	0.800	0.830	0.850
$\frac{V_3}{V_{op}}$	0.522	0.600	0.661	0.700
$\frac{V_4}{V_{op}}$	0.478	0.400	0.339	0.300
$\frac{V_5}{V_{op}}$	0.261	0.200	0.170	0.150
$\frac{V_{off(rms)}}{V_{op}}$	0.297	0.245	0.214	0.193
$\frac{V_{on(rms)}}{V_{op}}$	0.430	0.316	0.263	0.230
$D = \frac{V_{on(rms)}}{V_{off(rms)}}$	1.447	1.291	1.230	1.196
$\frac{V_{op}}{V_{th}}$	3.37	4.08	4.68	5.19

FUNCTIONAL DESCRIPTION (continued)



	multiplex rate (n)	
	n = 8	n = 16, 24, 32
R1	R	R
R2	$(\sqrt{n} - 2)$ R	R
R3	$(3 - \sqrt{n})$ R	$(\sqrt{n} - 3)$ R

Fig.3 Typical mixed mode configuration.

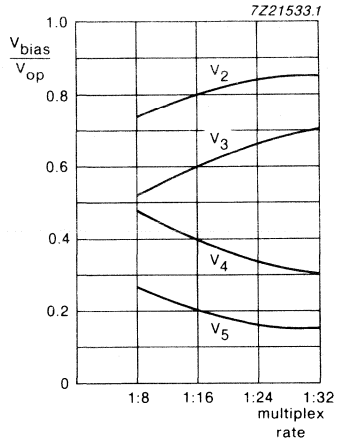


Fig.4 LCD bias voltages as a function of the multiplex rate.

Power-on reset

At power-on the PCF8578 resets to a defined starting condition as follows:

1. Display blank
2. 1:32 multiplex rate, row mode
3. Start bank 0 selected
4. Data pointer is set to X, Y address 0, 0
5. Character mode
6. Subaddress counter is set to 0
7. I²C-bus interface is initialized.

Data transfers on the I²C-bus should be avoided for 1 ms following power-on, to allow completion of the reset action.

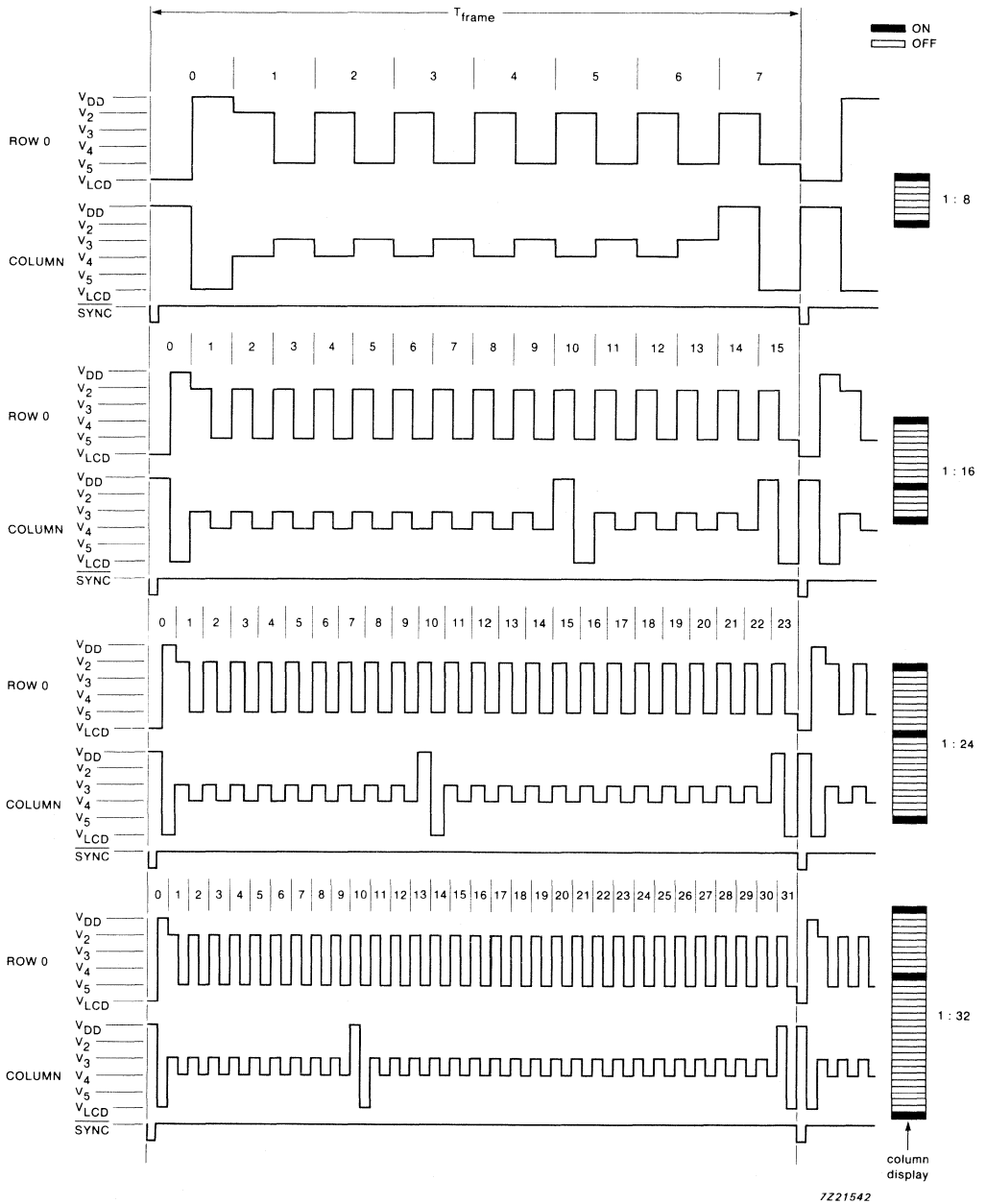
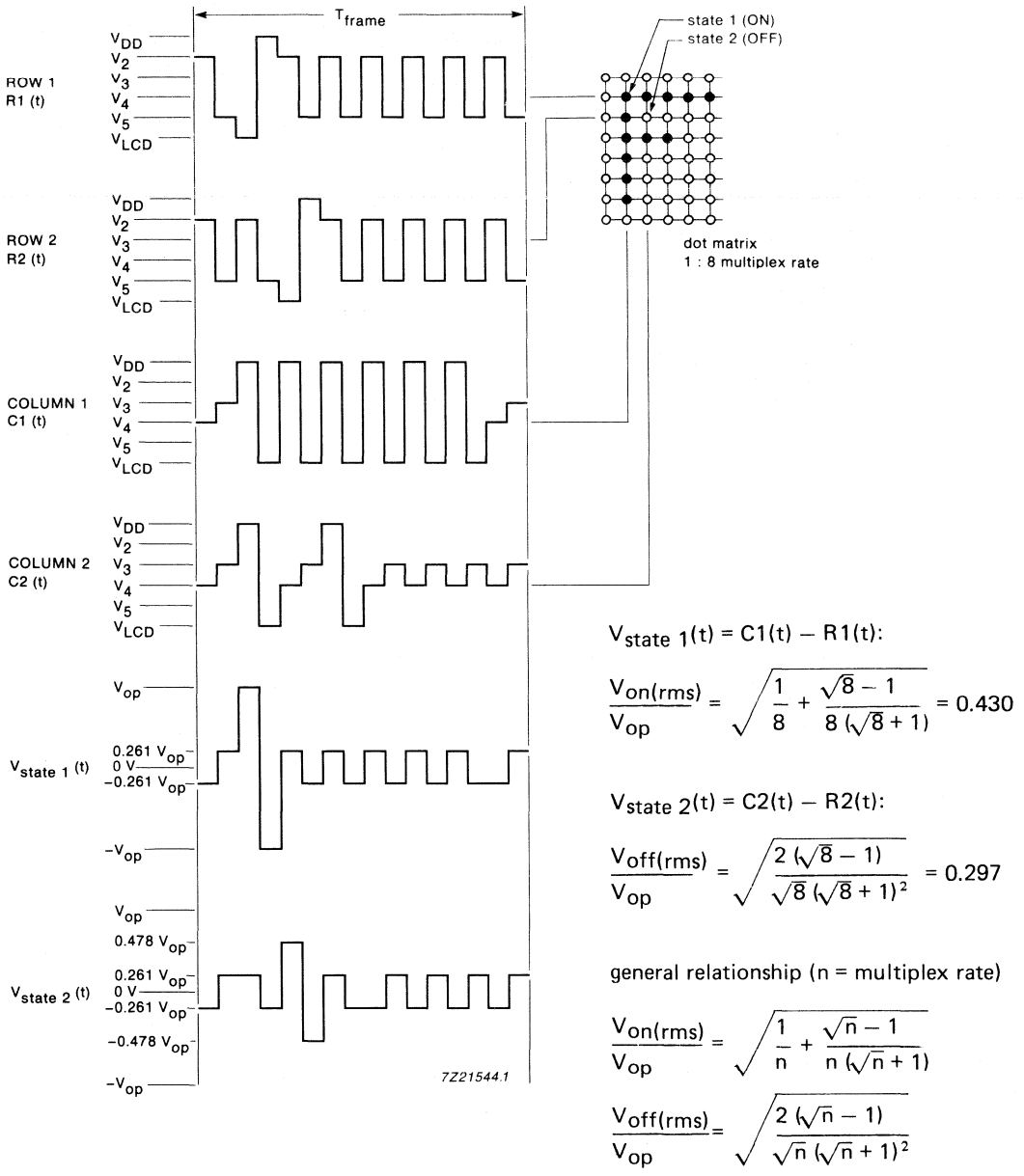


Fig.5 LCD row/column waveforms.

LCD row/column driver for dot matrix graphic displays

PCF8578



$V_{state\ 1}(t) = C1(t) - R1(t)$:

$$\frac{V_{on(rms)}}{V_{op}} = \sqrt{\frac{1}{8} + \frac{\sqrt{8}-1}{8(\sqrt{8}+1)}} = 0.430$$

$V_{state\ 2}(t) = C2(t) - R2(t)$:

$$\frac{V_{off(rms)}}{V_{op}} = \sqrt{\frac{2(\sqrt{8}-1)}{\sqrt{8}(\sqrt{8}+1)^2}} = 0.297$$

general relationship (n = multiplex rate)

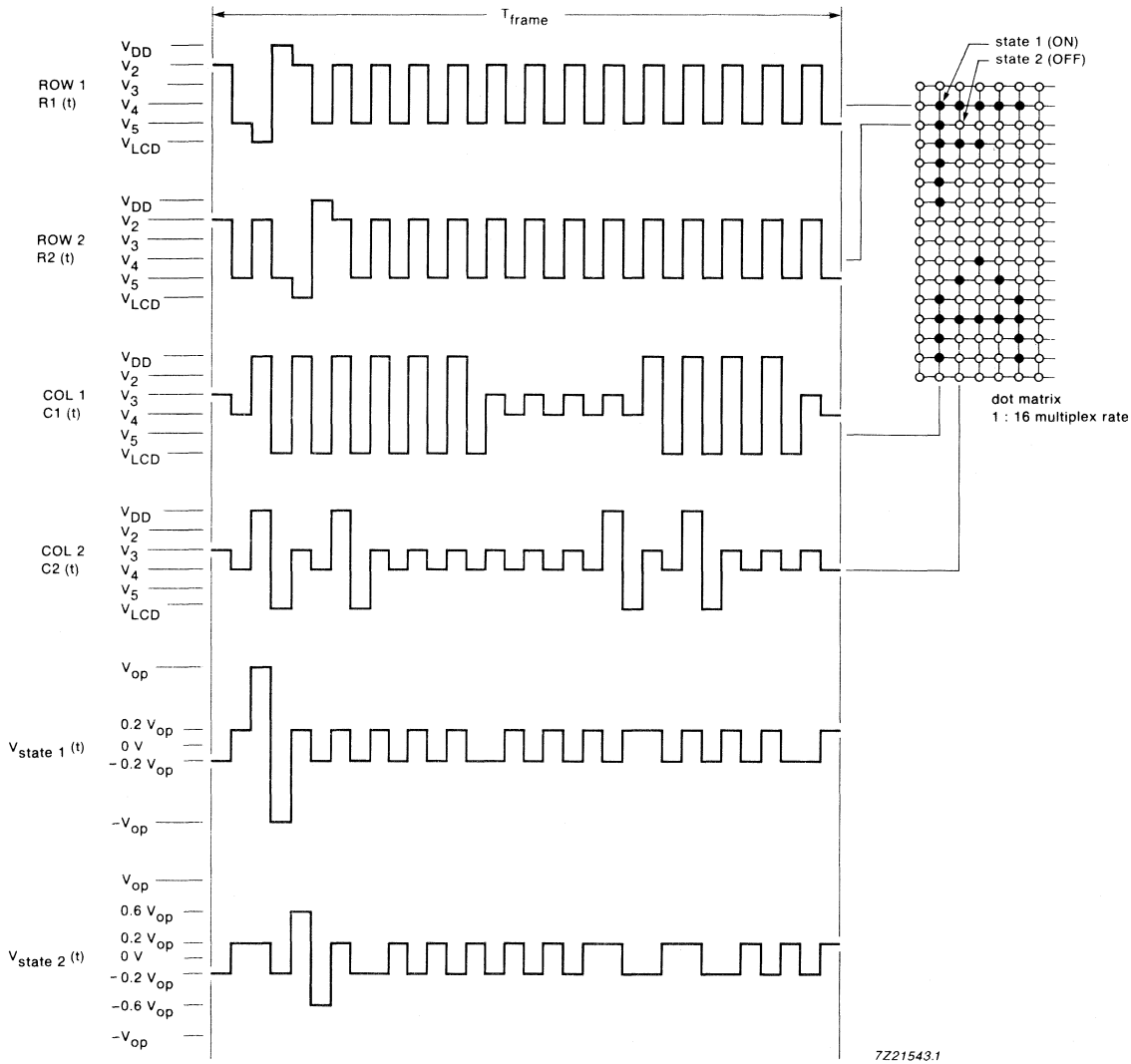
$$\frac{V_{on(rms)}}{V_{op}} = \sqrt{\frac{1}{n} + \frac{\sqrt{n}-1}{n(\sqrt{n}+1)}}$$

$$\frac{V_{off(rms)}}{V_{op}} = \sqrt{\frac{2(\sqrt{n}-1)}{\sqrt{n}(\sqrt{n}+1)^2}}$$

Fig.6 LCD drive mode waveforms for 1:8 multiplex rate.

LCD row/column driver for dot matrix graphic displays

PCF8578



$V_{state\ 1}(t) = C1(t) - R1(t)$:

$$\frac{V_{on(rms)}}{V_{op}} = \sqrt{\frac{1}{16} + \frac{\sqrt{16} - 1}{16\,(\sqrt{16} + 1)}} = 0.316$$

$V_{state\ 2}(t) = C2(t) - R2(t)$:

$$\frac{V_{off(rms)}}{V_{op}} = \sqrt{\frac{2\,(\sqrt{16} - 1)}{\sqrt{16}\,(\sqrt{16} + 1)^2}} = 0.245$$

general relationship (n = multiplex rate)

$$\frac{V_{on(rms)}}{V_{op}} = \sqrt{\frac{1}{n} + \frac{\sqrt{n} - 1}{n\,(\sqrt{n} + 1)}}$$

$$\frac{V_{off(rms)}}{V_{op}} = \sqrt{\frac{2\,(\sqrt{n} - 1)}{\sqrt{n}\,(\sqrt{n} + 1)^2}}$$

Fig.7 LCD drive mode waveforms for 1:16 multiplex rate.

Internal clock

The clock signal for the system may be generated by the internal oscillator and prescaler. The frequency is determined by the value of the resistor R_{OSC}, see Fig.8. For normal use a value of 330 kΩ is recommended. The clock signal, for cascaded PCF8579s, is output at CLK and has a frequency one-sixth (multiplex rate 1:8, 1:16 and 1:32) or one-eighth (multiplex rate 1:24) of the oscillator frequency.

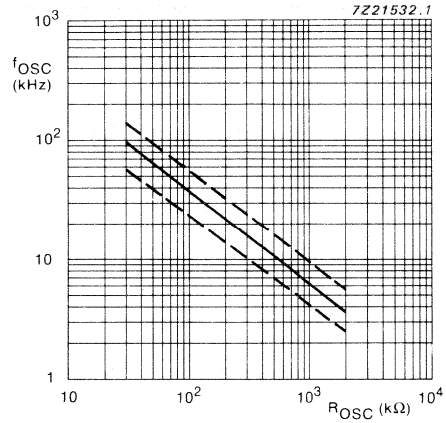


Fig.8 Oscillator frequency as a function of R_{OSC}.

Note

To avoid capacitive coupling, which could adversely affect oscillator stability, R_{OSC} should be placed as closely as possible to the OSC pin. If this proves to be a problem, a filtering capacitor may be connected in parallel to R_{OSC}.

External clock

If an external clock is used, OSC must be connected to V_{DD} and the external clock signal to CLK. Table 3 summarizes the nominal CLK and $\overline{SYNC}$ frequencies.

Table 3 Signal frequencies required for nominal 64 Hz frame frequency

oscillator frequency (R_{OSC} = 330 kΩ) f_{OSC} (Hz)	frame frequency $f_{\overline{SYNC}}$ (Hz)	multiplex rate n	division ratio	clock frequency f_{CLK} (Hz)
12288	64	1:8; 1:16; 1:32	6	2048
12288	64	1:24	8	1536

A clock signal must always be present, otherwise the LCD may be frozen in a DC state.

FUNCTIONAL DESCRIPTION (continued)

Timing generator

The timing generator of the PCF8578 organizes the internal data flow of the device and generates the LCD frame synchronization pulse $\overline{SYNC}$, whose period is an integer multiple of the clock period. In cascaded applications, this signal maintains the correct timing relationship between the PCF8578 and PCF8579s in the system.

Row/column drivers

Outputs R0 to R7 and C32 to C39 are fixed as row and column drivers respectively. The remaining 24 outputs R8/C8 to R31/C31 are programmable and may be configured (in blocks of 8) to be either row or column drivers. The row select signal is produced sequentially at each output from R0 up to the number defined by the multiplex rate (see Table 1). In mixed mode the remaining outputs are configured as columns. In row mode all programmable outputs (R8/C8 to R31/C31) are defined as row drivers and the outputs C32 to C39 should be left open-circuit. Using a 1:16 multiplex rate, two sets of row outputs are driven, thus facilitating split-screen configurations; i.e. a row select pulse appears simultaneously at R0 and R16/C16, R1 and R17/C17 etc. Similarly, using a multiplex rate of 1:8, four sets of row outputs are driven simultaneously. Driver outputs must be connected directly to the LCD. Unused outputs should be left open-circuit.

Display mode controller

The configuration of the outputs (row or column) and the selection of the appropriate driver waveforms are controlled by the display mode controller.

Display RAM

The PCF8578 contains a 32 x 40 bit static RAM which stores the display data. The RAM is divided into 4 banks of 40 bytes (4 x 8 x 40 bits). During RAM access, data is transferred to/from the RAM via the I²C-bus. The first eight columns of data (0 to 7) cannot be displayed but are available for general data storage and provide compatibility with the PCF8579.

Data pointer

The addressing mechanism for the display RAM is realized using the data pointer. This allows an individual data byte or a series of data bytes to be written into, or read from, the display RAM, controlled by commands sent on the I²C-bus.

Subaddress counter

The storage and retrieval of display data is dependent on the content of the subaddress counter. Storage takes place only when the contents of the subaddress counter agree with the hardware subaddress. The hardware subaddress of the PCF8578, valid in mixed mode only, is fixed at 0000.

I²C-bus controller

The I²C-bus controller detects the I²C-bus protocol, slave address, commands and display data bytes. It performs the conversion of the data input (serial-to-parallel) and the data output (parallel-to-serial). The PCF8578 acts as an I²C-bus slave transmitter/receiver in mixed mode, and as a slave receiver in row mode. A slave device cannot control bus communication.

Input filters

To enhance noise immunity in electrically adverse environments, RC low-pass filters are provided on the SDA and SCL lines.

RAM access

RAM operations are only possible when the PCF8578 is in mixed mode. In this event its hardware subaddress is internally fixed at 0000 and the hardware subaddresses of any PCF8579 used in conjunction with the PCF8578 must start at 0001.

There are three RAM ACCESS modes:

- Character
- Half-graphic
- Full-graphic

These modes are specified by bits G1 and G0 of the RAM ACCESS command. The RAM ACCESS command controls the order in which data is written to or read from the RAM (see Fig.9).

To store RAM data, the user specifies the location into which the first byte will be loaded (see Fig.10):

- Device subaddress (specified by the DEVICE SELECT command)
- RAM X-address (specified by the LOAD X-ADDRESS command)
- RAM bank (specified by bits Y1 and Y0 of the RAM ACCESS command)

Subsequent data bytes will be written or read according to the chosen RAM access mode. Device subaddresses are automatically incremented between devices until the last device is reached. If the last device has subaddress 15, further display data transfers will lead to a wrap-around of the subaddress to 0.

Display control

The display is generated by continuously shifting rows of RAM data to the dot matrix LCD via the column outputs. The number of rows scanned depends on the multiplex rate set by bits M1 and M0 of the SET MODE command.

The display status (all dots on/off and normal/inverse video) is set by bits E1 and E0 of the SET MODE command. For bank switching, the RAM bank corresponding to the top of the display is set by bits B1 and B0 of the SET START BANK command. This is shown in Fig.11. This feature is useful when scrolling in alphanumeric applications.

FUNCTIONAL DESCRIPTION (continued)

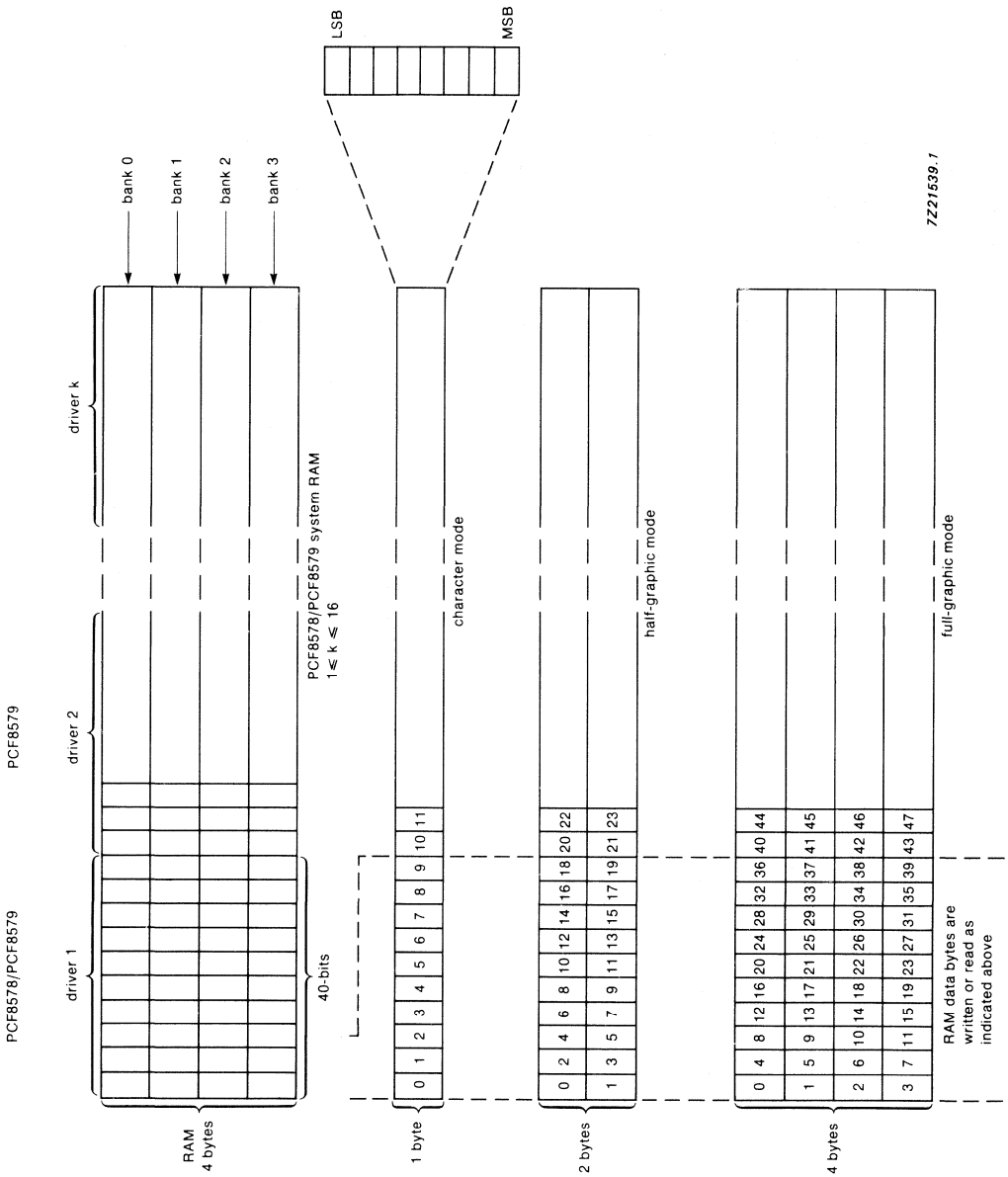


Fig.9 RAM access mode.

LCD row/column driver for dot matrix graphic displays

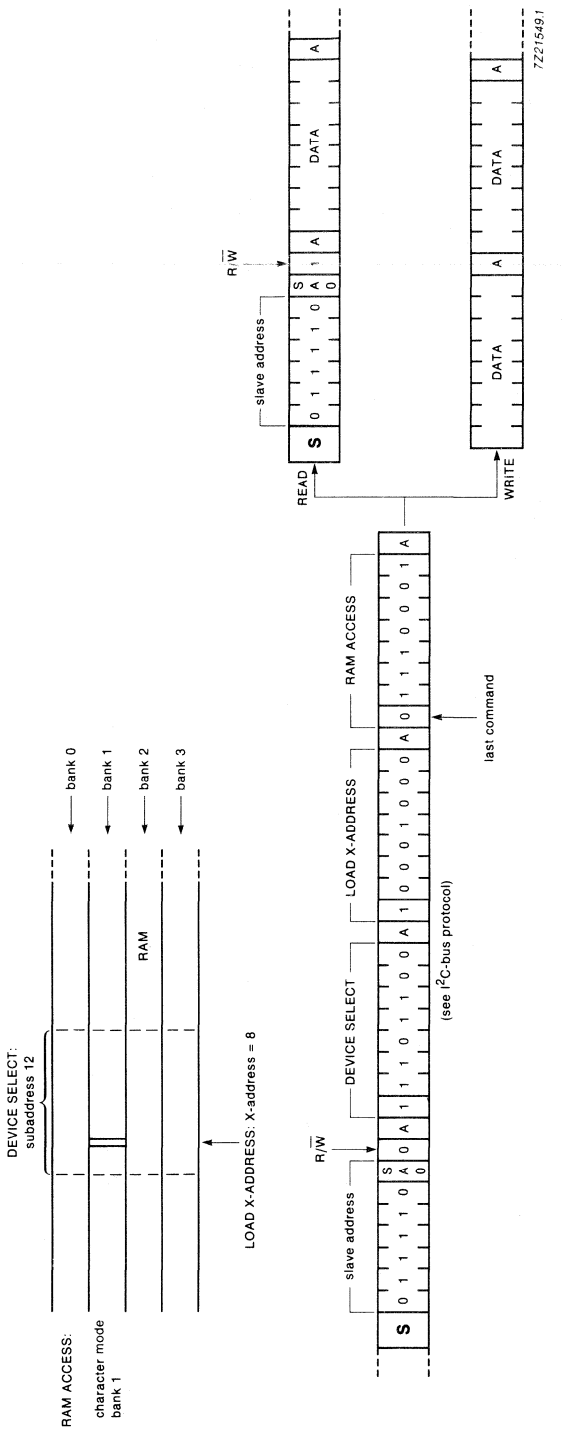


Fig.10 Example of commands specifying initial data byte RAM locations.

FUNCTIONAL DESCRIPTION (continued)

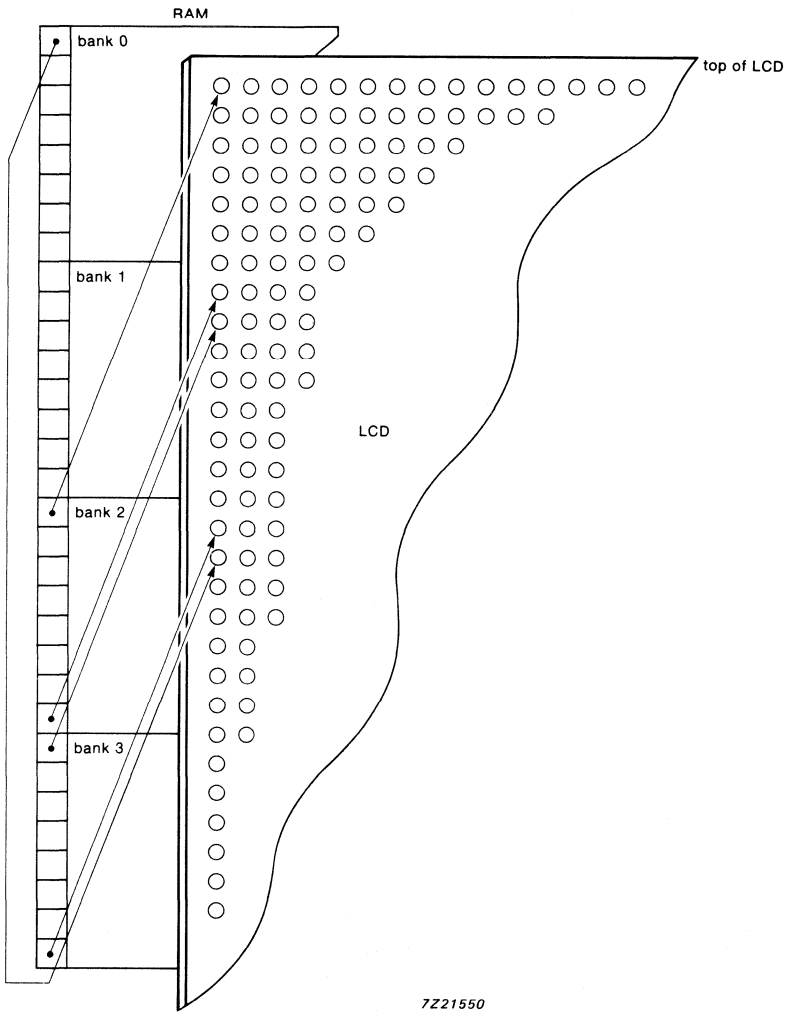


Fig.11 Relationship between display and SET START BANK; 1:32 multiplex rate and start bank = 2.

I²C-BUS PROTOCOL

Two 7-bit slave addresses (0111100 and 0111101) are reserved for both the PCF8578 and PCF8579. The least-significant bit of the slave address is set by connecting input SA0 to either 0 (V_{SS}) or 1 (V_{DD}). Therefore, two types of PCF8578 or PCF8579 can be distinguished on the same I²C-bus which allows:

(a) one PCF8578 to operate with up to 32 PCF8579s on the same I²C-bus for very large applications
(b) the use of two types of LCD multiplex schemes on the same I²C-bus.

In most applications the PCF8578 will have the same slave address as the PCF8579.

The I²C-bus protocol is shown in Fig. 12. All communications are initiated with a start condition (S) from the I²C-bus master, which is followed by the desired slave address and read/write bit. All devices with this slave address acknowledge in parallel. All other devices ignore the bus transfer.

In WRITE mode (indicated by setting the read/write bit LOW) one or more commands follow the slave address acknowledgement. The commands are also acknowledged by all addressed devices on the bus. The last command must clear the continuation bit C. After the last command a series of data bytes may follow. The acknowledgement after each byte is made only by the (A0, A1, A2 and A3) addressed PCF8579 or PCF8578 with its implicit subaddress 0. After the last data byte has been acknowledged, the I²C-bus master issues a stop condition (P).

In READ mode, indicated by setting the read/write bit HIGH, data bytes may be read from the RAM following the slave address acknowledgement. After this acknowledgement the master transmitter becomes a master receiver and the PCF8578 becomes a slave transmitter. The master receiver must acknowledge the reception of each byte in turn. The master receiver must signal an end of data to the slave transmitter, by **not** generating an acknowledge on the last byte clocked out of the slave. The slave transmitter then leaves the data line HIGH, enabling the master to generate a stop condition (P).

Display bytes are written into, or read from, the RAM at the address specified by the data pointer and subaddress counter. Both the data pointer and subaddress counter are automatically incremented, enabling a stream of data to be transferred either to, or from, the intended devices.

In multiple device applications, the hardware subaddress pins of the PCF8579s (A_0 to A_3) are connected to V_{SS} or V_{DD} to represent the desired hardware subaddress code. If two or more devices share the same slave address, then each device **must** be allocated a unique hardware subaddress.

I²C-BUS PROTOCOL (continued)

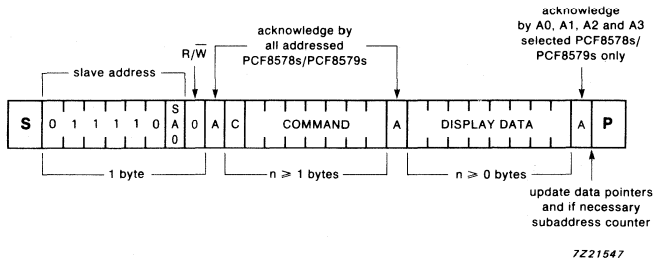


Fig.12(a) Master transmits to slave receiver (WRITE mode).

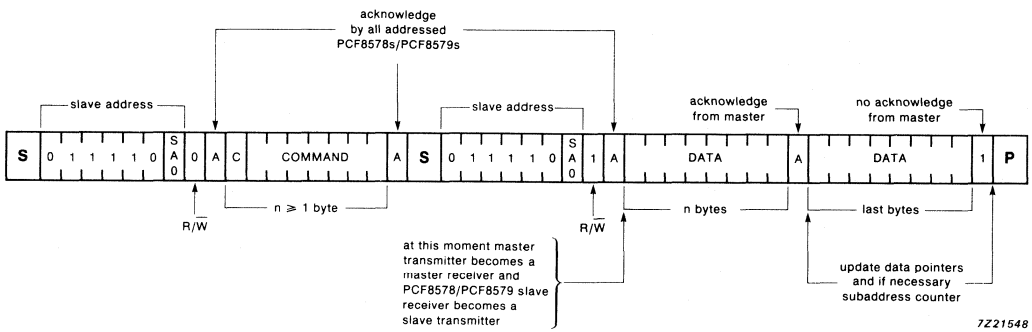


Fig.12(b) Master reads after sending command string (WRITE commands; READ data).

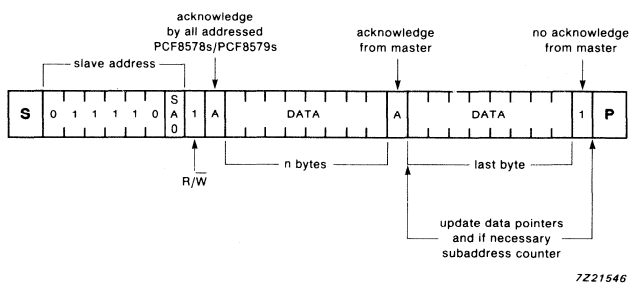
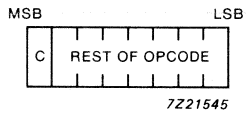


Fig.12(c) Master reads slave immediately after sending slave address (READ mode).

Command decoder

The command decoder identifies command bytes that arrive on the I²C-bus. The most-significant bit of a command is the continuation bit C (see Fig.13). When this bit is set, it indicates that the next byte to be transferred will also be a command. If the bit is reset, it indicates the conclusion of the command transfer. Further bytes will be regarded as display data. Commands are transferred in WRITE mode only.



C = 0; last command
C = 1; commands continue

Fig.13 General format of command byte.

The five commands available to the PCF8578 are defined in Tables 4 and 5.

Table 4 Summary of commands

code	command	description
C 0 D D D D D D	LOAD X-ADDRESS	0 to 39
C 1 0 D D D D D	SET MODE	multiplex rate, display status, system type
C 1 1 0 D D D D	DEVICE SELECT	defines device subaddress
C 1 1 1 D D D D	RAM ACCESS	graphic mode, bank select (D D D D ⩾ 12 is not allowed; see SET START BANK opcode)
C 1 1 1 1 1 D D	SET START BANK	defines bank at top of LCD

Where:

C = command continuation bit
D = may be a logic 1 or 0.

I²C-BUS PROTOCOL (continued)

Table 5 Definition of PCF8578/PCF8579 commands

command / opcode	options	description
SET MODE C 1 0 T E1 E0 M1 M0	LCD drive mode bits M1 M0 1:8 MUX (8 rows) 0 1 1:16 MUX (16 rows) 1 0 1:24 MUX (24 rows) 1 1 1:32 MUX (32 rows) 0 0	defines LCD drive mode
	display status bits E1 E0 blank 0 0 normal 0 1 all segments on 1 0 inverse video 1 1	defines display status
	system type bit T PCF8578 row only 0 PCF8578 mixed mode 1	defines system type
SET START BANK C 1 1 1 1 1 B1 B0	start bank pointer bits B1 B0 bank 0 0 0 bank 1 0 1 bank 2 1 0 bank 3 1 1	defines pointer to RAM bank corresponding to the top of the LCD. Useful for scrolling, pseudo-motion and background preparation of new display
DEVICE SELECT C 1 1 0 A3 A2 A1 A0	bits A3 A2 A1 A0 4-bit binary value of 0 to 15	four bits of immediate data, bits A0 to A3, are transferred to the subaddress counter to define one of sixteen hardware subaddresses

command / opcode	options	description
RAM ACCESS C | 1 1 1 | G1 G0 | Y1 Y0	RAM access mode bits G1 G0 character 0 0 half graphic 0 1 full graphic 1 0 not allowed * 1 1	defines the auto-increment behaviour of the address for RAM access
	bits Y1 Y0 2-bit binary value of 0 to 3	two bits of immediate data, bits Y0 to Y1, are transferred to the Y-address pointer to define one of four banks for RAM access
LOAD X-ADDRESS C 0 X5 X4 X3 X2 X1 X0	bits X5 X4 X3 X2 X1 X0 6-bit binary value of 0 to 39	six bits of immediate data, bits X0 to X5, are transferred to the X-address pointer to define one of forty display RAM columns

CHARACTERISTICS OF THE I²C-BUS

The I²C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL) which must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this moment will be interpreted as control signals.

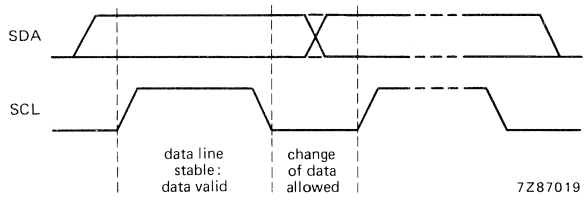


Fig.14 Bit transfer.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH, is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH, is defined as the stop condition (P).

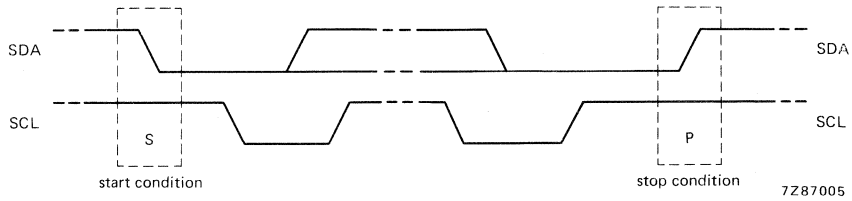


Fig.15 Definition of start and stop condition.

System configuration

A device transmitting a message is a "transmitter", a device receiving a message is the "receiver". The device that controls the message flow is the "master" and the devices which are controlled by the master are the "slaves".

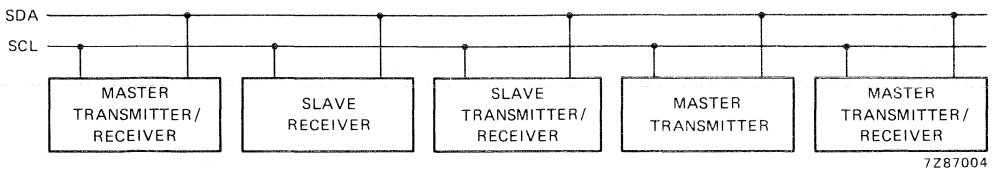


Fig.16 System configuration.

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is unlimited. Each data byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter, whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges must pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal the end of a data transmission to the transmitter by **not** generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

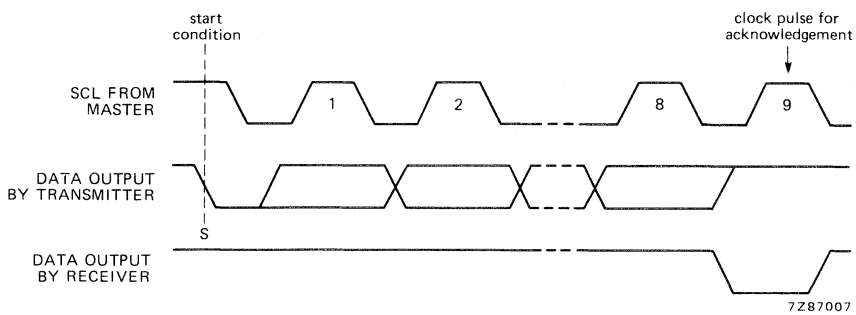


Fig.17 Acknowledgement on the I²C-bus.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage range	V_{DD}	−0.5	+8.0	V
LCD supply voltage range	V_{LCD}	V_{DD} −11	V_{DD}	V
Input voltage range at SDA, SCL, CLK, TEST, SA0 and OSC	V_{I1}	V_{SS} −0.5	V_{DD} +0.5	V
V_2 to V_5	V_{I2}	V_{LCD} −0.5	V_{DD} +0.5	V
Output voltage range at $\overline{SYNC}$ and CLK	V_{O1}	V_{SS} −0.5	V_{DD} +0.5	V
R0 to R7, R8/C8 to R31/C31, and C32 to C39	V_{O2}	V_{LCD} −0.5	V_{DD} +0.5	V
DC input current	I_I	−10	10	mA
DC output current	I_O	−10	10	mA
V_{DD}, V_{SS} or V_{LCD} current	I_{DD}, I_{SS}, I_{LCD}	−50	50	mA
Power dissipation per package	P_{tot}	−	400	mW
Power dissipation per output	P_o	−	100	mW
Storage temperature range	T_{stg}	−65	+150	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

DC CHARACTERISTICS

V_{DD} = 2.5 V to 6.0 V; V_{SS} = 0 V; V_{LCD} = V_{DD} −3.5 V to V_{DD} −9 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage		V_{DD}	2.5	–	6.0	V
LCD supply voltage		V_{LCD}	V_{DD} −9	–	V_{DD} −3.5	V
Supply current	note 1;					
external clock	f_{CLK} = 2 kHz	I_{DD1}	–	6	15	μA
internal clock	R_{OSC} = 330 kΩ	I_{DD2}	–	20	50	μA
Power-on reset level	note 2	V_{POR}	0.8	1.3	1.8	V
Logic						
Input voltage LOW		V_{IL}	V_{SS}	–	0.3 V_{DD}	V
Input voltage HIGH		V_{IH}	0.7 V_{DD}	–	V_{DD}	V
Output current LOW at $\overline{SYNC}$ and CLK	V_{OL} = 1.0 V; V_{DD} = 5 V	I_{OL1}	1	–	–	mA
Output current HIGH at $\overline{SYNC}$ and CLK	V_{OH} = 4.0 V; V_{DD} = 5 V	I_{OH1}	–	–	−1	mA
SDA output current LOW	V_{OL} = 0.4 V; V_{DD} = 5 V	I_{OL2}	3.0	–	–	mA
Leakage current at SDA, SCL, $\overline{SYNC}$, CLK, TEST and SA0	V_I = V_{DD} or V_{SS}	I_{L1}	−1	–	1	μA
Leakage current at OSC	V_I = V_{DD}	I_{L2}	−1	–	1	μA
Input capacitance at SCL and SDA	note 3	C_I	–	–	5	pF
LCD outputs						
Leakage current at V_2 to V_5	V_I = V_{DD} or V_{LCD}	I_{L3}	−2	–	2	μA
DC component of LCD drivers R0 to R7, R8/C8 to R31/C31, and C32 to C39		± V_{DC}	–	20	–	mV
Output resistance at R0 to R7 and R8/C8 to R31/C31	note 4; row mode	R_{ROW}	–	1.5	3.0	kΩ
R8/C8 to R31/C31 and C32 to C39	column mode	R_{COL}	–	3	6	kΩ

AC CHARACTERISTICS (note 5)

V_{DD} = 2.5 to 6 V; V_{SS} = 0 V; V_{LCD} = V_{DD} −3.5 V to V_{DD} −9 V; T_{amb} = − 40 to + 85 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Clock frequency at multiplex rates of 1:8, 1:16 and 1:32	R_{OSC} = 330 kΩ; V_{DD} = 6 V	f_{CLK1}	1.2	2.1	3.3	kHz
1:24		f_{CLK2}	0.9	1.6	2.5	kHz
$\overline{SYNC}$ propagation delay		t_{PSYNC}	–	–	500	ns
Driver delays	V_{DD} − V_{LCD} = 9 V; with test loads	t_{PLCD}	–	–	100	µs
I²C-bus						
SCL clock frequency		f_{SCL}	–	–	100	kHz
Tolerable spike width on bus		t_{SW}	–	–	100	ns
Bus free time		t_{BUF}	4.7	–	–	µs
Start condition set-up time	repeated start codes only	$t_{SU;STA}$	4.7	–	–	µs
Start condition hold time		$t_{HD;STA}$	4.0	–	–	µs
SCL LOW time		t_{LOW}	4.7	–	–	µs
SCL HIGH time		t_{HIGH}	4.0	–	–	µs
SCL and SDA rise time		t_r	–	–	1.0	µs
SCL and SDA fall time		t_f	–	–	0.3	µs
Data set-up time		$t_{SU;DAT}$	250	–	–	ns
Data hold time		$t_{HD;DAT}$	0	–	–	ns
Stop condition set-up time		$t_{SU;STO}$	4.0	–	–	µs

Notes to the characteristics

1. Outputs are open; inputs at V_{DD} or V_{SS}; I²C-bus inactive; external clock with 50% duty factor, (I_{DD1} only).
2. Resets all logic when $V_{DD} < V_{POR}$.
3. Periodically sampled; not 100% tested.
4. Resistance measured between output terminal (R0 to R7, R8/C8 to R31/C31 and C32 to C39) and bias input (V_2 to V_5, V_{DD} and V_{LCD}) when the specified current flows through one output under the following conditions (see Table 2):

   $V_{OP} = V_{DD} - V_{LCD} = 9$ V;

   row mode, R0 to R7 and R8/C8 to R31/C31 (row mode):
   $V_2 - V_{LCD} \geqslant 6.65$ V; $V_5 - V_{LCD} \leqslant 2.35$ V; $I_{LOAD} = 150\ \mu$A

   column mode, R8/C8 to R31/C31 (column mode) and C32 to C39:
   $V_3 - V_{LCD} \geqslant 4.70$ V; $V_4 - V_{LCD} \leqslant 4.30$ V; $I_{LOAD} = 100\ \mu$A.
5. All timing values are referred to V_{IH} and V_{IL} levels with an input voltage swing of V_{SS} to V_{DD}.

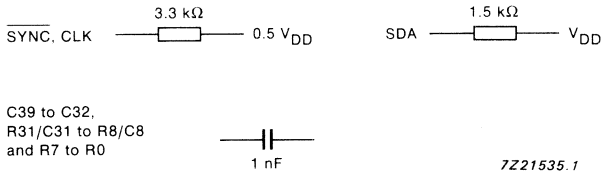


Fig.18 Test loads.

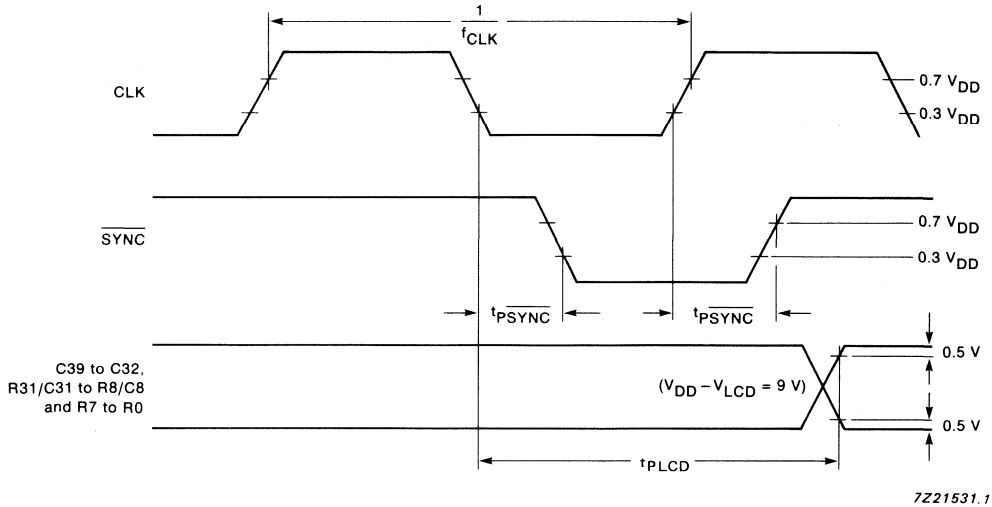


Fig.19 Driver timing waveforms.

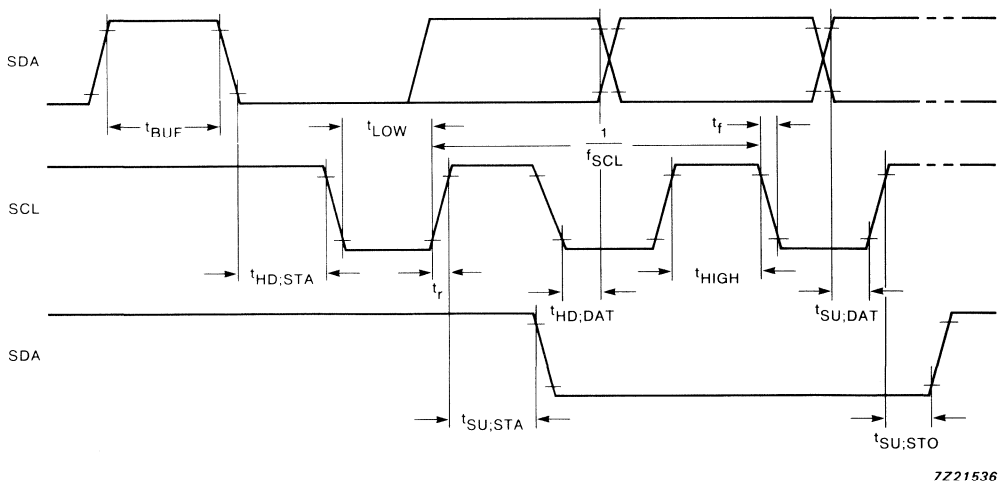


Fig.20 I²C-bus timing waveforms.

APPLICATION INFORMATION

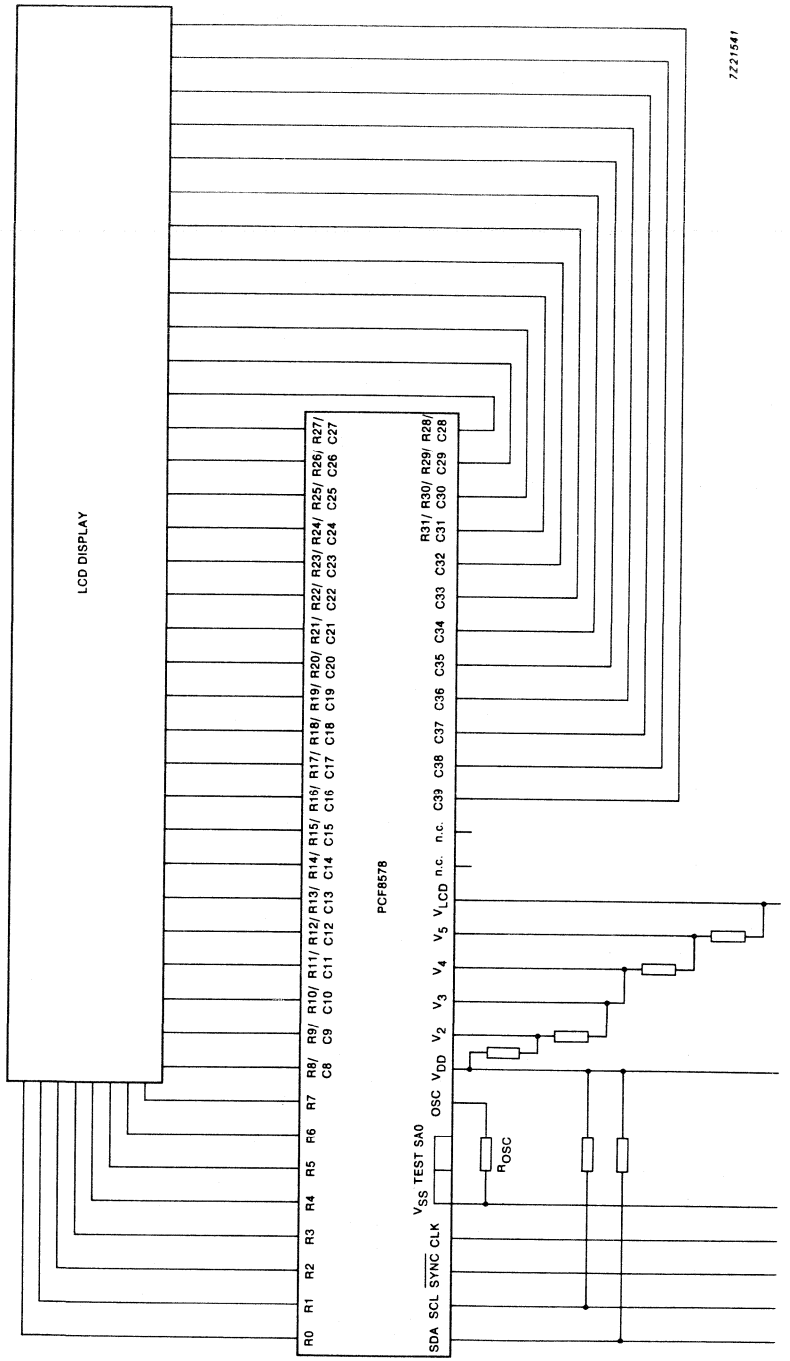


Fig.21 Stand-alone application using 8 rows and 32 columns.

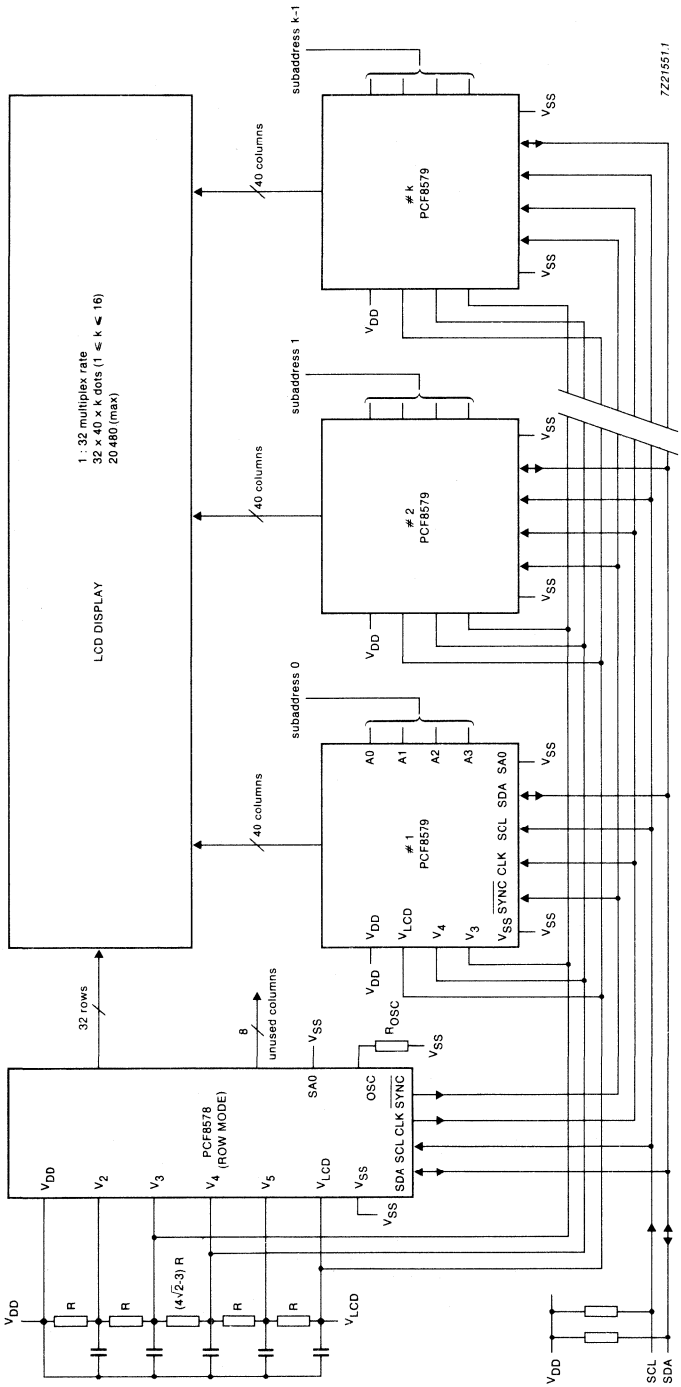


Fig.22 Typical LCD driver system with 1:32 multiplex rate.

LCD row/column driver for dot matrix graphic displays

PCF8578

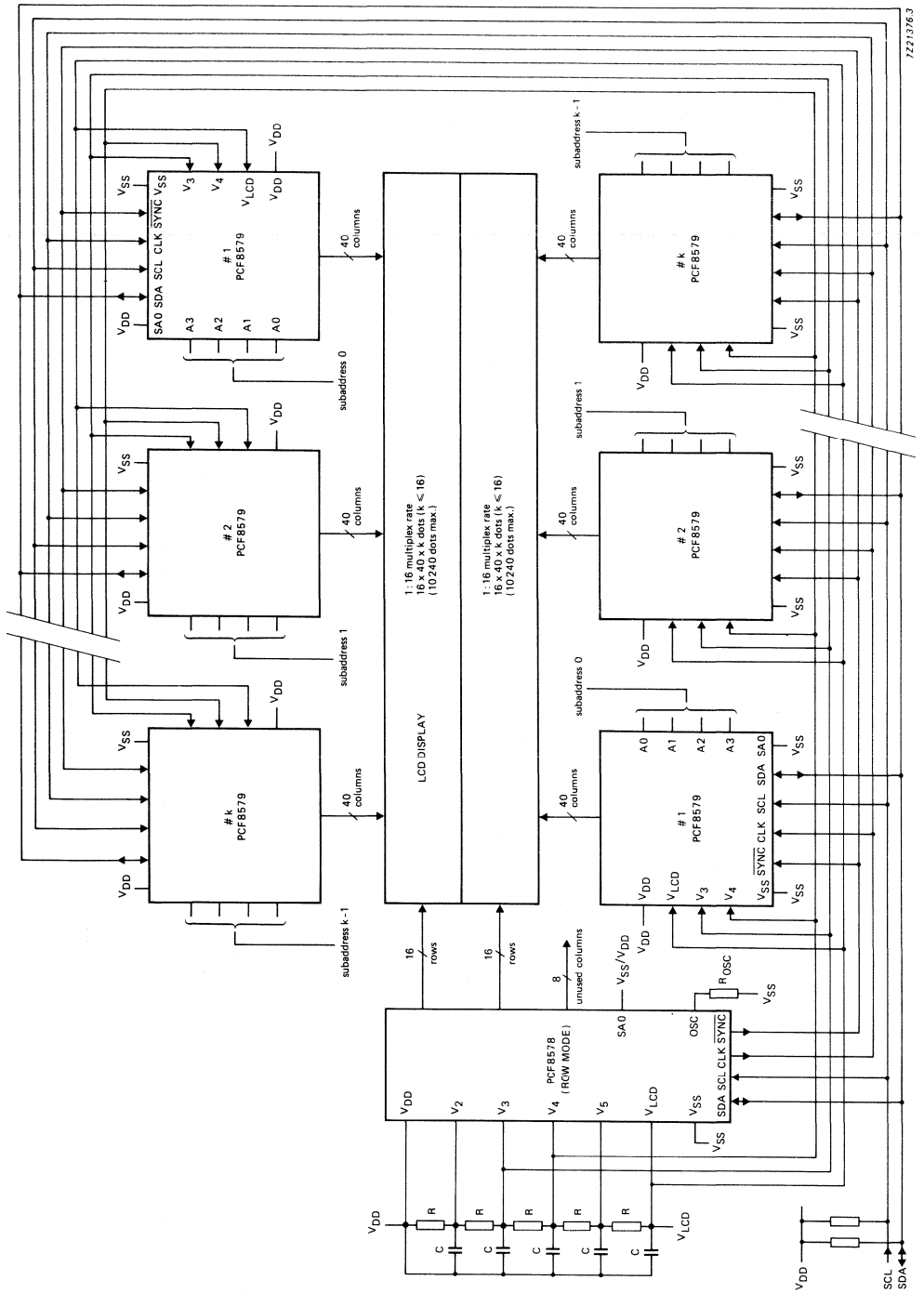


Fig.23 Split screen application with 1:16 multiplex rate for improved contrast.

LCD row/column driver for dot matrix graphic displays

PCF8578

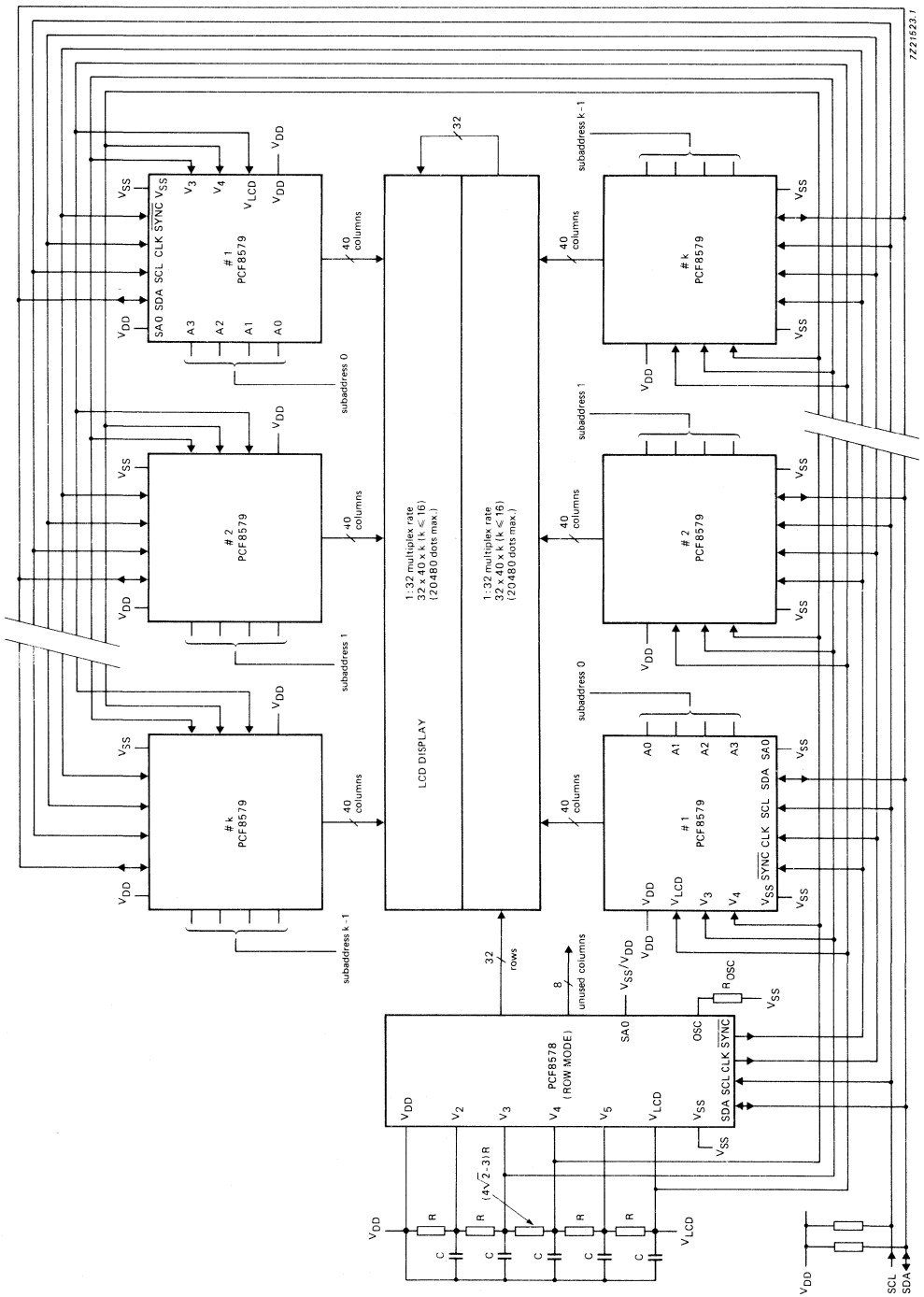


Fig.24 Split screen application with 1:32 multiplex rate.

LCD row/column driver for dot matrix graphic displays

PCF8578

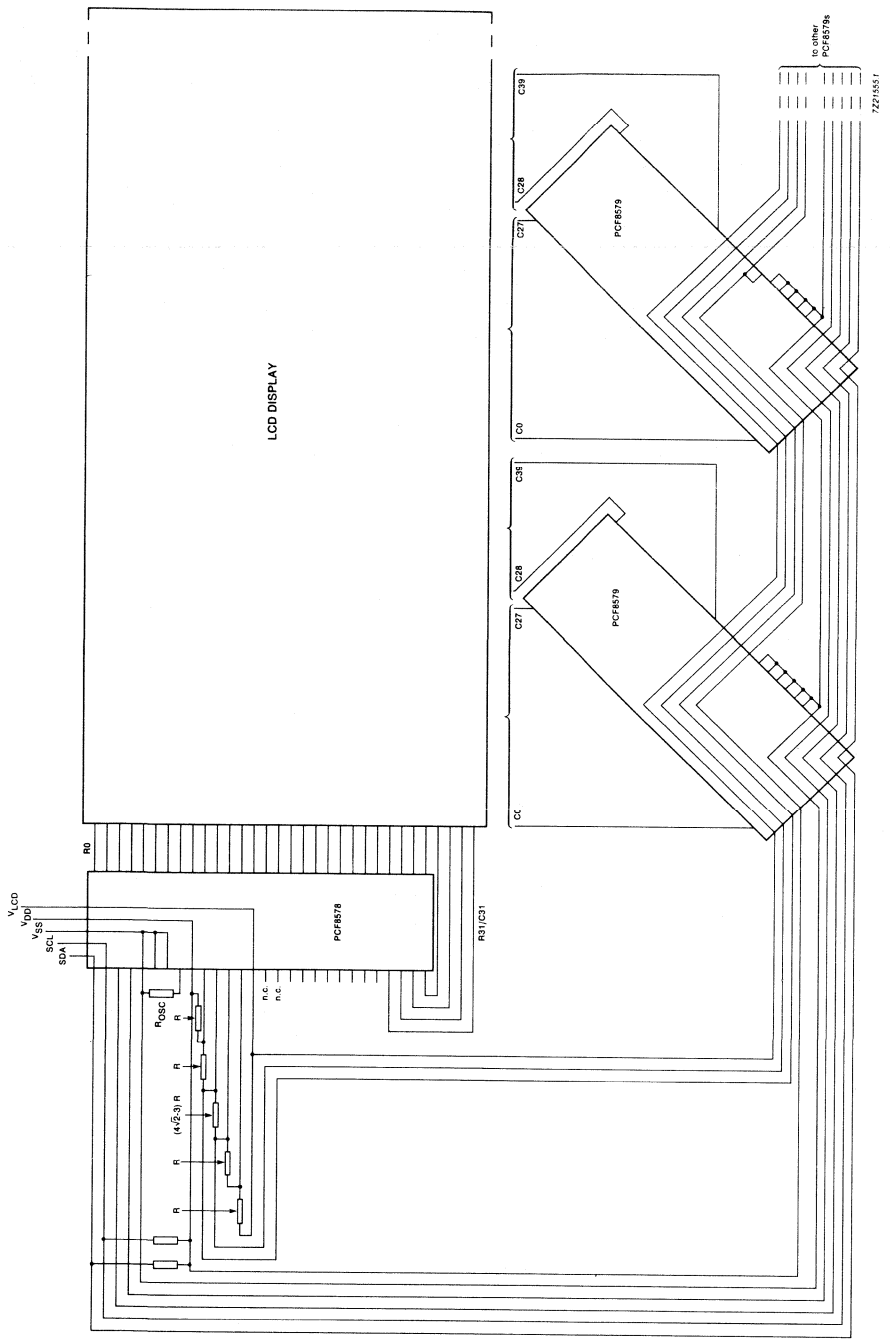


Fig.25 Example of single plane wiring, single screen with 1:32 multiplex rate (PCF8578 in row driver mode).

LCD column driver for dot matrix graphic displays

PCF8579

GENERAL DESCRIPTION

The PCF8579 is a low power CMOS LCD column driver, designed to drive dot matrix graphic displays at multiplex rates of 1:8, 1:16, 1:24 or 1:32. The device has 40 outputs and can drive 32 x 40 dots in a 32 row multiplexed LCD. Up to 16 PCF8579s can be cascaded and up to 32 devices may be used on the same I²C-bus (using the two slave addresses). The device is optimized for use with the PCF8578 LCD row/column driver. Together these two devices form a general LCD dot matrix driver chip set, capable of driving displays of up to 40,960 dots. The PCF8579 is compatible with most microcontrollers and communicates via a two-line bidirectional bus (I²C-bus). Communication overheads are minimized by a display RAM with auto-incremented addressing and display bank switching.

Features

- LCD column driver
- Used in conjunction with the PCF8578, this device forms part of a chip set capable of driving up to 40,960 dots
- 40 column outputs
- Selectable multiplex rates; 1:8, 1:16, 1:24 or 1:32
- Externally selectable bias configuration, 5 or 6 levels
- Easily cascadable for large applications (up to 32 devices)
- 1280-bit RAM for display data storage
- Display memory bank switching
- Auto-incremented data loading across hardware subaddress boundaries
- Power-on reset blanks display
- Logic voltage supply range 2.5 V to 6.0 V
- Maximum LCD supply voltage 9 V
- Low power consumption
- I²C-bus interface
- TTL/CMOS compatible
- Compatible with most microcontrollers
- Optimized pinning for single plane wiring in multiple device applications
- Space saving 56-lead plastic mini-pack
- Compatible with chip-on-glass technology

APPLICATIONS

- Automotive information systems
- Telecommunication systems
- Point-of-sale terminals
- Computer terminals
- Instrumentation

PACKAGE OUTLINES

PCF8579T: 56-lead mini-pack; plastic (VSO56; SOT190).
PCF8579V: 64-lead tape-automated-bonding module (SOT267A).
PCF8579U: chip with bumps on-tape.

LCD column driver for dot matrix graphic displays

PCF8579

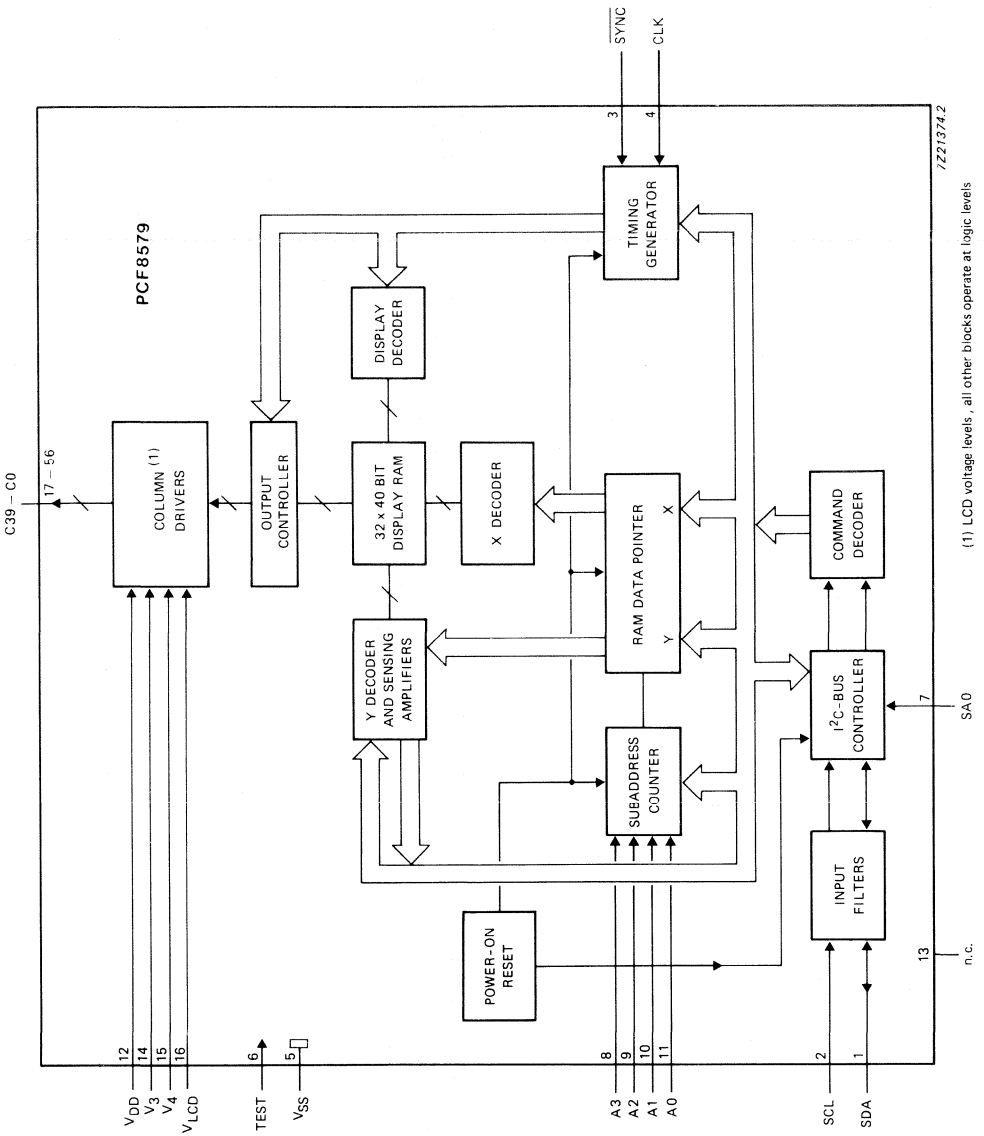


Fig.1 Block diagram.

PINNING

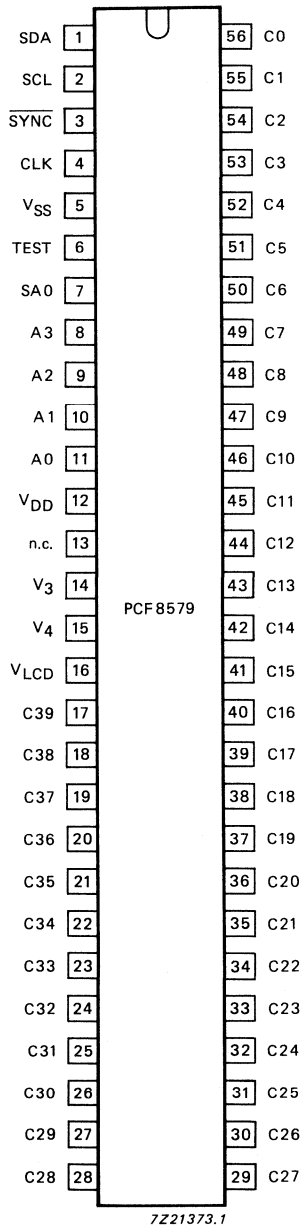
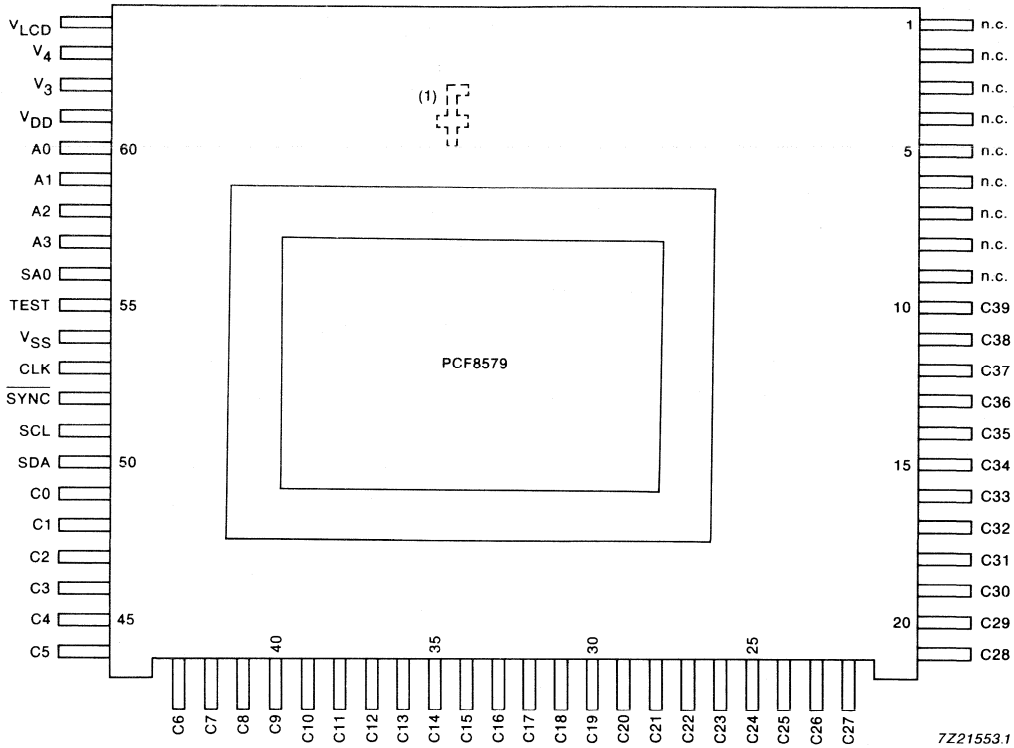


Fig.2 (a) Pinning diagram: VSO56; SOT190.

PINNING (continued)



(1) Orientation mark.

Fig.2 (b) Pinning diagram: SO122.

mnemonic	pin no.		description
	SOT190	SO122	
SDA	1	50	I²C-bus serial data line
SCL	2	51	I²C-bus serial clock line
$\overline{SYNC}$	3	52	cascade synchronization input
CLK	4	53	external clock input
V_{SS}	5	54	ground (logic)
TEST	6	55	test pin (connect to V_{SS})
SA0	7	56	I²C-bus slave address input (bit 0)
A3 to A0	8 - 11	57 - 60	I²C-bus subaddress inputs
V_{DD}	12	61	positive supply voltage
n.c.	13 *	1 - 9	not connected
V_3 to V_4	14 - 15	62 - 63	LCD bias voltage inputs
V_{LCD}	16	64	LCD supply voltage
C39 to C0	17 - 56	10 - 49	LCD column driver outputs

* Do not connect, this pin is reserved.

FUNCTIONAL DESCRIPTION

The PCF8579 column driver is designed for use with the PCF8578. Together they form a general purpose LCD dot matrix chip set.

Typically up to 16 PCF8579s may be used with one PCF8578. Each of the PCF8579s is identified by a unique 4-bit hardware subaddress, set by pins A0 to A3. The PCF8578 can operate with up to 32 PCF8579s when using two I²C-bus slave addresses. The two slave addresses are set by the logic level on input SA0.

Multiplexed LCD bias generation

The bias levels required to produce maximum contrast depend on the multiplex rate and the LCD threshold voltage (V_{th}). V_{th} is typically defined as the RMS voltage at which the LCD exhibits 10% contrast. Table 1 shows the optimum voltage bias levels for the PCF8578/PCF8579 chip set as functions of V_{op} ($V_{op} = V_{DD} - V_{LCD}$), together with the discrimination ratios (D) for the different multiplex rates. A practical value for V_{op} is obtained by equating $V_{off(rms)}$ with V_{th}.

Table 1 Optimum LCD bias voltages

parameter	multiplex rate			
	1:8	1:16	1:24	1:32
$\frac{V_2}{V_{op}}$	0.739	0.800	0.830	0.850
$\frac{V_3}{V_{op}}$	0.522	0.600	0.661	0.700
$\frac{V_4}{V_{op}}$	0.478	0.400	0.339	0.300
$\frac{V_5}{V_{op}}$	0.261	0.200	0.170	0.150
$\frac{V_{off(rms)}}{V_{op}}$	0.297	0.245	0.214	0.193
$\frac{V_{on(rms)}}{V_{op}}$	0.430	0.316	0.263	0.230
$D = \frac{V_{on(rms)}}{V_{off(rms)}}$	1.447	1.291	1.230	1.196
$\frac{V_{op}}{V_{th}}$	3.37	4.08	4.68	5.19

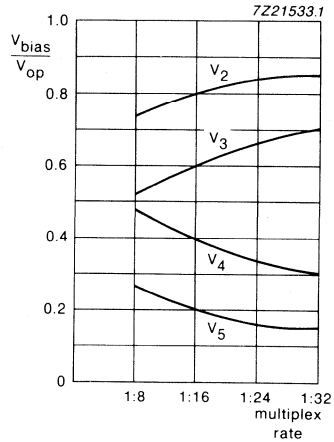


Fig.3 LCD bias voltage as a function of the multiplex rate.

Power-on reset

At power-on the PCF8579 resets to a defined starting condition as follows.

1. Display blank (in conjunction with PCF8578)
2. 1:32 multiplex rate
3. start bank 0 selected
4. Data pointer is set to X, Y address 0, 0
5. Character mode
6. Subaddress counter is set to 0
7. I²C-bus is initialized.

Data transfers on the I²C-bus should be avoided for 1 ms following power-on, to allow completion of the reset action.

FUNCTIONAL DESCRIPTION (continued)

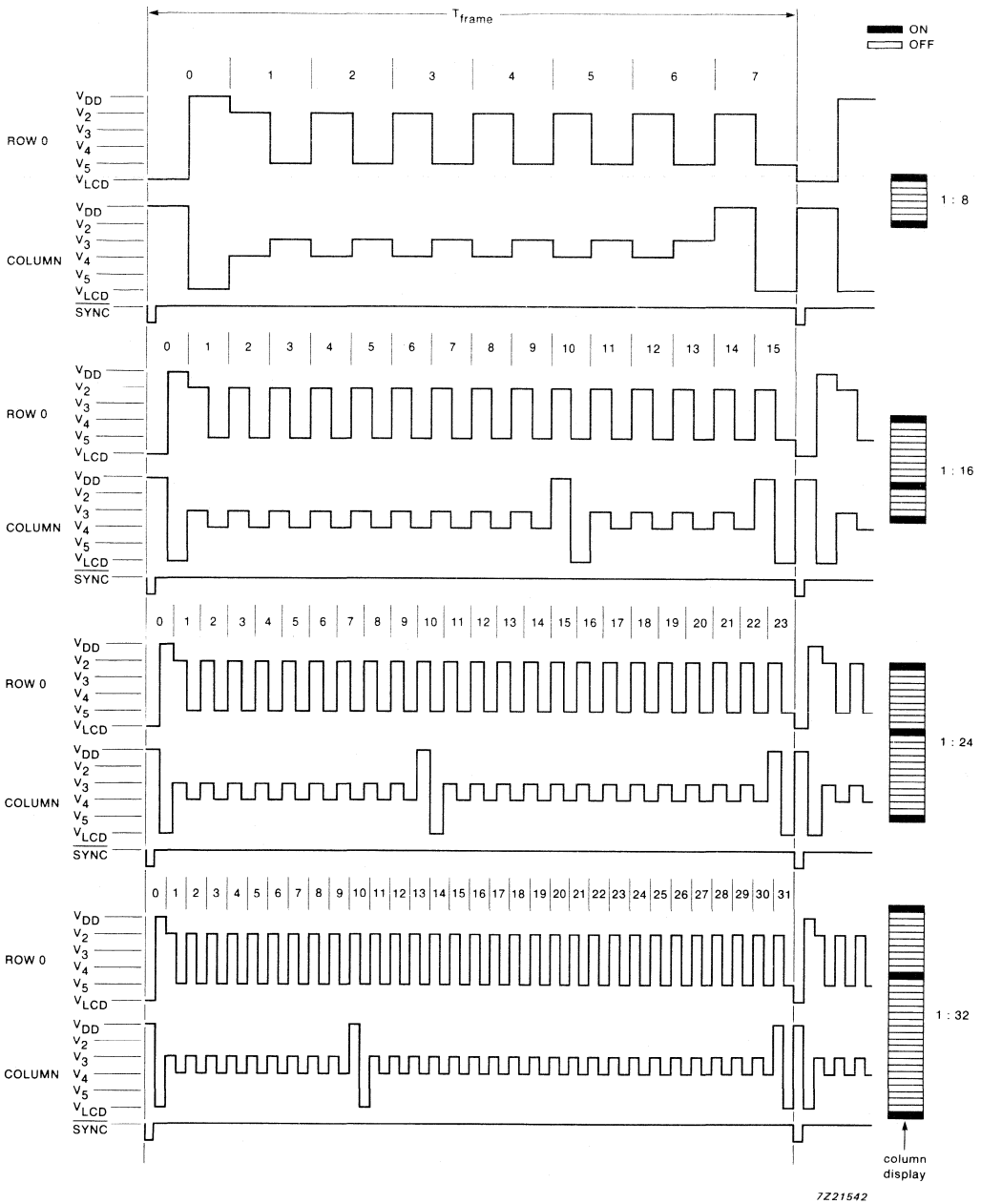


Fig.4 LCD row/column waveforms.

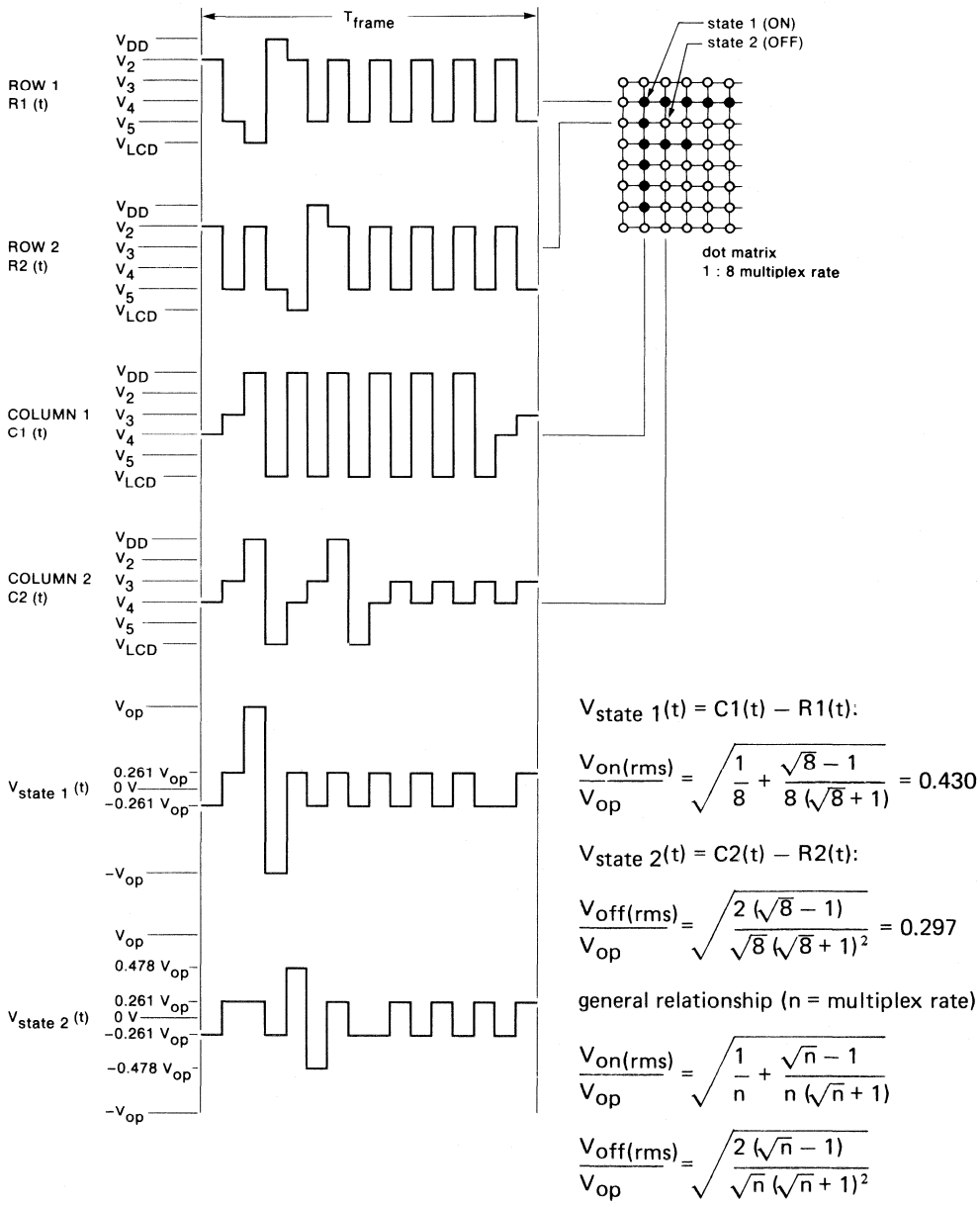
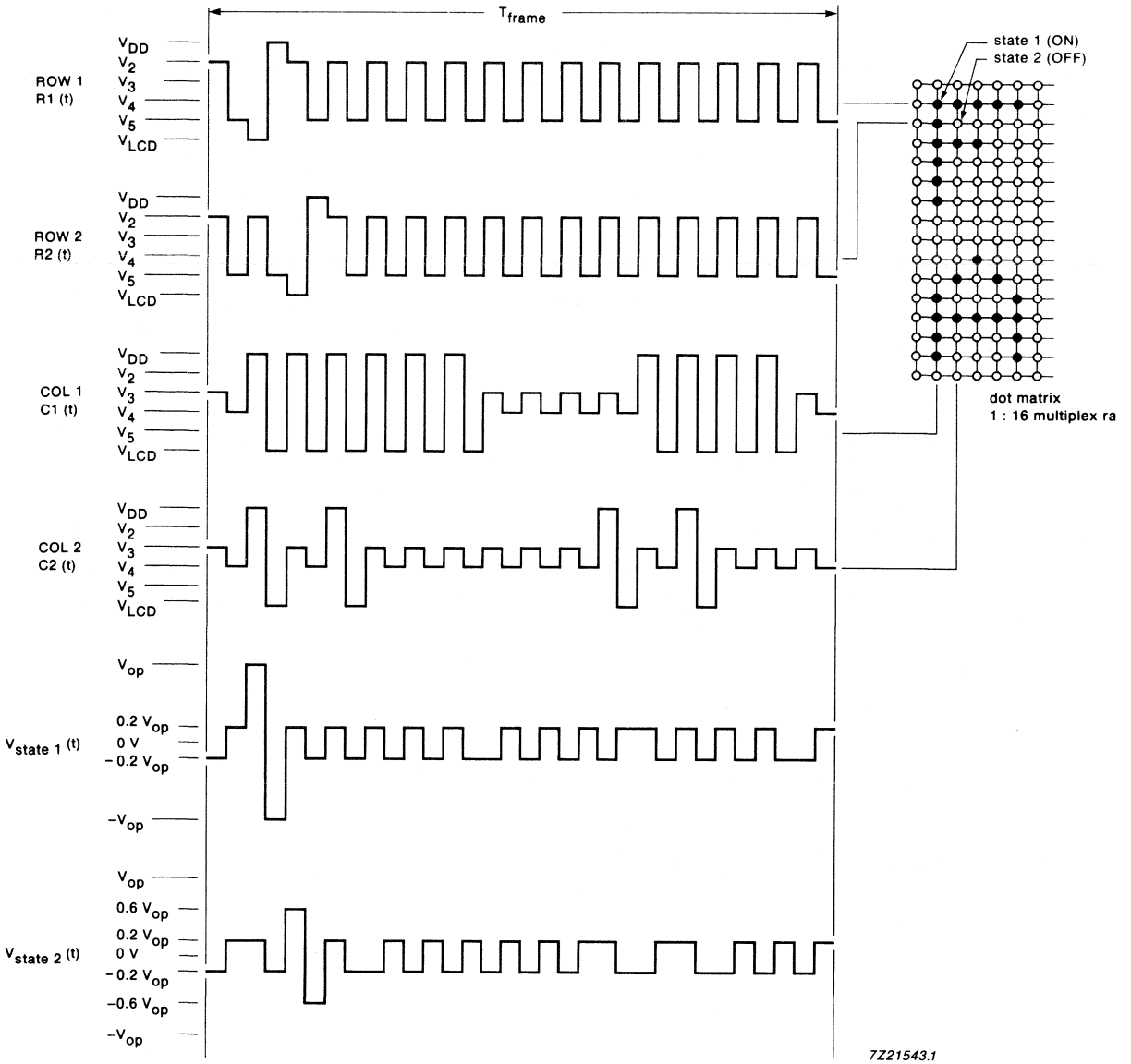


Fig.5 LCD drive mode waveforms for 1:8 multiplex rate.



$V_{state\ 1}(t) = C1(t) - R1(t)$:

$$\frac{V_{on(rms)}}{V_{op}} = \sqrt{\frac{1}{16} + \frac{\sqrt{16} - 1}{16\,(\sqrt{16} + 1)}} = 0.316$$

$V_{state\ 2}(t) = C2(t) - R2(t)$:

$$\frac{V_{off(rms)}}{V_{op}} = \sqrt{\frac{2\,(\sqrt{16} - 1)}{\sqrt{16}\,(\sqrt{16} + 1)^2}} = 0.245$$

general relationship (n = multiplex rate)

$$\frac{V_{on(rms)}}{V_{op}} = \sqrt{\frac{1}{n} + \frac{\sqrt{n} - 1}{n\,(\sqrt{n} + 1)}}$$

$$\frac{V_{off(rms)}}{V_{op}} = \sqrt{\frac{2\,(\sqrt{n} - 1)}{\sqrt{n}\,(\sqrt{n} + 1)^2}}$$

Fig.6 LCD drive mode waveforms for 1:16 multiplex rate.

Timing generator

The timing generator of the PCF8579 organizes the internal data flow from the RAM to the display drivers. An external synchronization pulse $\overline{SYNC}$ is received from the PCF8578. This signal maintains the correct timing relationship between cascaded devices.

Column drivers

Outputs C0 to C39 are column drivers which must be connected to the LCD. Unused outputs should be left open-circuit.

Display RAM

The PCF8579 contains a 32 x 40 bit static RAM which stores the display data. The RAM is divided into 4 banks of 40 bytes (4 x 8 x 40 bits). During RAM access, data is transferred to/from the RAM via the I²C-bus.

Data pointer

The addressing mechanism for the display RAM is realized using the data pointer. This allows an individual data byte or a series of data bytes to be written into or read from the display RAM, as specified by commands sent on the I²C-bus.

Subaddress counter

The storage and retrieval of display data is dependent on the content of the subaddress counter. Storage and retrival take place, only when the contents of the subaddress counter agree with the hardware subaddress at pins A0, A1, A2 and A3.

I²C-bus controller

The I²C-bus controller detects the I²C-bus protocol, slave address, commands and display data bytes. It performs the conversion of the data input (serial-to-parallel) and the data output (parallel-to-serial). The PCF8579 acts as an I²C-bus slave transmitter/receiver. Device selection depends on the I²C-bus slave address, the hardware subaddress and the commands transmitted.

Input filters

To enhance noise immunity in electrically adverse environments, RC low-pass filters are provided on the SDA and SCL lines.

RAM access

There are three RAM ACCESS modes:

- Character
- Half-graphic
- Full-graphic

These modes are specified by bits G1 and G0 of the RAM ACCESS command. The RAM ACCESS command controls the order in which data is written to or read from the RAM (see Fig.7).

To store RAM data, the user specifies the location into which the first byte will be loaded (see Fig.8):

- Device subaddress (specified by the DEVICE SELECT command)
- RAM X-address (specified by the LOAD X-ADDRESS command)
- RAM bank (specified by bits Y1 and Y0 of the RAM ACCESS command)

Subsequent data bytes will be written or read according to the chosen RAM access mode. Device subaddresses are automatically incremented between devices until the last device is reached. If the last device has subaddress 15, further display data transfers will lead to a wrap-around of the subaddress to 0.

Display control

The display is generated by continuously shifting rows of RAM data to the dot matrix LCD, via the column outputs. The number of rows scanned depends on the multiplex rate set by bits M1 and M0 of the SET MODE command.

The display status (all dots on/off and normal/inverse video) is set by bits E1 and E0 of the SET MODE command. For bank switching, the RAM bank corresponding to the top of the display is set by bits B1 and B0 of the SET START BANK command. This is shown in Fig.9. This feature is useful when scrolling in alphanumeric applications.

LCD column driver for dot matrix graphic displays

PCF8579

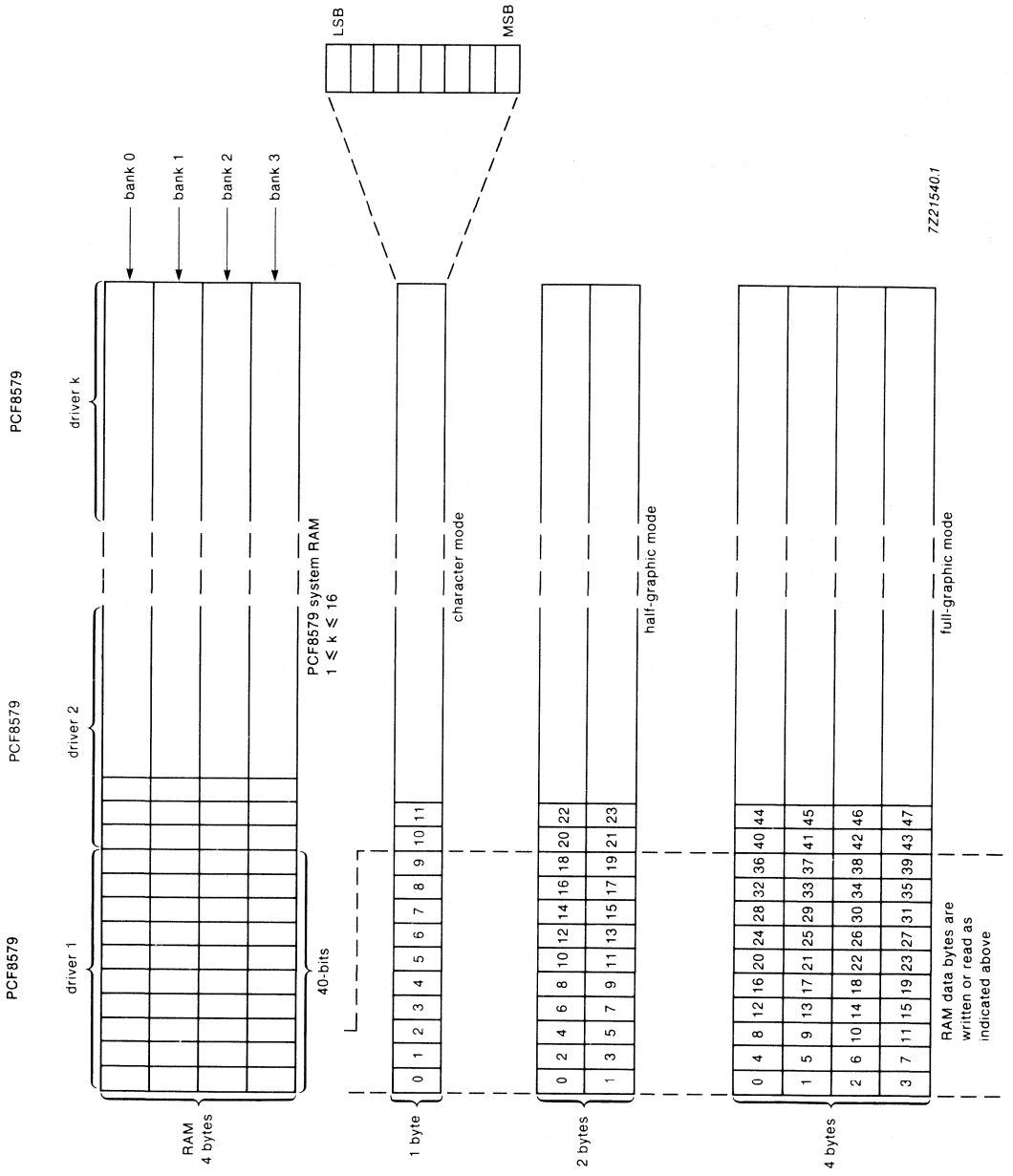


Fig.7 RAM ACCESS mode.

LCD column driver for dot matrix graphic displays

PCF8579

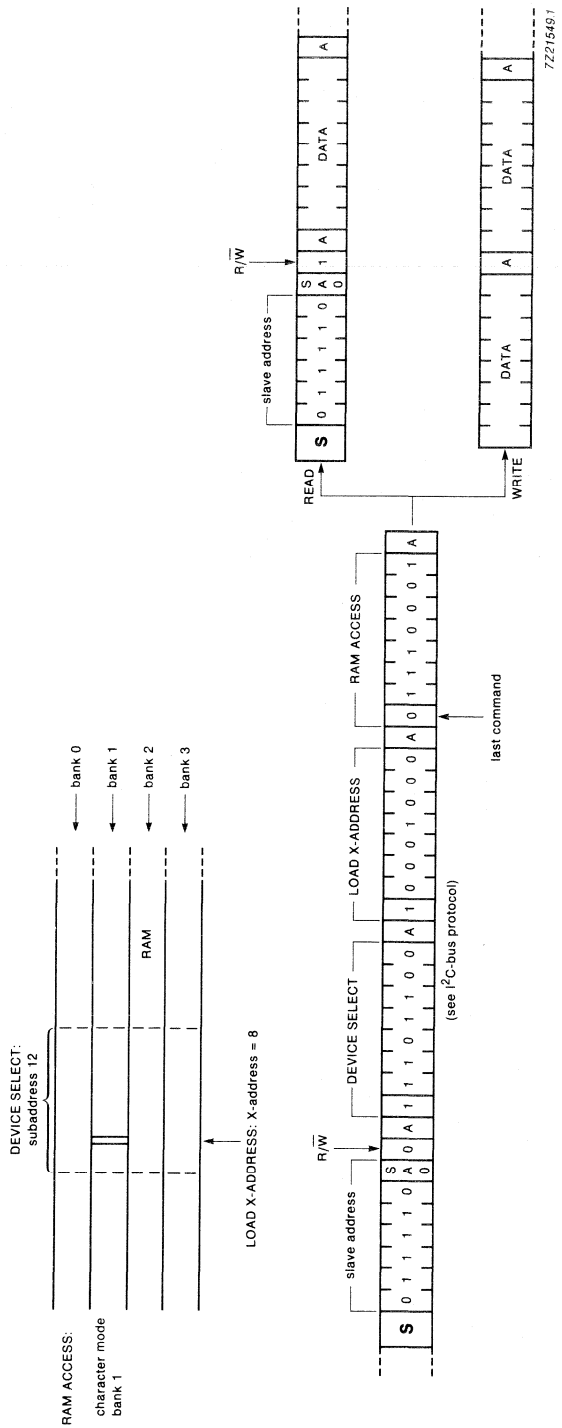


Fig.8 Example of commands specifying initial data byte RAM locations.

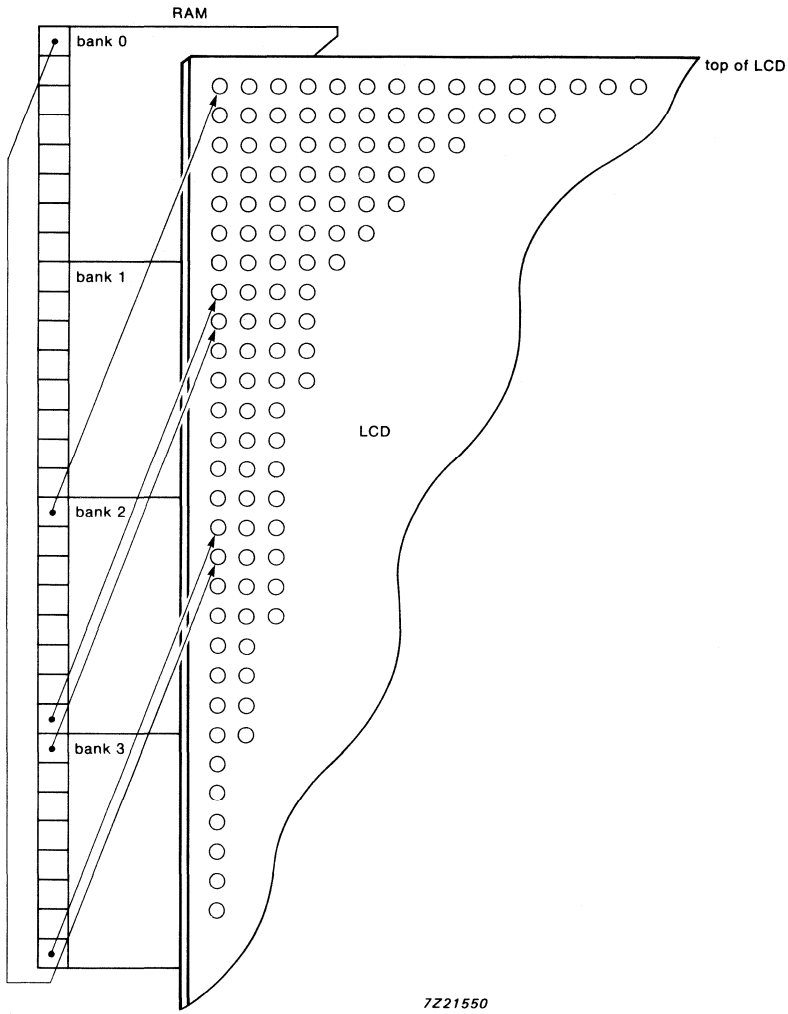


Fig.9 Relationship between display and SET START BANK; 1:32 multiplex rate and start bank = 2.

I²C-BUS PROTOCOL

Two 7-bit slave addresses (0111100 and 0111101) are reserved for both the PCF8578 and PCF8579. The least-significant bit of the slave address is set by connecting input SA0 to either 0 (V_{SS}) or 1 (V_{DD}). Therefore, two types of PCF8578 or PCF8579 can be distinguished on the same I²C-bus which allows:

(a) one PCF8578 to operate with up to 32 PCF8579s on the same I²C-bus for very large applications.
(b) the use of two types of LCD multiplex schemes on the same I²C-bus.

In most applications the PCF8578 will have the same slave address as the PCF8579.

The I²C-bus protocol is shown in Fig. 10. All communications are initiated with a start condition (S) from the I²C-bus master, which is followed by the desired slave address and read/write bit. All devices with this slave address acknowledge in parallel. All other devices ignore the bus transfer.

In WRITE mode (indicated by setting the read/write bit LOW) one or more commands follow the slave address acknowledgement. The commands are also acknowledged by all addressed devices on the bus. The last command must clear the continuation bit C. After the last command a series of data bytes may follow. The acknowledgement after each byte is made only by the (A0, A1, A2 and A3) addressed PCF8579 or PCF8578 with its implicit subaddress 0. After the last data byte has been acknowledged, the I²C-bus master issues a stop condition (P).

In READ mode, indicated by setting the read/write bit HIGH, data bytes may be read from the RAM following the slave address acknowledgement. After this acknowledgement the master transmitter becomes a master receiver and the PCF8579 becomes a slave transmitter. The master receiver must acknowledge the reception of each byte in turn. The master receiver must signal an end of data to the slave transmitter, by **not** generating an acknowledge on the last byte clocked out of the slave. The slave transmitter then leaves the data line HIGH, enabling the master to generate a stop condition (P).

Display bytes are written into, or read from, the RAM at the address specified by the data pointer and subaddress counter. Both the data pointer and subaddress counter are automatically incremented, enabling a stream of data to be transferred either to, or from, the intended devices.

In multiple device applications, the hardware subaddress pins of the PCF8579s (A0, A1, A2 and A3) are connected to V_{SS} or V_{DD} to represent the desired hardware subaddress code. If two or more devices share the same slave address, then each device **must** be allocated with an unique hardware subaddress.

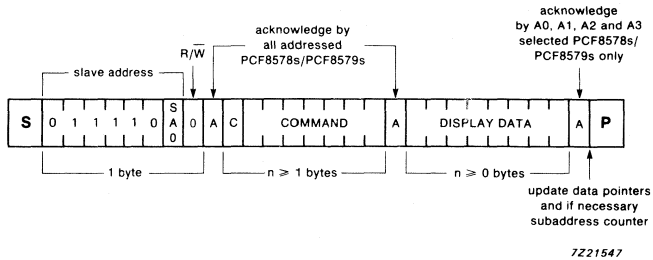


Fig.10(a) Master transmits to slave receiver (WRITE mode).

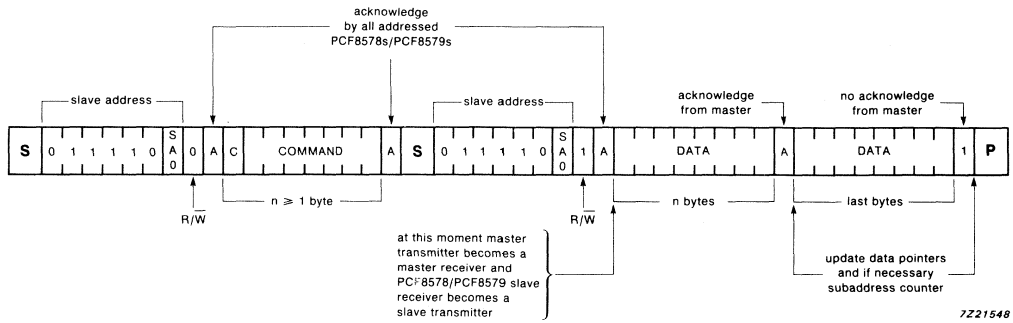


Fig.10(b) Master reads after sending command string (WRITE commands; READ data).

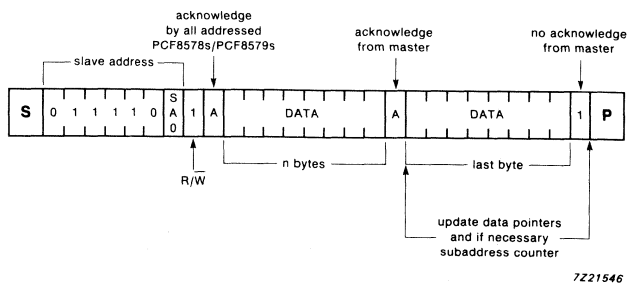
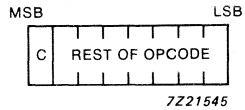


Fig.10(c) Master reads-slave immediately after sending slave address (READ mode).

Command decoder

The command decoder indentifies command bytes that arrive on the I²C-bus. The most-significant bit of a command is the continuation bit C (see Fig.11). When this bit is set, it indicates that the next byte to be transferred will be a command. If the bit is reset, it indicates the conclusion of the command transfer. Further bytes will be regarded as display data. Commands are transferred in WRITE mode only.



C = 0; last command
C = 1; commands continue

Fig.11 General format of command byte.

The five commands available to the PCF8579 are defined in Table 2.

Table 2 Summary of commands

code	command	description
C 0 D D D D D D	LOAD X-ADDRESS	0 to 39
C 1 0 D D D D D	SET MODE	multiplex rate, display status, system type
C 1 1 0 D D D D	DEVICE SELECT	defines device subaddress
C 1 1 1 D D D D	RAM ACCESS	graphic modes, bank select (D D D D ⩾ 12 is not allowed; see SET START BANK opcode)
C 1 1 1 1 1 D D	SET START BANK	defines bank at top of LCD

Where:

C = command continuation bit
D = may be a logic 1 or 0.

Table 3 Definition of PCF8578/PCF8579 commands

command / opcode	options	description
SET MODE C 1 0 T E1 E0 M1 M0	LCD drive mode bits M1 M0 1:8 MUX (8 rows) 0 1 1:16 MUX (16 rows) 1 0 1:24 MUX (24 rows) 1 1 1:32 MUX (32 rows) 0 0	defines LCD drive mode
	display status bits E1 E0 blank 0 0 normal 0 1 all segments on 1 0 inverse video 1 1	defines display status
	system type bit T PCF8578 row only 0 PCF8578 mixed mode 1	defines system type
SET START BANK C 1 1 1 1 1 B1 B0	start bank pointer bits B1 B0 bank 0 0 0 bank 1 0 1 bank 2 1 0 bank 3 1 1	defines pointer to RAM bank corresponding to the top of the LCD. Useful for scrolling, pseudo-motion and background preparation of new display
DEVICE SELECT C 1 1 0 A3 A2 A1 A0	bits A3 A2 A1 A0 4-bit binary value of 0 to 15	four bits of immediate data, bits A0 to A3, are transferred to the subaddress counter to define one of sixteen hardware subaddresses

Table 3 (continued)

command / opcode	options	description
RAM ACCESS C 1 1 1 G1 G0 Y1 Y0	RAM access mode bits G1 G0 character 0 0 half graphic 0 1 full graphic 1 0 not allowed* 1 1	defines the auto-increment behaviour of the address for RAM access
	bits Y1 Y0 2-bit binary value of 0 to 3	two bits of immediate data, bits Y0 to Y1, are transferred to the Y-address pointer to define one of four banks for RAM access
LOAD X-ADDRESS C 0 X5 X4 X3 X2 X1 X0	bits X5 X4 X3 X2 X1 X0 6-bit binary value of 0 to 39	six bits of immediate data, bits X0 to X5, are transferred to the X-address pointer to define one of forty display RAM columns

* See opcode for SET START BANK.

CHARACTERISTICS OF THE I²C-BUS

The I²C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as a control signal.

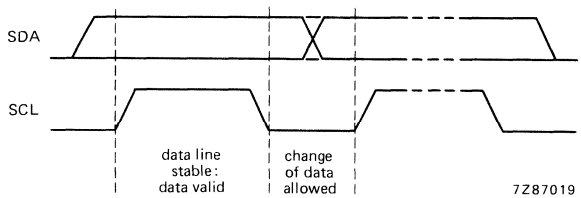


Fig.12 Bit transfer.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH, is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH, is defined as the stop condition (P).

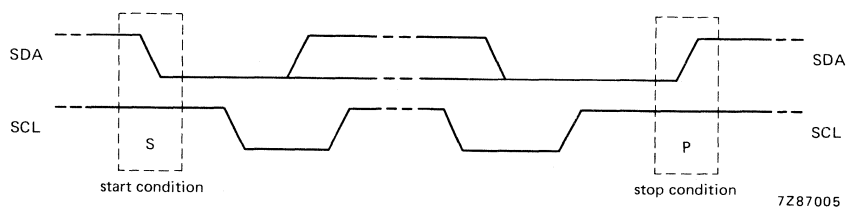


Fig.13 Definition of start and stop condition.

CHARACTERISTICS OF THE I²C-BUS (continued)

System configuration

A device transmitting a message is a "transmitter", a device receiving a message is the "receiver". The device that controls the message flow is the "master" and the devices which are controlled by the master are the "slaves".

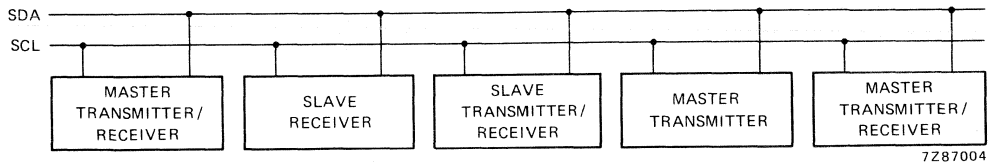


Fig.14 System configuration.

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is unlimited. Each data byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter, whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges must pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal the end of a data transmission to the transmitter by **not** generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

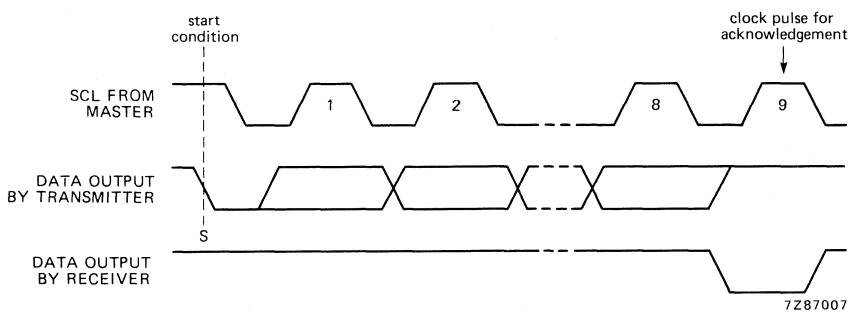


Fig.15 Acknowledgement on the I²C-bus.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage range	V_{DD}	−0.5	+8.0	V
LCD supply voltage range	V_{LCD}	V_{DD} −11	V_{DD}	V
Input voltage range at				
SDA, SCL, $\overline{SYNC}$, CLK, TEST, SA0, A0, A1, A2 and A3	V_{I1}	V_{SS} −0.5	V_{DD} + 0.5	V
V_3 to V_4	V_{I2}	V_{LCD} −0.5	V_{DD} + 0.5	V
Output voltage range at				
SDA	V_{O1}	V_{SS} −0.5	V_{DD} + 0.5	V
C0 to C39	V_{O2}	V_{LCD} −0.5	V_{DD} + 0.5	V
DC input current	I_I	−10	10	mA
DC output current	I_O	−10	10	mA
V_{DD}, V_{SS} or V_{LCD} current	I_{DD}, I_{SS}, I_{LCD}	−50	50	mA
Power dissipation per package	P_{tot}	−	400	mW
Power dissipation per output	P_o	−	100	mW
Storage temperature range	T_{stg}	−65	+ 150	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

DC CHARACTERISTICS

V_{DD} = 2.5 V to 6.0 V; V_{SS} = 0 V; V_{LCD} = V_{DD} −3.5 V to V_{DD} −9 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage		V_{DD}	2.5	–	6.0	V
LCD supply voltage		V_{LCD}	V_{DD} −9	–	V_{DD} −3.5	V
Supply current	note 1; f_{CLK} = 2 kHz	I_{DD1}	–	9	20	μA
Power-on reset level	note 2	V_{POR}	–	1.3	1.8	V
Logic						
Input voltage LOW		V_{IL}	V_{SS}	–	0.3 V_{DD}	V
Input voltage HIGH		V_{IH}	0.7 V_{DD}	–	V_{DD}	V
Leakage current at SDA, SCL, $\overline{SYNC}$, CLK, TEST, SA0, A0, A1, A2 and A3	V_I = V_{DD} or V_{SS}	I_{L1}	−1	–	1	μA
SDA output current LOW	V_{OL} = 0.4 V; V_{DD} = 5 V	I_{OL}	3	–	–	mA
Input capacitance	note 3	C_I	–	–	5	pF
LCD outputs						
Leakage current at V_3 to V_4	V_I = V_{DD} or V_{LCD}	I_{L2}	−2	–	2	μA
DC component of LCD drivers C0 to C39		± V_{DC}	–	20	–	mV
Output resistance at C0 to C39	note 4	R_{COL}	–	3	6	kΩ

AC CHARACTERISTICS (note 5)

V_{DD} = 2.5 to 6 V; V_{SS} = 0 V; V_{LCD} = V_{DD} −3.5 V to V_{DD} −9 V; T_{amb} = −40 to +85 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Clock frequency	50% duty factor	f_{CLK}	–	*	10	kHz
Driver delays	V_{DD} – V_{LCD} = 9 V; with test loads	t_{PLCD}	–	–	100	µs
I²C-bus						
SCL clock frequency		f_{SCL}	–	–	100	kHz
Tolerable spike width on bus		t_{SW}	–	–	100	ns
Bus free time		t_{BUF}	4.7	–	–	µs
Start condition set-up time	repeated start codes only	$t_{SU;STA}$	4.7	–	–	µs
Start condition hold time		$t_{HD;STA}$	4.0	–	–	µs
SCL LOW time		t_{LOW}	4.7	–	–	µs
SCL HIGH time		t_{HIGH}	4.0	–	–	µs
SCL and SDA rise time		t_r	–	–	1.0	µs
SCL and SDA fall time		t_f	–	–	0.3	µs
Data set-up time		$t_{SU;DAT}$	250	–	–	ns
Data hold time		$t_{HD;DAT}$	0	–	–	ns
Stop condition set-up time		$t_{SU;STO}$	4.0	–	–	µs

Notes to the characteristics

1. Outputs are open; inputs at V_{DD} or V_{SS}; I²C-bus inactive; clock with 50% duty cycle.
2. Resets all logic when $V_{DD} < V_{POR}$.
3. Periodically sampled; not 100% tested.
4. Resistance measured between output terminal (C0 to C39) and bias input (V_3 to V_4, V_{DD} and V_{LCD}) when the specified current flows through one output under the following conditions (see Table 1):

   $V_{OP} = V_{DD} - V_{LCD} = 9$ V;

   $V_3 - V_{LCD} \geqslant 4.70$ V; $V_4 - V_{LCD} \leqslant 4.30$ V; $I_{LOAD} = 100$ µA.
5. All timing values are referred to V_{IH} and V_{IL} levels with an input voltage swing of V_{SS} to V_{DD}.

* Typically 0.9 to 3.3 kHz.

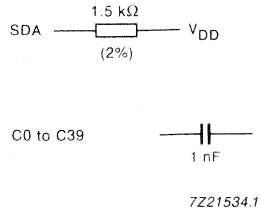


Fig.16 Test loads.

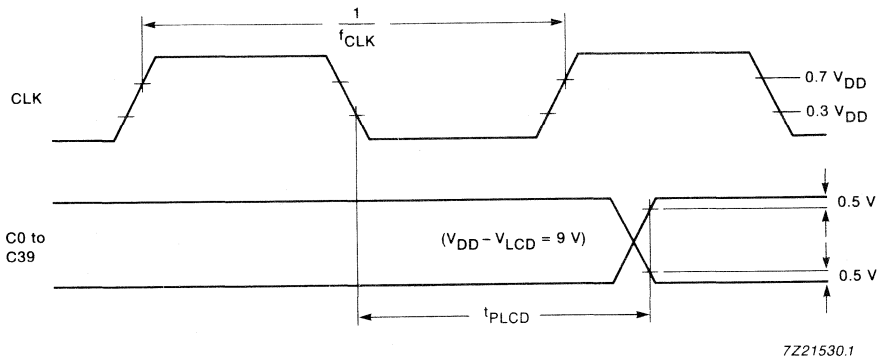


Fig.17 Driver timing waveforms.

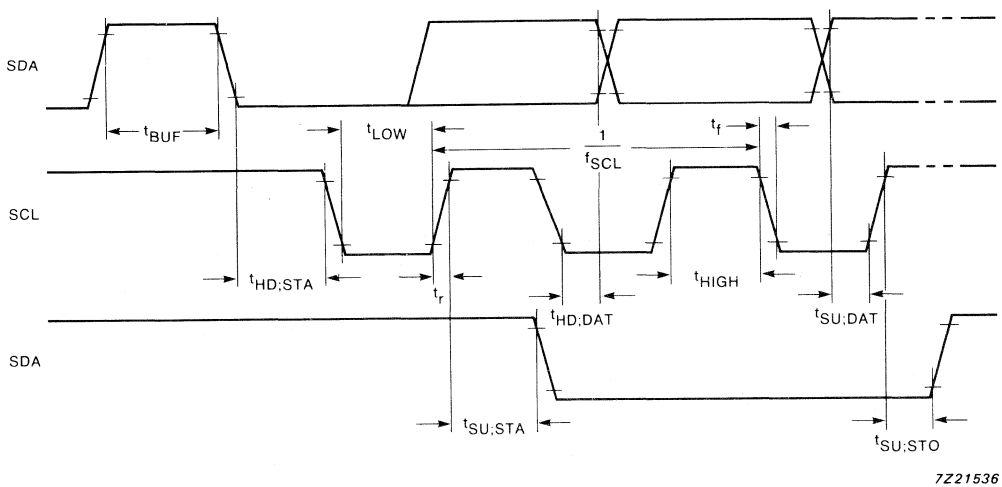


Fig.18 I²C-bus timing waveforms.

LCD column driver for dot matrix graphic displays

PCF8579

APPLICATION INFORMATION

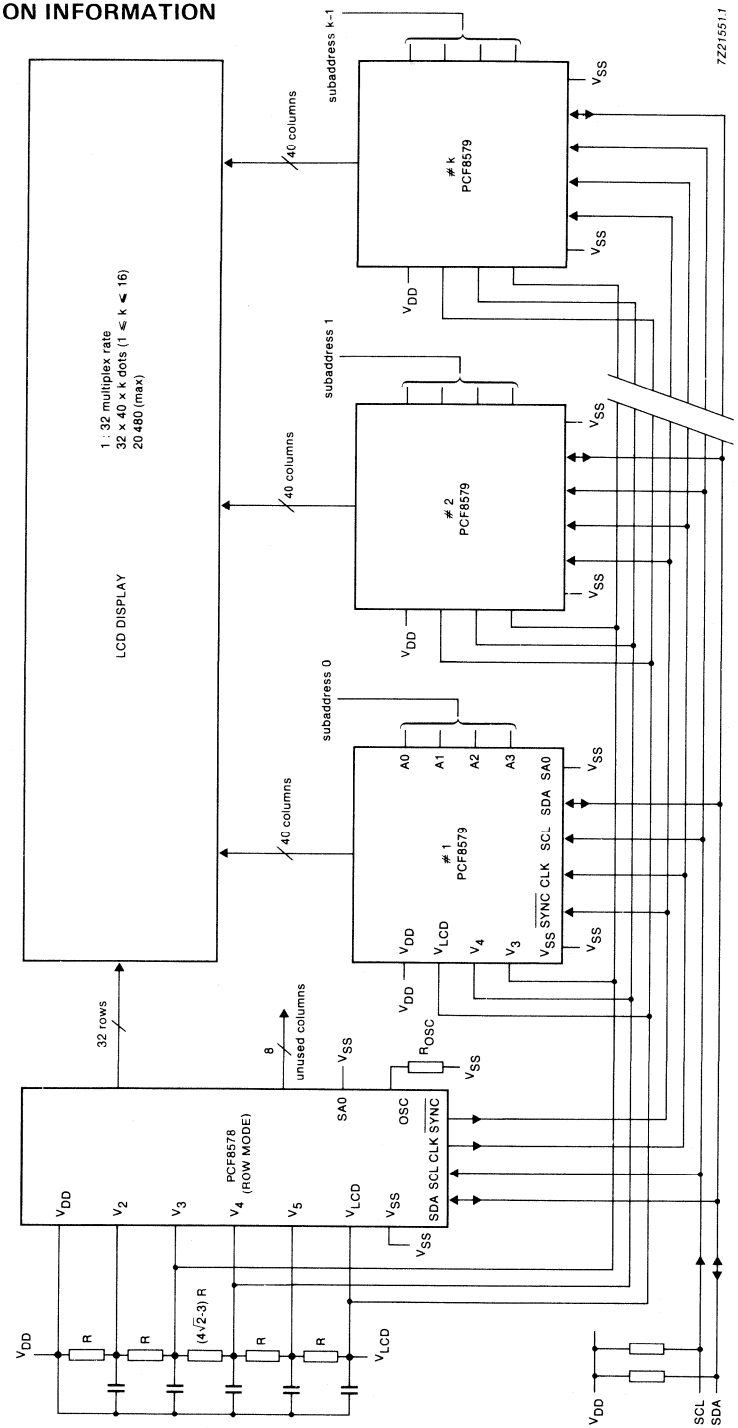


Fig.19 Typical LCD driver system with 1:32 multiplex rate.

LCD column driver for dot matrix graphic displays

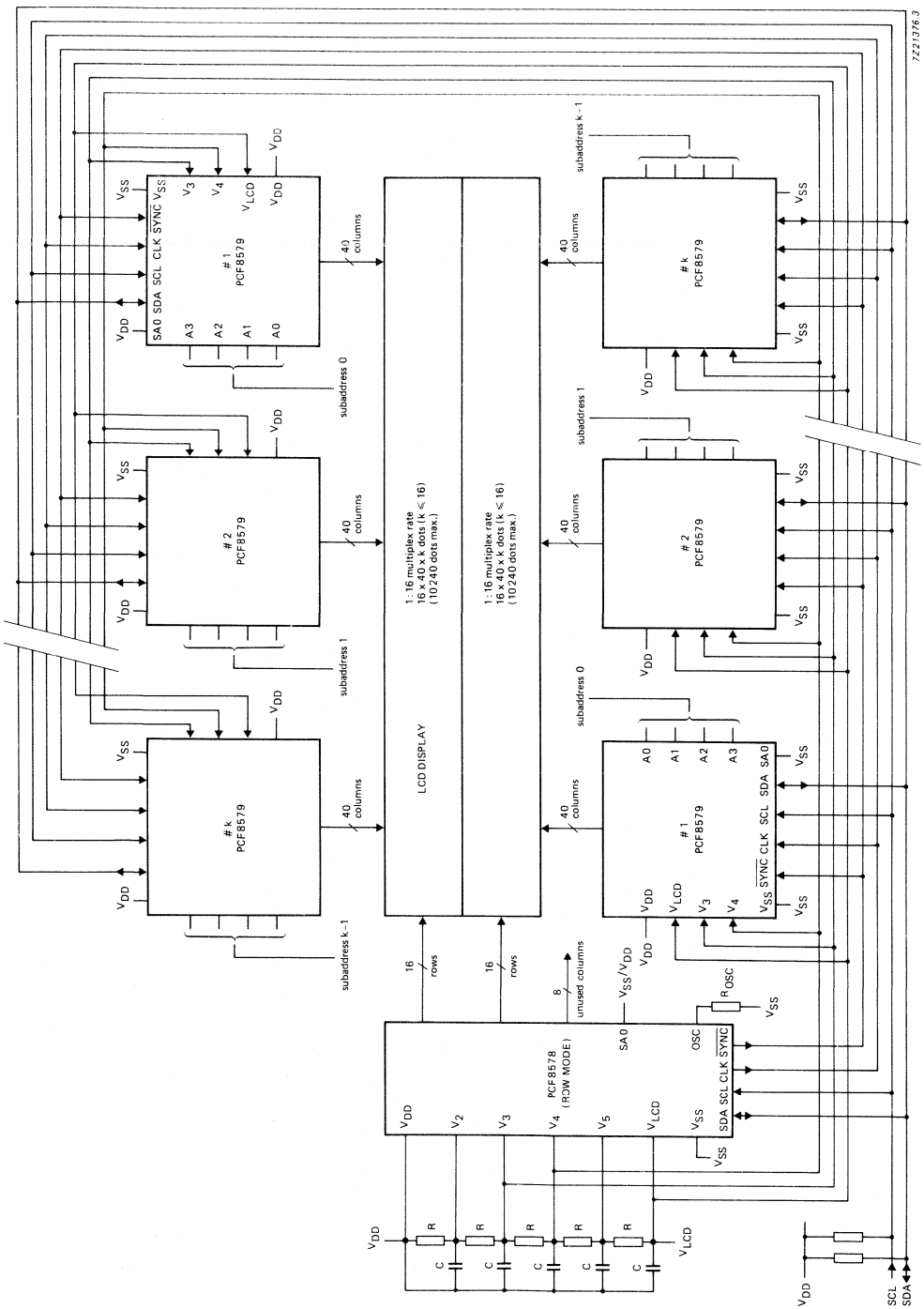


Fig.20 Split screen application with 1:16 multiplex rate for improved contrast.

LCD column driver for dot matrix graphic displays

PCF8579

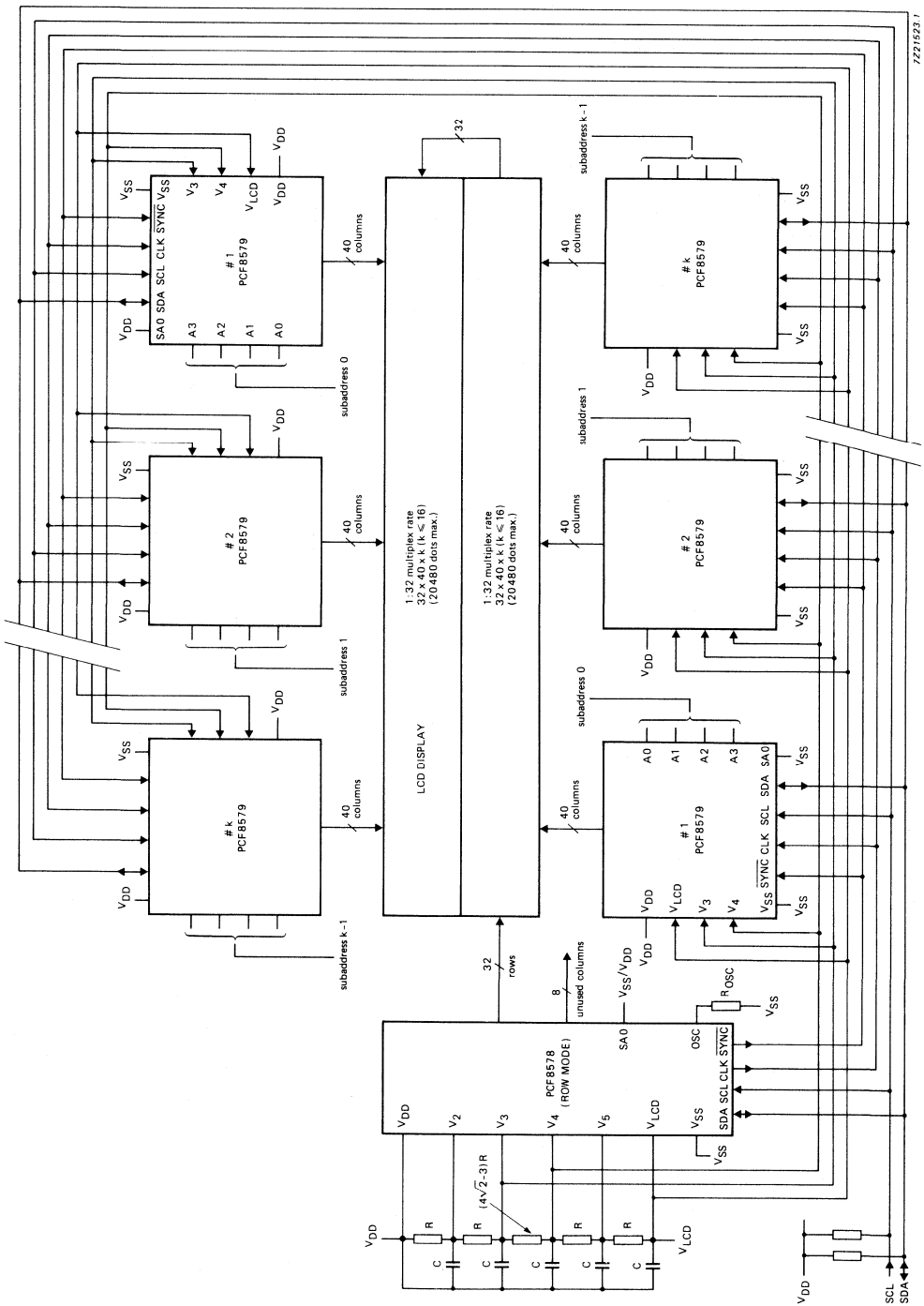


Fig.21 Split screen application using double screen with 1:32 multiplex rate.

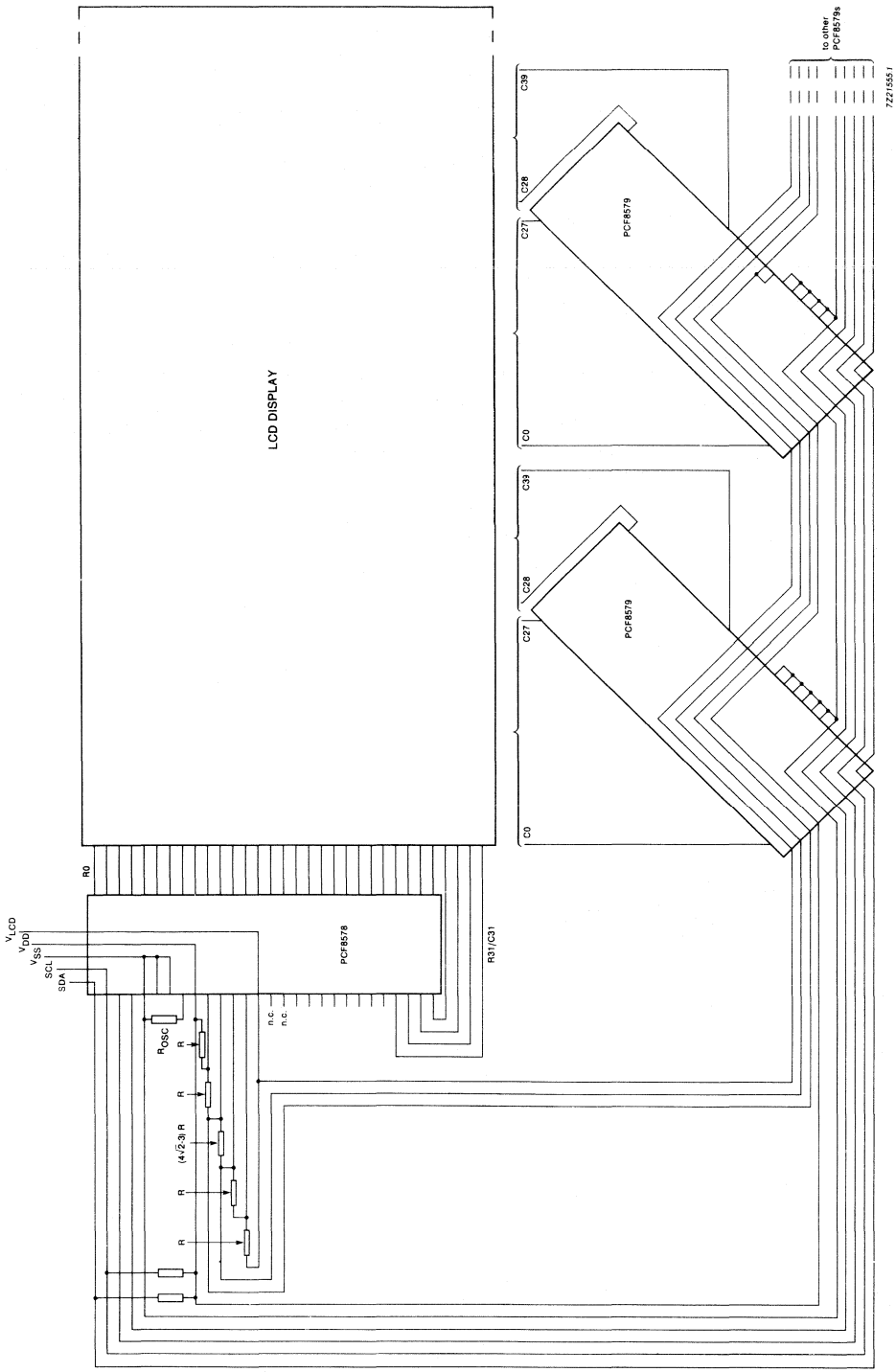


Fig.22 Example of single plane wiring, single screen with 1:32 multiplex rate (PCF8578 in row driver mode).

128 × 8-bit EEPROM with I²C-bus interface PCF8581/PCF8581C

GENERAL DESCRIPTION

The PCF8581 and PCF8581C are low-power CMOS EEPROMs with standard and wide operating voltage:
4.5 to 5.5 V (PCF8581); 2.5 to 6.0 V (PCF8581C).

In the following text, the generic term "PCF8581" is used to refer to both types in all packages except where specified.

The PCF8581 is organized as 128 words by 8-bits.

Addresses and data are transferred serially via a two-line bidirectional bus (I²C). The built-in word address register is incremented automatically after each written or read data byte. All bytes can be read in a single operation. Up to eight bytes can be written in one operation, reducing the total write time per byte. Three address pins A0, A1 and A2 are used to define the hardware address, allowing the use of up to eight devices connected to the bus without additional hardware.

Features

- Operating supply voltage: 4.5 to 5.5 V (PCF8581); 2.5 to 6.0 V (PCF8581C)
- Integrated voltage multiplier and timer for writing (no external components required)
- Automatic erase before write
- Low standby current max. 10 μA
- Eight-byte page write mode
- Serial input/output bus (I²C)
- Address by 3 hardware address pins
- Automatic word address incrementing
- Designed for 10 000 write cycles per byte minimum
- 10 years minimum non-volatile data retention
- Infinite number of read cycles
- Pin and address compatibility to PCF8570, PCF8571 and PCF8582

PACKAGE OUTLINES

PCF8581P/PCF8581CP: 8-lead DIL; plastic (SOT97).
PCF8581T/PCF8581CT: 8-lead mini-pack (SO-8L; SOT176C).

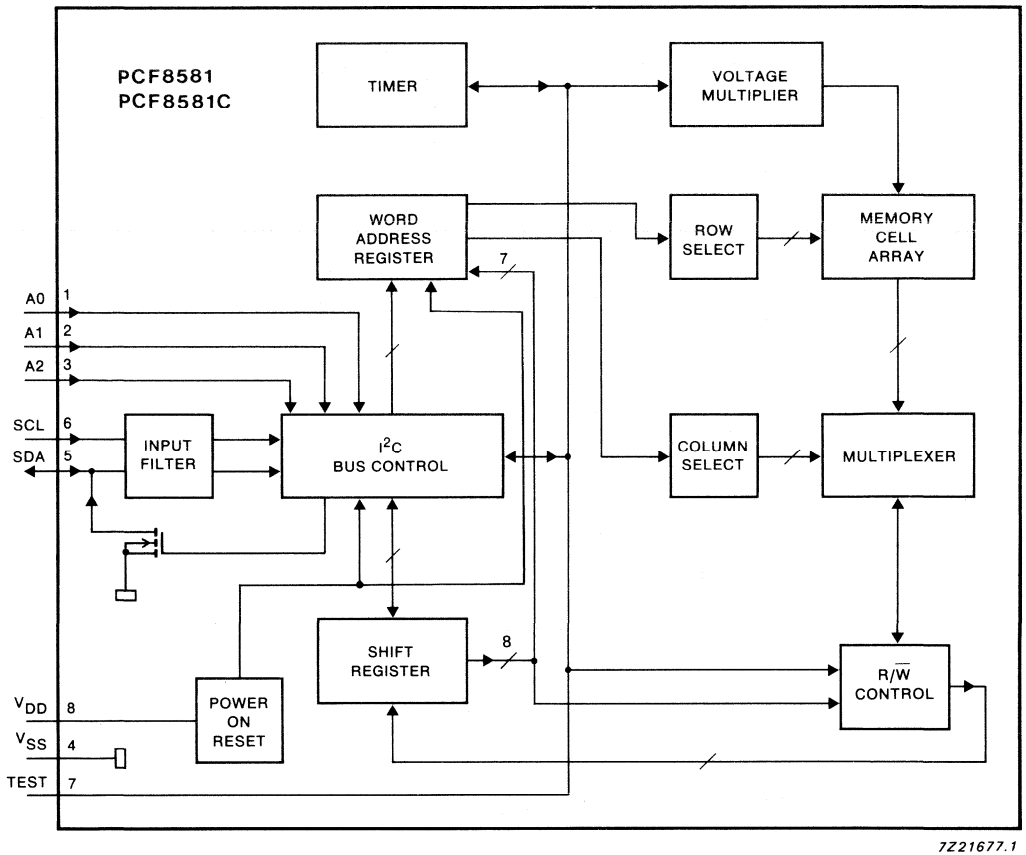


Fig.1 Block diagram.

PINNING

1	A0	hardware address inputs
2	A1	
3	A2	
4	V_{SS}	negative supply
5	SDA	serial data input/output (I²C-bus)
6	SCL	serial clock input (I²C-bus)
7	TEST	test output can be connected to V_{SS}, V_{DD} or left open-circuit
8	V_{DD}	positive supply

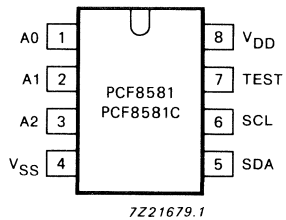


Fig.2 Pinning diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

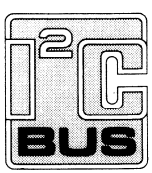
parameter	symbol	min.	max.	unit
Supply voltage range (pin 8)	V_{DD}	−0.3	7.0	V
Voltage range on any input*	V_I	−0.8	V_{DD} + 0.8	V
DC input current (any input)	$\pm I_I$	–	10	mA
DC output current (any output)	$\pm I_O$	–	10	mA
Total power dissipation	P_{tot}	–	150	mW
Power dissipation per output	P	–	50	mW
Storage temperature range	T_{stg}	−65	+ 150	°C
Operating ambient temperature range	T_{amb}	−40	+ 85	°C

* Measured via a 500 Ω resistor.

CHARACTERISTICS

V_{DD} = 2.5 to 6 V (PCF8581C) 4.5 to 5.5 V (PCF8581); V_{SS} = 0 V; T_{amb} = −40 to + 85 °C unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage range						
PCF8581A		V_{DD}	2.5	–	6.0	V
PCF8581		V_{DD}	4.5	–	5.5	V
Supply current						
standby	f_{SCL} = 0 Hz	I_{DD}	–	–	10	μA
operating	f_{SCL} = 100 kHz	I_{DD}	–	–	400	μA
during write	see bus protocol	I_{DD}	–	–	1000	μA
Inputs						
A0, A1, A2, SCL, SDA						
Input voltage LOW		V_{IL}	–	–	$0.3V_{DD}$	V
Input voltage HIGH		V_{IH}	$0.7V_{DD}$	–	–	V
Input leakage current	pin at V_{SS} or V_{DD}	I_{LI}	–	–	1	μA
Input capacitance	pin at V_{SS}	C_I	–	–	7	pF
Outputs						
SDA						
Output current LOW	pin at 0.4 V	I_{OL}	3	–	–	mA
TEST						
Output leakage current	pin at V_{SS} or V_{DD}	I_{LO}	–	–	1	μA
Erase/write data						
Write time		t_{WR}	6	–	12	ms
Data retention time		t_{RET}	10	–	–	years



Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

CHARACTERISTICS OF THE I²C-BUS

The I²C-bus is for two-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

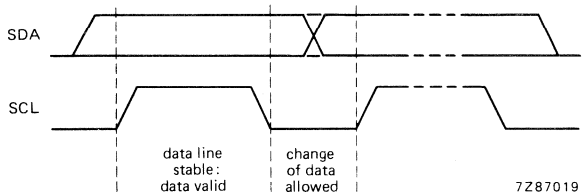


Fig. 3 Bit transfer.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

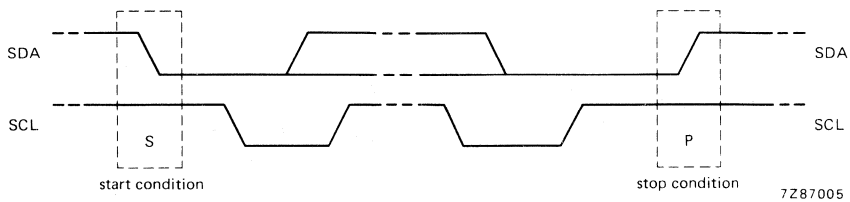


Fig. 4 Definition of start and stop conditions.

System configuration

A device generating a message is a "transmitter", a device receiving a message is the "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

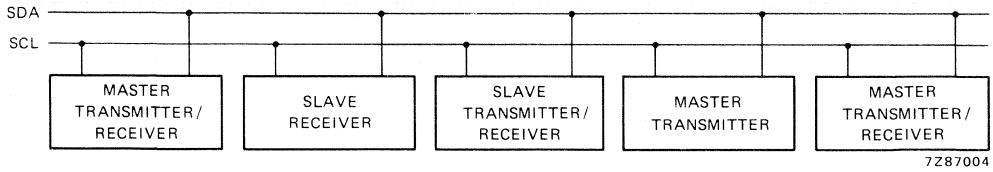


Fig. 5 System configuration.

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte of eigth bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set-up and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by **not** generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

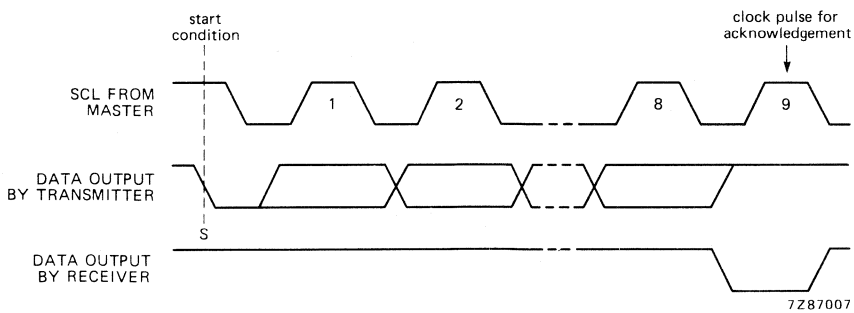


Fig. 6 Acknowledgement on the I²C-bus.

Timing specifications

All the timing values are valid within the operating supply voltage and ambient temperature range and refer to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.

parameter	symbol	min.	typ.	max.	unit
SCL clock frequency	f_{SCL}	–	–	100	kHz
Tolerable spike width on bus	t_{SW}	–	–	100	ns
Bus free time	t_{BUF}	4.7	–	–	μs
Start condition set-up time	$t_{SU;STA}$	4.7	–	–	μs
Start condition hold time	$t_{HD;STA}$	4.0	–	–	μs
SCL LOW time	t_{LOW}	4.7	–	–	μs
SCL HIGH time	t_{HIGH}	4.0	–	–	μs
SCL and SDA rise time	t_r	–	–	1.0	μs
SCL and SDA fall time	t_f	–	–	0.3	μs
Data set-up time	$t_{SU;DAT}$	250	–	–	ns
Data hold time	$t_{HD;DAT}$	0	–	–	ns
SCL LOW to data out valid	$t_{VD;DAT}$	–	–	3.4	μs
Stop condition set-up time	$t_{SU;STO}$	4.0	–	–	μs

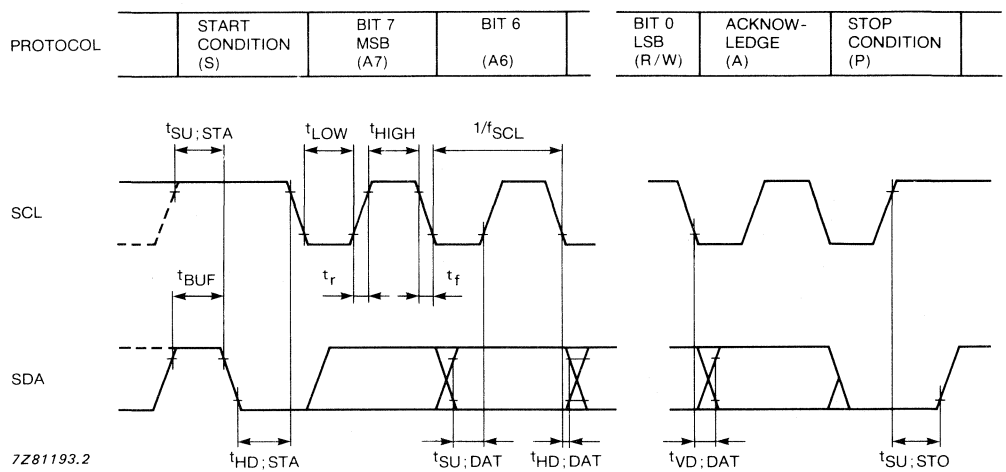


Fig. 7 I²C-bus timing diagram.

Bus protocol

Before any data is transmitted on the I²C-bus, the device which should respond is addressed first. The addressing is always done with the first byte transmitted after the start procedure. The I²C-bus configuration for PCF8581 WRITE cycle is shown in Fig. 8 and READ cycle in Figs 10 and 11.

Writing

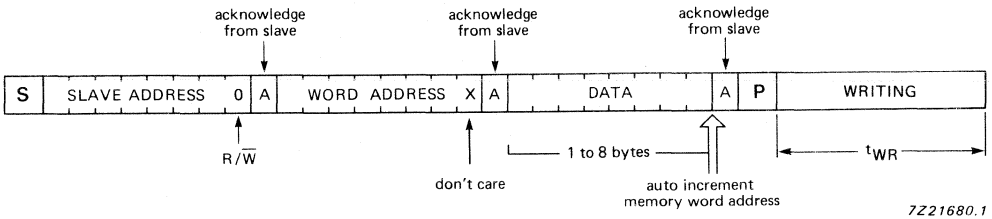


Fig. 8 Master transmits to slave receiver (WRITE mode).

After the word address, one to eight data bytes can be sent. The address is automatically incremented, but the four highest address bits (row) are internally latched. Therefore all bytes are written in the same row.

An example of writing eight bytes with word address X0000000 and six bytes with word address X0010101 is shown in Fig. 9. Where X = don't care.

word address	row	bytes							
X0000000	0	1 →	2 →	3 →	4 →	5 →	6 →	7 →	8 →
X0000001	1								
X0010101	2	4 →	5 →	6			1 →	2 →	3 → →
X0011101	3								
	•								
	•								
column		0	1	2	3	4	5	6	7

Fig. 9 Writing eight and six bytes with different word addresses.

To transmit eight bytes in sequential order, begin with the lowest address bits 000. The data is written after a stop is detected. The data is only written if complete bytes have been received and acknowledged. Writing takes a time t_{WR} (6 to 12 ms) during which the device will not respond to its slave address. Note that to write the next row, a new write operation is required (start, slave address, row address, data, stop).

Reading

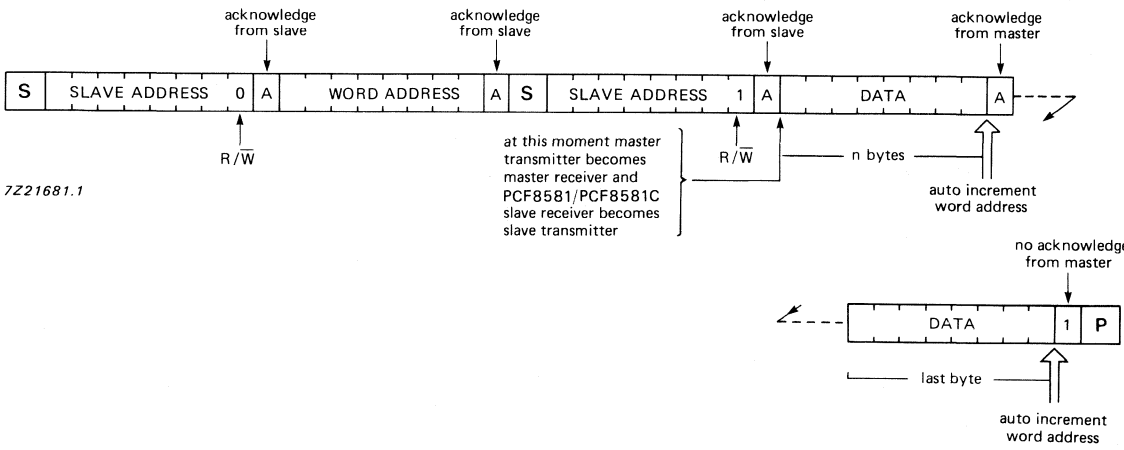


Fig. 10 Master reads after setting word address (WRITE word address; READ data).

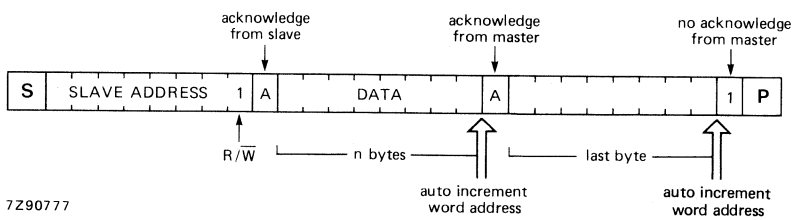


Fig. 11 Master reads slave immediately after first byte (READ mode).

An unlimited number of data bytes can be read in one operation. The address is automatically incremented. If a read without setting the word address is performed after a write operation, the address pointer may point at a byte in the row after the previously written row. This occurs if, during writing, the three lowest address bits (column) rolled over.

APPLICATION INFORMATION

The PCF8581 slave address has a fixed combination 1010 as group 1, while group 2 is fully programmable (see Fig. 12).

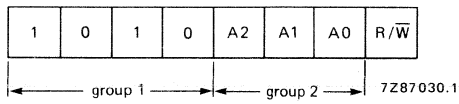


Fig. 12 PCF8581 address.

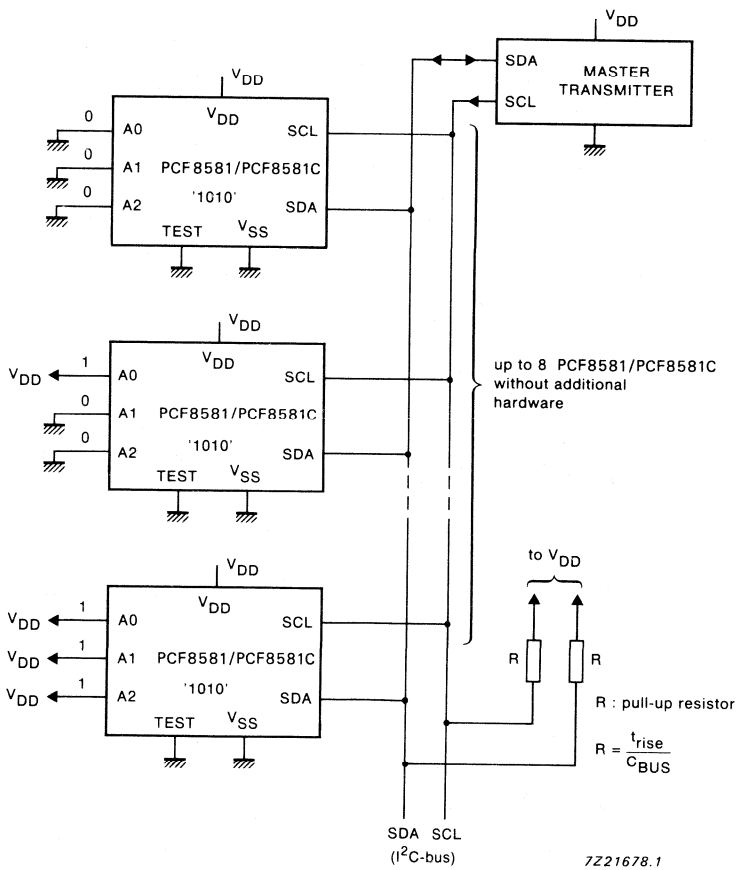


Fig. 13 Application diagram.

Note

A0, A1 and A2 inputs must be connected to V_{DD} or V_{SS} but not left open-circuit.

256 × 8-bit CMOS EEPROMs with I²C-bus interface

PC.8582 Family

GENERAL DESCRIPTION

The 2 Kbit (256 x 8-bit) CMOS EEPROMS are floating gate electrically erasable programmable read only memories.

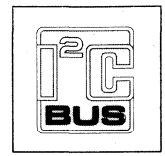
Power consumption is low due to the full CMOS technology used. The programming voltage is generated on-chip using a voltage multiplier.

As data bytes are received and transmitted via the serial I²C-bus, a package using eight pins is sufficient.

Chip select is accomplished by the three address inputs, which also allows up to eight devices to be connected to the I²C-bus.

Features

- Non-volatile storage of 2 Kbits organized as 256 x 8-bits
- Only one power supply required
- On chip voltage multiplier
- Serial input/output bus (I²C)
- Automatic word address incrementing
- Low power consumption
- Power-on reset
- 10 years non-volatile data retention time
- Pin and address compatible to PCF8570, PCF8571, and PCF8581
- Mini-pack package for SMD technology.



QUICK SELECTION GUIDE

TYPE	PCF8582A	PCA8582B	PCF8582C	PCD8582D	PCF8582E
extended temperature range	•	•	•	–	•
extended voltage supply range	–	–	•	•	–
no external RC required	–	–	•	•	•
single bit error correction for extended number of erase/write cycles	–	•	•	•	•

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
PCA8582BP	8	DIL	plastic	SOT97
PCA8582BT	16	SO16L	plastic	SOT162A
PCD8582DP	8	DIL	plastic	SOT97
PCD8582DT	8	SO8	plastic	SOT96A
PCF8582AP	8	DIL	plastic	SOT97
PCF8582AT	16	SO16L	plastic	SOT162A
PCF8582CP	8	DIL	plastic	SOT97
PCF8582CT	16	SO16L	plastic	SOT162A
PCF8582EP	8	DIL	plastic	SOT97
PCF8582ET	8	SO8	plastic	SOT96A

256 × 8-bit CMOS EEPROMs with I²C-bus interface

PC.8582 Family

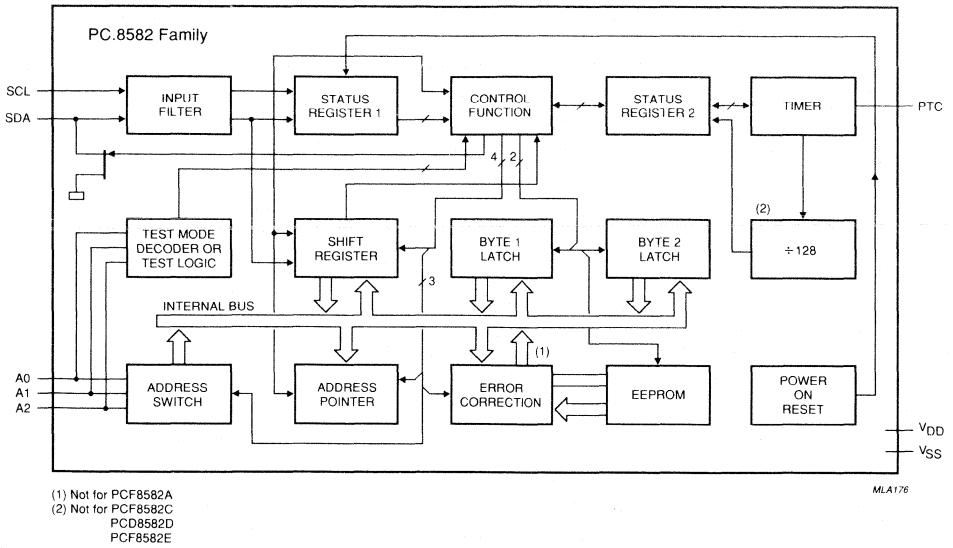


Fig.1 Block diagram.

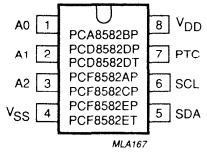


Fig.2 Pin configuration (SOT96A and SOT97).

PINNING

SYMBOL	PIN	DESCRIPTION
A0	1	address input
A1	2	address input
A2	3	address input
V_{SS}	4	ground
SDA	5	serial data
SCL	6	serial clock
PTC	7	can be connected to V_{DD} or left open-circuit
V_{DD}	8	positive supply voltage

FUNCTIONAL DESCRIPTION

Characteristics of the I²C-bus

The I²C-bus is a bidirectional, 2-line communication between different ICs or modules. The two lines are for serial data (SDA) and serial clock (SCL). Both the SDA and the SCL lines must be connected to a positive supply voltage via a pull-up resistor.

The following protocol has been defined:

- data transfer may be initiated only when the bus is not busy.
- during data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as control signals.

The following bus conditions have been defined:

Bus not busy: both data and clock lines remain HIGH.
Start data transfer: a change in the state of the data line, from HIGH-to-LOW, while the clock is HIGH defines the start condition.

Stop data transfer: a change in the state of the data line, from LOW-to-HIGH, while the clock is HIGH, defines the stop condition.

Data valid: the state of the data line represents valid data when, after a start condition, the data line is stable for the duration of the HIGH period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a start condition and terminated with a stop condition; the number of the data bytes, transferred between the start and stop conditions is limited to two bytes in the ERASE/WRITE mode and unlimited in the READ mode. The information is transmitted in bytes and each receiver acknowledges with a ninth bit.

256 × 8-bit CMOS EEPROMs with I²C-bus interface

PC.8582 Family

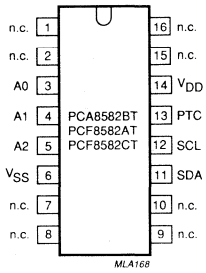


Fig.3 Pin configuration (SOT162A).

PINNING

SYMBOL	PIN	DESCRIPTION
n.c.	1	not connected
n.c.	2	not connected
A0	3	address input
A1	4	address input
A2	5	address input
V_{SS}	6	ground
n.c.	7	not connected
n.c.	8	not connected
n.c.	9	not connected
n.c.	10	not connected
SDA	11	serial data
SCL	12	serial clock
PTC	13	can be connected to V_{DD} or left open-circuit
V_{DD}	14	positive supply voltage
n.c.	15	not connected
n.c.	16	not connected

By definition a device that sends a signal is called a "transmitter" and the device which receives the signal is called a "receiver". The device which controls the signals is called the "master". The devices that are controlled by the master are called "slaves".

Each byte of eight bits is followed by one acknowledge bit. This acknowledge bit is a HIGH level put on the bus by the transmitter. The master generates an extra acknowledge related clock pulse.

The slave receiver which is addressed is obliged to generate an acknowledge after the reception of each byte.

The master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.

The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse.

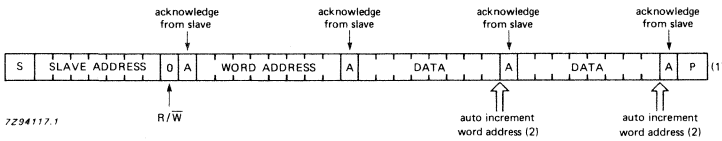
Set up and hold times must be taken into account. A master receiver must signal an end of data to the slave transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master generation of the stop condition.

(1)

(1) Detailed specifications of the I²C-bus are available on request.

I²C-bus protocol

The I²C-bus configuration for different READ and WRITE cycles of the EEPROM are shown in Figures 4, 5 and 6.



(1) After this stop condition the ERASE/WRITE cycle starts and the bus is free for another transmission. During the ERASE/WRITE cycle the slave receiver does not send an acknowledge bit if addressed via the I²C-bus.

(2) The second data byte is voluntary. It is not allowed to ERASE/WRITE more than two bytes.

Fig.4 Master transmitter transmits to EEPROM slave receiver (ERASE/WRITE mode).

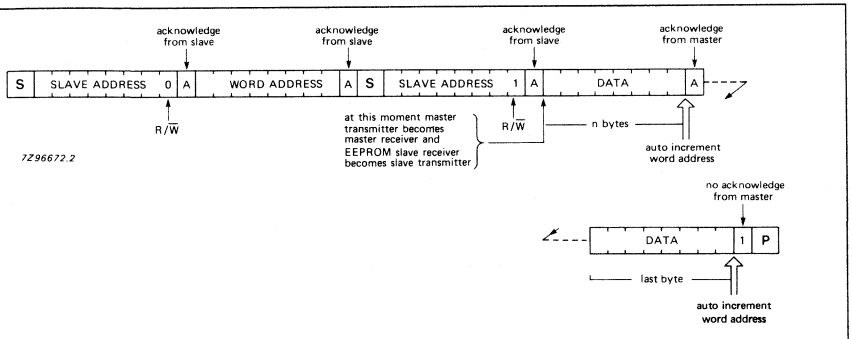


Fig.5 Master reads EEPROM slave after setting word address (write word address; READ data).

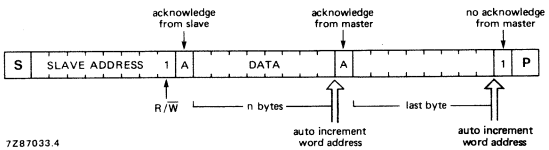


Fig.6 Master reads EEPROM slave immediately after first byte (READ mode). Write protection can be achieved by connecting pin PTC to V_{DD} (for PCF8582A and PCA8582B only).

The slave address is defined in accordance with the I²C-bus specification as:

1	0	1	0	A2	A1	A0	R/W

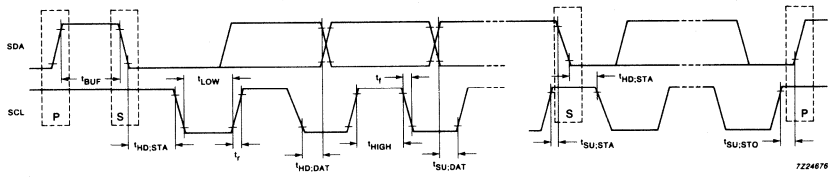


Fig.7 I²C-bus timing.

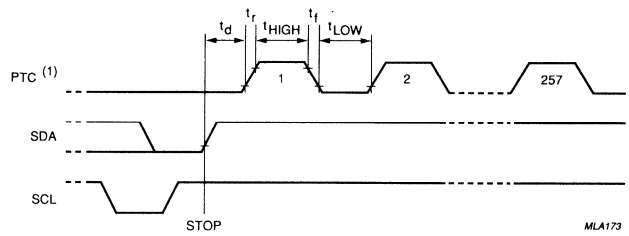


Fig.8 One byte ERASE/WRITE cycle.

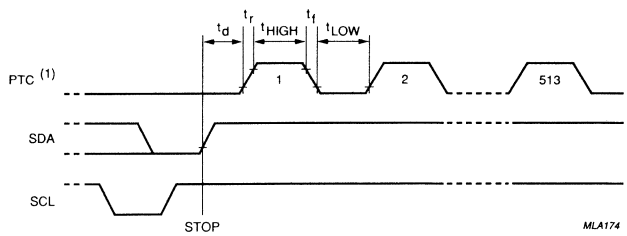
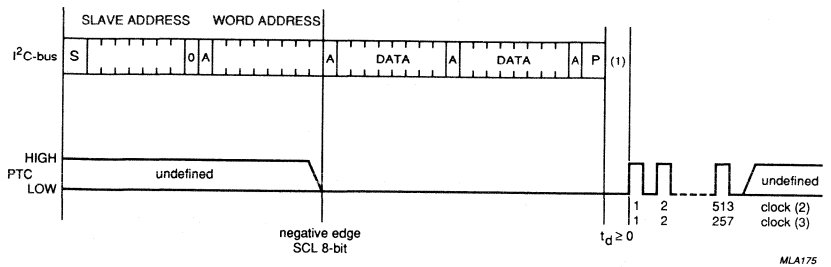


Fig.9 Two byte ERASE/WRITE cycles.



(1) If an external clock is chosen, this information is latched internally by leaving pin PTC LOW after transmission of the eigth bit of the word address (negative edge of SCL). The state of pin 7 then, may be previously undefined.

(2) 2 byte programming

(3) 1 byte programming

Fig.10 External clock.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage		−0.3	+7.0	V
V_I	voltage on any input	$\|Z_I\| > 500\ \Omega$	V_{SS}−0.8	V_{DD} + 0.8	V
I_I	current on any input pin		-	1	mA
I_O	output current		-	10	mA
T_{stg}	storage temperature range		−65	+150	°C
T_{amb}	operating ambient temperature range				
	PCF8582A/C/E		−40	+85	°C
	PCA8582B		−40	+125	°C
	PCD8582D		−25	+70	°C

CHARACTERISTICS

PCF8582A; V_{DD} = 4.5 to 5.5 V; V_{SS} = 0 V; T_{amb} = −40 to +85 °C
PCA8582B; V_{DD} = 4.5 to 5.5 V; V_{SS} = 0 V; T_{amb} = −40 to +125 °C
PCF8582C; V_{DD} = 2.5 to 6 V; V_{SS} = 0 V; T_{amb} = −40 to +85 °C
PCD8582D; V_{DD} = 3 to 6 V; V_{SS} = 0 V; T_{amb} = −25 to +70 °C
PCF8582E; V_{DD} = 4.5 to 5.5 V; V_{SS} = 0 V; T_{amb} = −40 to +85 °C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage					
	PCF8582A/E, PCA8582B		4.5	-	5.5	V
	PCF8582C		2.5	-	6.0	V
	PCD8582D		3	-	6	V
I_{DDR}	supply current READ	f_{SCL} = 100 kHz				
	PCF8582A	$V_{DD(max)}$	–	–	0.4	mA
	PCA8582B	$V_{DD(max)}$	–	–	0.8	mA
	PCF8582C/PCD8582D	V_{DD} = 3 V	–	–	0.25	mA
		V_{DD} = 6 V	–	–	1.6	mA
	PCF8582E	$V_{DD(max)}$	–	–	1.6	mA
$I_{DDE/W}$	supply current ERASE/WRITE	f_{SCL} = 100 kHz				
	PCF8582A/PCA8582B	$V_{DD(max)}$	–	–	2	mA
	PCF8582C/PCD8582D	V_{DD} = 3 V	–	–	0.35	mA
		V_{DD} = 6 V	–	–	2.5	mA
	PCF8582E	$V_{DD(max)}$	–	–	2.5	mA
I_{stb}	supply current STANDBY					
	PCF8582A	$V_{DD(max)}$	–	–	10	µA
	PCA8582B	$V_{DD(max)}$	–	–	20	µA
	PCF8582C/PCD8582D	V_{DD} = 3 V	–	–	3.5	µA
		V_{DD} = 6 V	–	–	10	µA
	PCF8582E	$V_{DD(max)}$	–	–	10	µA
PTC input (PCF8582A/PCA8582B)						
V_{IH}	input voltage HIGH		V_{DD}−0.3	–	V_{DD} + 0.8	V
V_{IL}	input voltage LOW		−0.8	–	V_{SS} + 0.3	V
PTC input (PCF8582C/PCD8582D/PCF8582E)						
V_{IH}	input voltage HIGH		0.9 V_{DD}	–	V_{DD} + 0.8	V
V_{IL}	input voltage LOW		−0.8	–	0.1 V_{DD}	V
SCL input						
V_{IH}	input voltage HIGH					
	PCF8582A/PCA8582B		3	–	V_{DD} + 0.8	V
	PCF8582C/PCD8582D/PCF8582E		0.7 V_{DD}	–	V_{DD} + 0.8	V
SDA input/output						
V_{IL}	input voltage LOW					
	PCF8582A/PCA8582B		−0.3	–	1.5	V
	PCF8582C/PCD8582D/PCF8582E		−0.8 V_{DD}	–	0.3 V_{DD}	V
V_{OL}	output voltage LOW	I_{OL} = 3 mA				
	PCF8582A/PCA8582B	V_{DD} = 4.5 V	–	–	0.4	V
	PCF8582C	V_{DD} = 2.5 V	–	–	0.4	V
	PCD8582D	V_{DD} = 3 V	–	–	0.4	V
	PCF8582E	$V_{DD(min)}$	–	–	0.4	V
I_{LO}	output leakage current	V_{OH} = V_{DD}	–	–	1	µA
I_{LI}	input leakage current	V_I = V_{DD} or V_{SS}	–	–	1	µA
Data retention time						
t_S	data retention time	T_{amb} = 55 °C	10	–	–	yrs

WRITE CYCLE LIMITS

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
t_{EW}	ERASE/WRITE cycle time				
	PCF8582A/PCA8582B		5	40	ms
	PCF8582C/PCD8582D/PCF8582E		5	25	ms
Endurance					
N_{EW}	ERASE/WRITE cycles per byte				
	PCF8582A		–	10000	
	PCA8582B	T_{amb} = 125 °C; t_{EW} = 5 to 40 ms	–	50000	
		T_{amb} = 85 °C; t_{EW} = 5 to 40 ms	–	100000	
		T_{amb} = 33 °C; t_{EW} = 10 ms	-	500000	
	PCF8582C	T_{amb} = 85 °C; t_{EW} = 5 to 25 ms	–	100000	
		T_{amb} = 33 °C; t_{EW} = 10 ms	–	500000	
	PCD8582D	T_{amb} = −25 to +70 °C; t_{EW} = 5 to 25 ms	–	10000	
		T_{amb} = 0 to +40 °C; t_{EW} = 10 ms	–	100000	
	PCF8582E	T_{amb} = −40 to +85 °C; t_{EW} = 5 to 25 ms	–	100000	

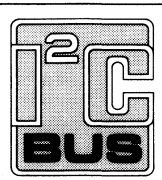
I²C-BUS CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
f_{SCL}	clock frequency		0	-	100	kHz
C_I	input capacitance (SDA; SCL)	$V_I = V_{SS}$	-	-	7	pF
t_{BUF}	time the bus must be free before new transmission can start		4.7	-	-	µs
$t_{HD;STA}$	start condition hold time after which first clock pulse is generated		4	-	-	µs
t_{LOW}	clock period LOW		4.7	-	-	µs
t_{HIGH}	clock period HIGH		4	-	-	µs
$t_{SU;STA}$	set up time for start condition	repeated start	4.7	-	-	µs
$t_{HD;DAT}$	data hold time for bus compatible masters		5	-	-	µs
$t_{HD;DAT}$	data hold time for bus devices	note 1	0	-	-	ns
$t_{SU;DAT}$	data set up time		250	-	-	ns
t_r	SDA and SCL rise time		-	-	1	µs
t_f	SDA and SCL fall time		-	-	300	ns
$t_{SU;STO}$	set up time for stop condition		4.7	-	-	µs

Note

1. The hold time required to bridge the undefined region of the falling edge of SCL must be internally provided by a transmitter. It is not greater than 300 ns.

I²C



Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specification defined by Philips.

E/W programming time control

Using external resistor R_{EW} and capacitor C_{EW} (see Table 1).

Table 1 Recommended R_{EW} and C_{EW} combinations (PCF8582A/PCA8582B only).

R_{EW} (kΩ)	C_{EW} (nF)	T_{EW} (typ.) (ms)
56	3.3	34
56	2.2	21
22	3.3	13
22	2.2	7.5

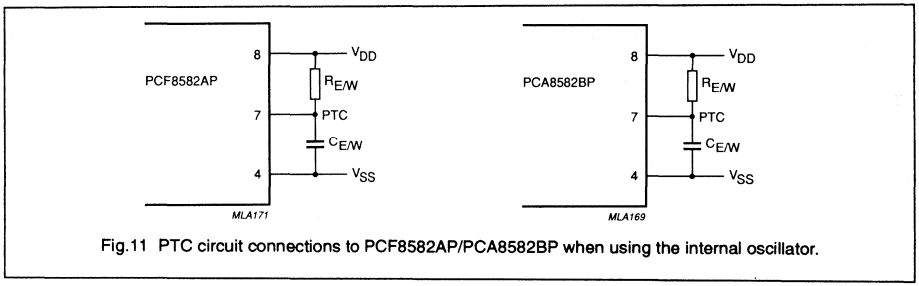


Fig.11 PTC circuit connections to PCF8582AP/PCA8582BP when using the internal oscillator.

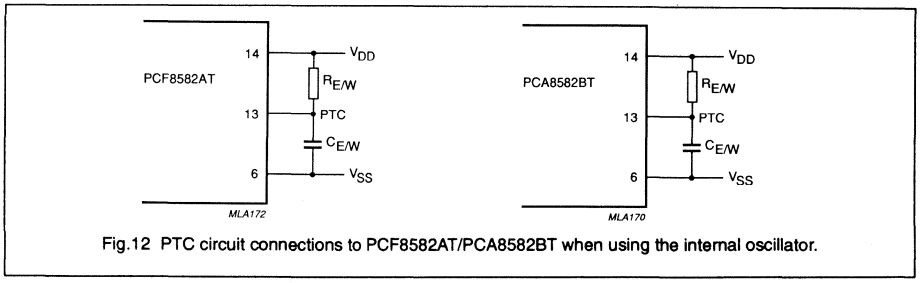


Fig.12 PTC circuit connections to PCF8582AT/PCA8582BT when using the internal oscillator.

Using external clock (see Table 2 and Figs 8, 9 and 10).

Table 2 E/W programming time control using an external clock.

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
f_{CLK}	frequency	10	50	kHz
t_{LOW}	clock period LOW	10	-	µs
t_{HIGH}	clock period HIGH	10	-	µs
t_r	rise time	-	300	ns
t_f	fall time	-	300	ns
t_d	delay time	0	t_{LOW}	µs

USING AN INTERNAL OSCILLATOR

When using an internal oscillator t_{EW} has a minimum value of 5 ms and a maximum value of 25 ms; a typical value is 10 ms.

Clock calendar with 256 × 8-bit static RAM — PCF8583

FEATURES

- I²C-bus interface operating supply voltage: 2.5 V to 6 V
- Clock operating supply voltage (0 to +70 °C): 1.0 V to 6.0 V
- Data retention voltage: 1.0 V to 6 V
- Operating current (f_{scl} = 0 Hz): max. 50 A
- Clock function with four year calendar
- Universal timer with alarm and overflow indication
- 24 or 12 hour format
- 32.768 kHz or 50 Hz time base
- Serial input/output bus (I²C)
- Automatic word address incrementing
- Programmable alarm, timer and interrupt function
- Slave address, READ: A1 or A3, WRITE: A0 or A2.

GENERAL DESCRIPTION

The PCF8583 is a low power 2048-bit static CMOS RAM organized as 256 words by 8 bits. Addresses and data are transferred serially via a two-line bidirectional bus (I²C). The built-in word address register is incremented automatically after each written or read data byte. One address pin A0 is used for programming the hardware address, allowing the connection of two devices to the bus without additional hardware. The built-in 32.768 kHz oscillator circuit and the first 8 bytes of the RAM are used for the clock/calendar and counter functions. The next 8 bytes may be programmed as alarm registers or used as free RAM space.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITION	MIN.	MAX.	UNIT
V_{DD}	supply voltage operating range	I²C-bus active	2.5	6.0	V
V_{DD}	supply voltage operating range	I²C-bus inactive	1.0	6.0	V
I_{DD}	supply current operating mode	f_{scl} =100 kHz	-	200	µA
I_{DDO}	supply current clock mode	f_{scl} = 0 Hz; V_{DD} = 5 V	-	50	µA
		f_{scl} = 0 Hz; V_{DD} = 1 V	-	10	µA
T_{amb}	operating ambient temperature range		–40	+85	°C
T_{stg}	storage temperature range		–65	+150	°C

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
PCF8583P	8	DIL	plastic	SOT97
PCF8583T	8	mini-pack	plastic	SO8L; SOT176C

Clock calendar with 256 × 8-bit static RAM — PCF8583

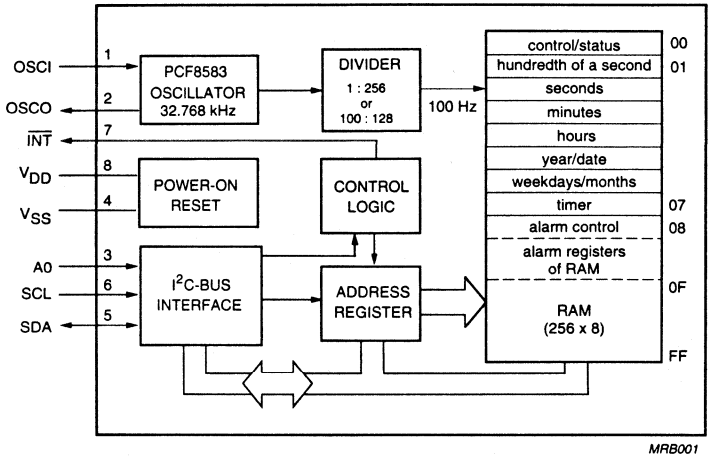


Fig.1 Block diagram.

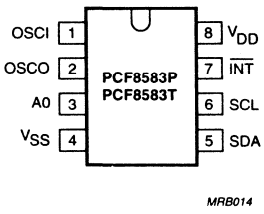


Fig.2 Pinning diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
OSCI	1	oscillator input, 50 Hz or event-pulse input
OSCO	2	oscillator output
A0	3	address input
V_{SS}	4	negative supply
SDA	5	serial data line
SCL	6	serial clock line
$\overline{INT}$	7	open drain interrupt output (active LOW)
V_{DD}	8	positive supply

PURCHASE OF PHILIPS I²C COMPONENTS

Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 358 10011.

FUNCTIONAL DESCRIPTION

The PCF8583 contains a 256 by 8-bit RAM with an 8-bit auto-increment address register, an on-chip 32.768 kHz oscillator circuit, a frequency divider, a serial two-line bidirectional I²C-bus interface and a power-on reset circuit.

The first 8 bytes of the RAM (memory addresses 00 to 07) are designed as addressable 8-bit parallel registers. The first register (memory address 00) is used as a control/status register. The memory addresses 01 to 07 are used as counters for the clock function. The memory addresses 08 to 0F are free RAM locations or may be programmed as alarm registers.

Counter function modes

When the control/status register is programmed, a 32.768 kHz clock mode, a 50 Hz clock mode or an event-counter mode can be selected.

In the clock modes the hundredth of a second, seconds, minutes, hours, date, month (four year calendar) and weekday are stored in a BCD format. The timer register stores up to 99 days. The event counter mode is used to count pulses applied to the oscillator input (OSCO left open). The event counter stores up to 6 digits of data.

When one of the counters is read (memory locations 01 to 07), the contents of all counters are strobed into capture latches at the beginning of a read cycle. Therefore, faulty reading of the count during a carry condition is prevented.

When a counter is written, other counters are not affected.

Alarm function modes

By setting the alarm enable bit of the control/status register the alarm control register (address 08) is activated.

By setting the alarm control register a dated alarm, a daily alarm, a weekday alarm or a timer alarm may be programmed. In the clock modes, the timer register (address 07) may be programmed to count hundredths of a second, seconds, minutes, hours or days. Days are counted when an alarm is not programmed.

Whenever an alarm event occurs the alarm flag of the control/status register is set. A timer alarm event will set the alarm flag and an overflow condition of the timer will set the timer flag. The open drain interrupt output is switched on (active LOW) when the alarm or timer flag is set (enabled). The flags remain set until directly reset by a write operation.

When a timer function without any function is programmed the remaining alarm registers (addresses 09 to 0F) may be used as free RAM space.

Control/status register

The control/status register is defined as the memory location 00 with free access for reading and writing via the I²C-bus. All functions and options are controlled by the contents of the control/status register (see Fig. 3).

Counter registers

In the clock modes 24 h or 12 h format can be selected by setting the most significant bit of the hours counter register. The format of the hours counter is shown in Fig 5.

The year and date are packed into memory location 05 (see Fig 6). The weekdays and months are packed into memory location 06 (see Fig. 7). When reading these memory locations the year and weekdays are masked out when the mask flag of the control/status register is set. This allows the user to read the date and month count directly.

In the event-counter mode events are stored in BCD format. D5 is the most significant and D0 the least significant digit. The divider is by-passed.

In the different modes the counter registers are programmed and arranged as shown in Fig 4. Counter cycles are listed in Table 1.

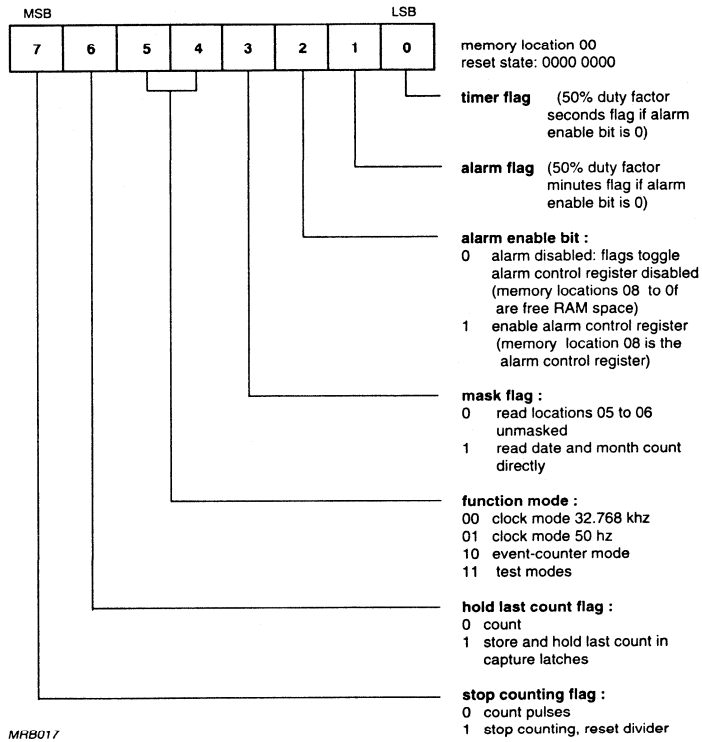


Fig.3 Control/status register.

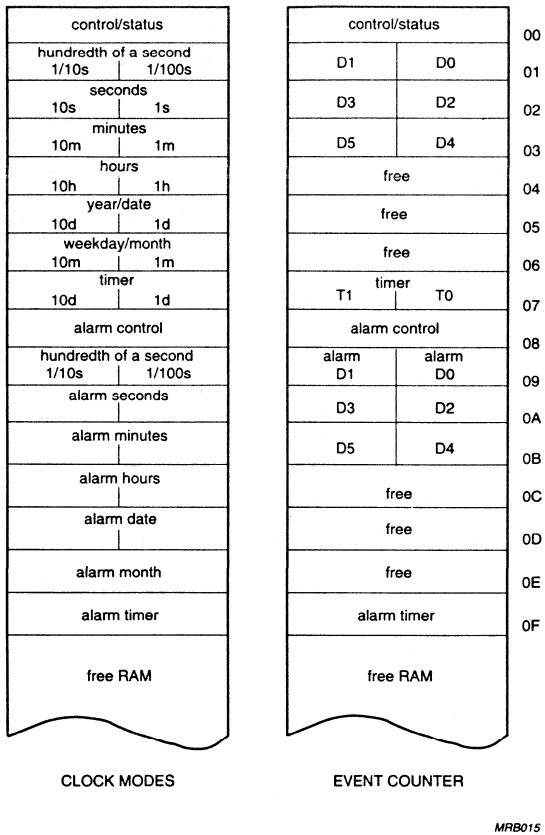


Fig.4 Register arrangement.

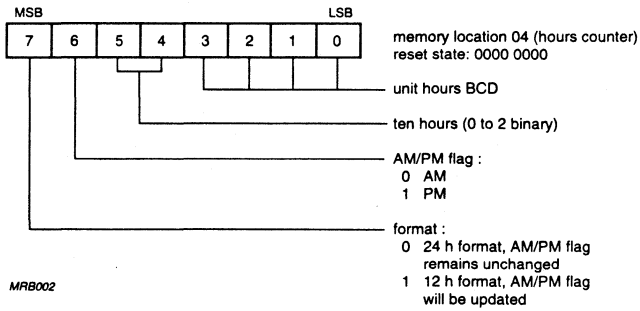


Fig.5 Format of the hours counter.

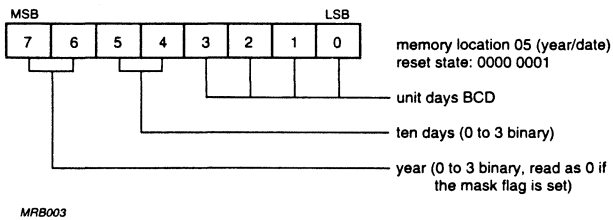


Fig.6 Format of the year/date counter.

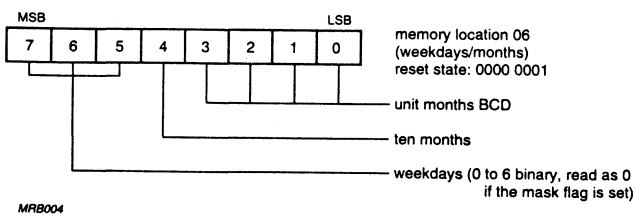


Fig.7 Format of the weekdays/months counter.

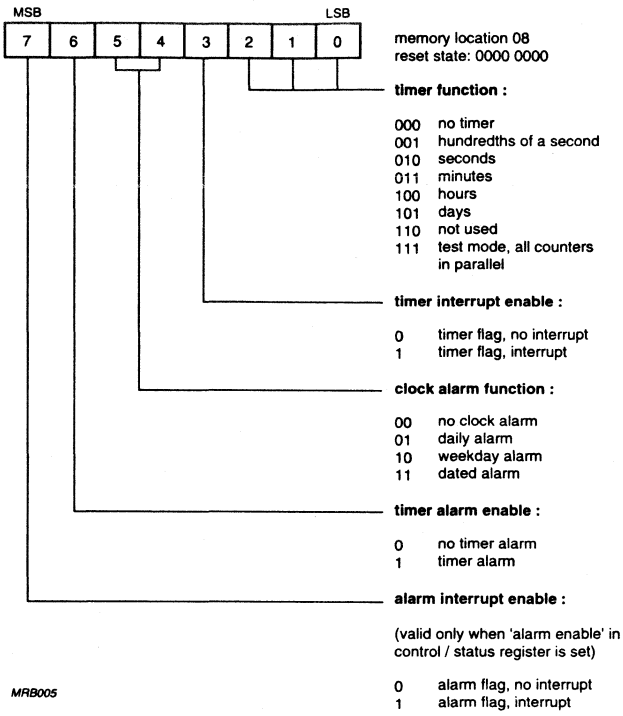


Fig.8 Alarm control register; clock mode.

Alarm Control register

When the alarm enable bit of the control/status register is set (address 00, bit 2) the Alarm Control register (address 08) is activated. All alarm, timer, and interrupt output functions are controlled by the contents of the alarm control register (see Fig 8).

Alarm registers

All alarm registers are allocated with a constant address offset of hex 08 to the corresponding counter registers (see Fig 4, Register arrangement).

An alarm signal is generated when the contents of the alarm registers matches bit-by-bit the contents of the involved counter registers. The year and weekday bits are ignored in a dated alarm. A daily alarm ignores the month and date bits. When a weekday alarm is selected , the contents of the alarm weekday/month register will select the weekdays on which an alarm is activated (see Fig. 9).

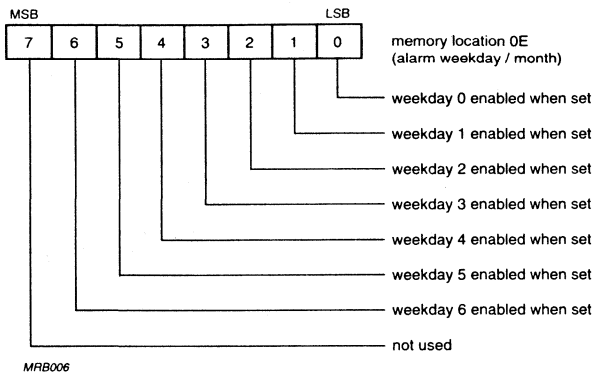


Fig.9 Selection of alarm weekdays.

Note:

In the 12 h mode, bits 6 and 7 of the alarm hours register must be the same as the hours counter.

Timer

The timer (location 07) is enabled by setting the Control/Status register = XX0X X1XX. The timer counts up from 0 (or a programmed value) to 99. On overflow, the timer resets to 0. The Timer flag (LSB of Control/Status register) is set on overflow of the timer. This flag must be reset by software. The inverted value of this flag can be transferred to the external interrupt by setting bit 3 of the Alarm Control register.

Additionally, a timer alarm can be programmed by setting the Timer Alarm enable (bit 6 of the Alarm Control register). When the value of the timer equals a pre-programmed value in the Alarm Timer register (location 0F), the Alarm flag is set (bit 1 of the Control/status register). The inverted value of the alarm flag can be transferred to the external interrupt by enabling the Alarm interrupt (bit 6 of the Alarm Control register).

Resolution of the timer is programmed via the 3 LSBs of the Alarm Control register. See fig 11: Alarm and Timer Interrupt logic diagram.

Event Counter Mode

Event Counter mode is selected by bits 4 and 5 = 10 in the Control/status register. The event counter mode is used to count pulses externally applied to the oscillator input (OSCO left open). The event counter stores up to 6 digits of data, which are stored as 6 hexadecimal values located in locations 1, 2, and 3. Thus, up to 1 million events may be recorded.

An event counter alarm occurs when the event counter registers match the value programmed in locations 9, A, and B, and the event alarm is enabled (bits 4 and 5 = 01 in the Alarm Control register). In this case, the Alarm flag (bit 1 of the Control/status register) is set. The inverted value of this flag can be transferred to the interrupt pin (pin 7) by setting the Alarm interrupt enable in the Alarm Control register. In this mode, the timer (location 07) increments once for every one, one-hundred, ten thousand, or 1 million events, depending on the value programmed in bits 0 1 2 of the Alarm Control register. In all other respects, the timer functions as in the clock mode.

Interrupt output

The conditions for activating the open-drain n-channel interrupt output (active LOW) are determined by appropriate programming of the Alarm Control register. These conditions are: Clock alarm, timer alarm, timer overflow, and event counter alarm. An interrupt occurs when the alarm flag or the timer flag is set, and the corresponding interrupt is enabled. In all cases, the interrupt is cleared only by software resetting of the flag which initiated the interrupt.

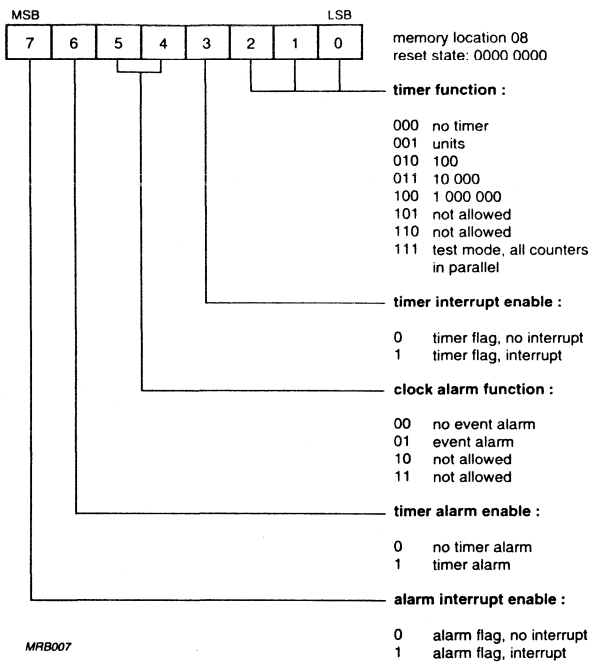


Fig.10 Alarm control register, event-counter mode.

In the clock mode, if the Alarm enable is not activated (Alarm Enable bit of Control/status register = 0), the interrupt output toggles with at 1 Hz with a 50% duty cycle. This is the default power-on state of the device. The OFF voltage of the interrupt output may exceed the supply voltage, up to a maximum of 6.0 V. A logic diagram of the interrupt output is shown in Fig 11.

Oscillator and divider

A 32.768 kHz quartz crystal has to be connected to OSCI (pin 1) and OSCO (pin 2). A trimmer capacitor between OSCI and V_{DD} is used for tuning the oscillator (see quartz frequency adjustment). A 100 Hz clock signal is derived from the quartz oscillator for the clock counters.

In the 50 Hz clock mode or event-counter mode the oscillator is disabled and the oscillator input is switched to a high impedance state. This allows the user to feed the 50 Hz reference frequency or an external high speed event signal into the input OSCI.

Initialization

When power-up occurs the I²C-bus interface, the control/status register and all clock counters are reset. The device starts time-keeping in the 32.768 kHz clock mode with the 24 h format on the first of January at 0.00.00: 00. A 1 Hz square wave with 50% duty cycle appears at the interrupt output pin (starts HIGH).

It is recommended to set the stop counting flag of the control/status register before loading the actual time into the counters. Loading of illegal states may lead to a temporary clock malfunction.

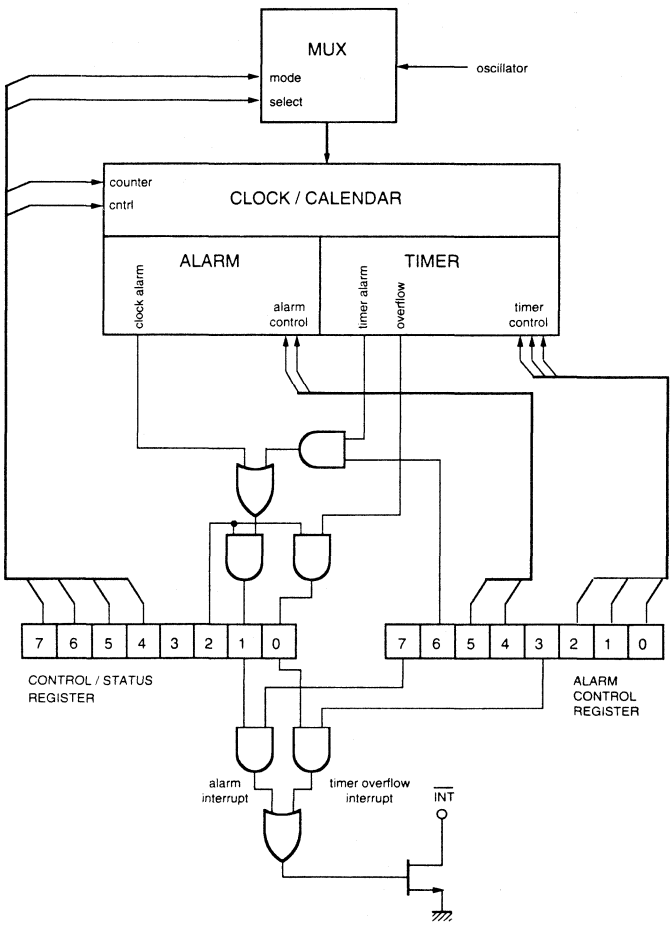


Fig.11 Alarm and Timer Interrupt logic diagram.

CHARACTERISTICS OF THE I²C-BUS

The I²C-bus is for bi-directional, two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as a control signal.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

System configuration

A device generating a message is a "transmitter", a device receiving a message is the "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is unlimited. Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH level signal put on the bus by the transmitter during which time the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges must pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

I²C-bus protocol

Before any data is transmitted on the I²C-bus, the device which should respond is addressed first. The addressing is always done with the first byte transmitted after the start procedure. The I²C-bus configuration for the different PCF8583 READ and WRITE cycles is shown in Figs. 16, 17 and 18.

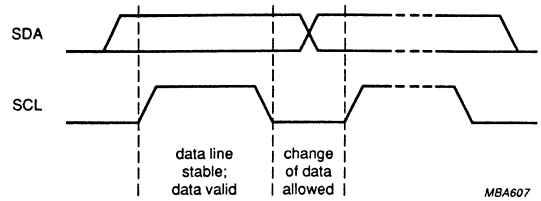


Fig.12 Bit transfer.

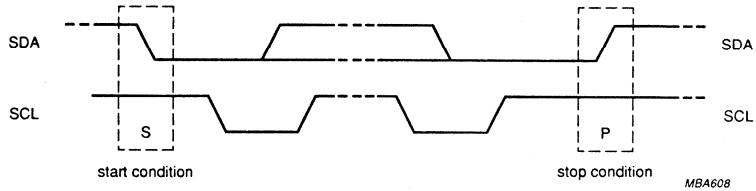


Fig.13 Definition of start and stop conditions.

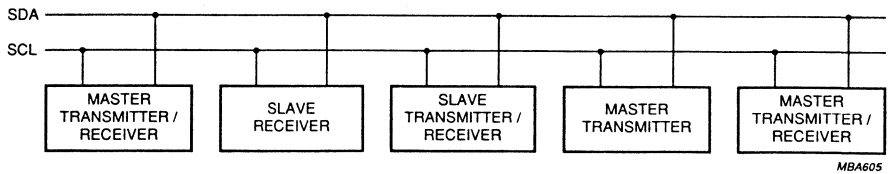


Fig.14 System configuration.

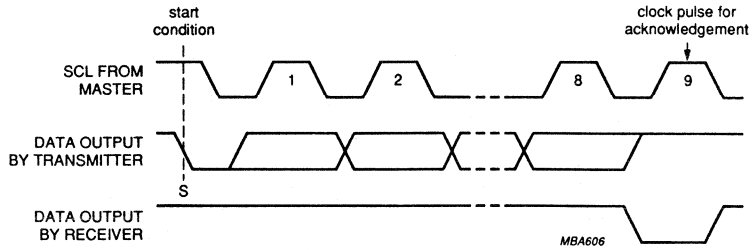


Fig.15 Acknowledgement on the I²C-bus.

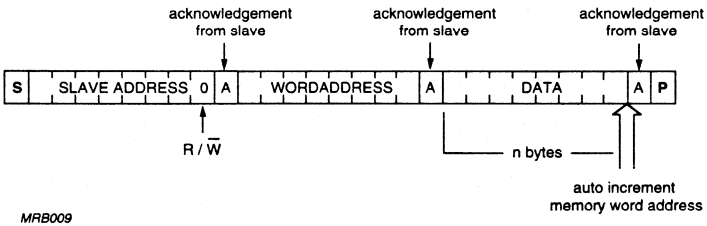


Fig.16 Master transmits to slave receiver (WRITE mode).

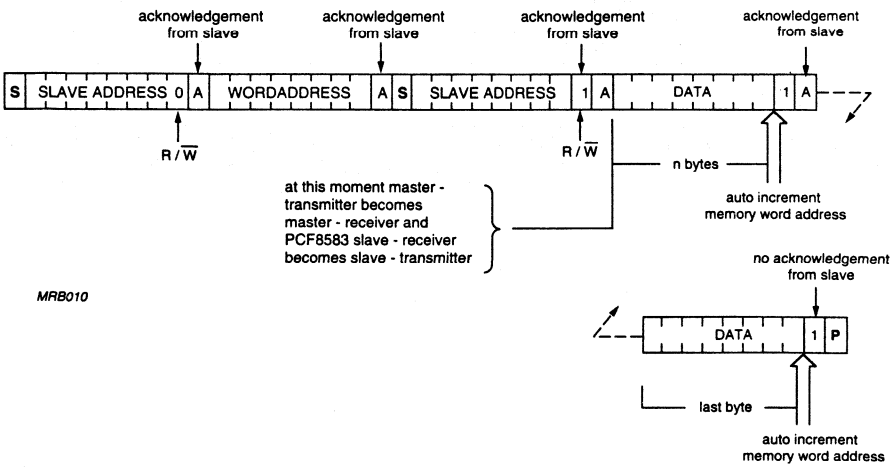


Fig.17 Master reads after setting word address (Write word address; READ data)

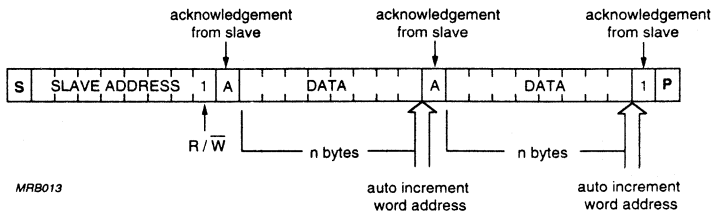


Fig.18 Master reads slave immediately after first byte (READ mode).

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage range (pin 8)	−0.8	+7.0	V
I_{SS}; I_{DD}	supply current (pin 4 or pin 8)	-	50	mA
V_I	input voltage range	−0.8 to V_{DD}	+0.8	V
I_I	DC input current	-	10	mA
I_O	DC output current	-	10	mA
P_{tot}	power dissipation per package	-	300	mW
P_O	power dissipation per output	-	50	mW
T_{amb}	operating ambient temperature range	−40	+85	°C
T_{stg}	storage temperature range	−65	+150	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

DC CHARACTERISTICS

V_{DD} = 2.5 to 6.0 V; V_{SS} = 0 V; T_{amb} = −40 to +85 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage range	I²C-bus active	2.5	-	6.0	V
		I²C-bus inactive	1.0	-	6.0	V
	quartz oscillator supply voltage range	T_{amb} = 0 to 70 °C; note 1	1.0	-	6.0	V
I_{DD}	supply current operating mode	f_{scl} =100 kHz; clock mode; note 2	-	-	200	µA
I_{DDO}	supply current clock mode	f_{scl} = 0 Hz; V_{DD} = 5 V; f_{scl} = 0 Hz; V_{DD} = 1 V	- -	10 2	50 10	µA µA
I_{DDR}	data retention	f_{OSCI} = 0 Hz; V_{DD} = 1 V; T_{amb} = −40 to +85 °C	-	-	5	µA
		f_{OSCI} = 0 Hz; V_{DD} = 1 V T_{amb} = −25 to +70 °C	-	-	2	µA
V_{EN}	I²C-bus enable level	note 3	1.5	1.9	2.3	V
SDA						
V_{IL}	input voltage LOW	note 4	−0.8	-	0.3 V_{DD}	V
V_{IH}	input voltage HIGH	note 4	0.7 V_{DD}	-	V_{DD} +0.8	V
I_{OL}	output current LOW	V_{OL} = 0.4 V	3	-	-	mA
$\|I_L\|$	leakage current	$V_I = V_{DD}$ or V_{SS}	-	-	1	µA
C_I	input capacitance	note 5	-	-	7	pF
A0; OSCI						
$\|I_L\|$	leakage current	$V_I = V_{DD}$ or V_{SS}	-	-	250	nA
$\overline{INT}$						
I_{OL}	output current LOW	V_{OL} = 0.4 V	3	-	-	mA
$\|I_L\|$	leakage current	$V_I = V_{DD}$ or V_{SS}	-	-	1	µA
SCL						
C_I	input capacitance	note 5	-	-	7	pF
$\|I_L\|$	leakage current	$V_I = V_{DD}$ or V_{SS}	-	-	1	µA

Notes

1. When powering up the device, V_{DD} must exceed 1.5 V until stable operation of the oscillator is established.
2. Event counter mode: supply current dependant upon input frequency.
3. The I²C-bus logic is disabled if $V_{DD} < V_{EN}$.
4. When the voltages are above or below the supply voltages V_{DD} or V_{SS}, an input current may flow; this current must not exceed ±0.5 mA.
5. Tested on sample basis.

AC CHARACTERISTICS

V_{DD} = 2.5 to 6.0 V; V_{SS} = 0 V; T_{amb} = −40 to +85 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Oscillator						
C_{OSC}	integrated oscillator capacitance		-	40	-	pF
f/f_{OSC}	oscillator stability	for ΔV_{DD} = 100 mV; T_{amb} = 25 °C; V_{DD} = 1.5 V	-	2×10^{-7}	-	
f_i	Input frequency	note 1	-	-	1	MHz
Quartz crystal parameters (frequency = 32.768 kHz)						
R_S	series resistance		-	-	40	kΩ
C_L	parallel capacitance		-	10	-	pF
C_T	trimmer capacitance		5	-	25	pF
I²C-bus timing (note 2)						
f_{scl}	SCL clock frequency		-	-	100	kHz
t_{SW}	tolerable spike width on bus		-	-	100	ns
t_{BUF}	bus free time		4.7	-	-	µs
$t_{SU;STA}$	start condition set-up time		4.7	-	-	µs
$t_{HD;STA}$	start condition hold time		4.0	-	-	µs
t_{LOW}	SCL LOW time		4.7	-	-	µs
t_{HIGH}	SCL HIGH time		4.0	-	-	µs
t_r	SCL and SDA rise time		-	-	1.0	µs
t_f	SCL and SDA fall time		-	-	0.3	µs
$t_{SU;DAT}$	data set-up time		250	-	-	ns
$t_{HD;DAT}$	data hold time		0	-	-	ns
$t_{VD;DAT}$	SCL LOW to data out valid		-	-	3.4	µs
$t_{SU;STO}$	stop condition set-up time		4.0	-	-	µs

Notes

1. Event counter mode only.
2. All timing values are valid within the operating supply voltage and ambient temperature range and refer V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.

Note:

The general characteristics and detailed specification of the I²C-bus are available on request.

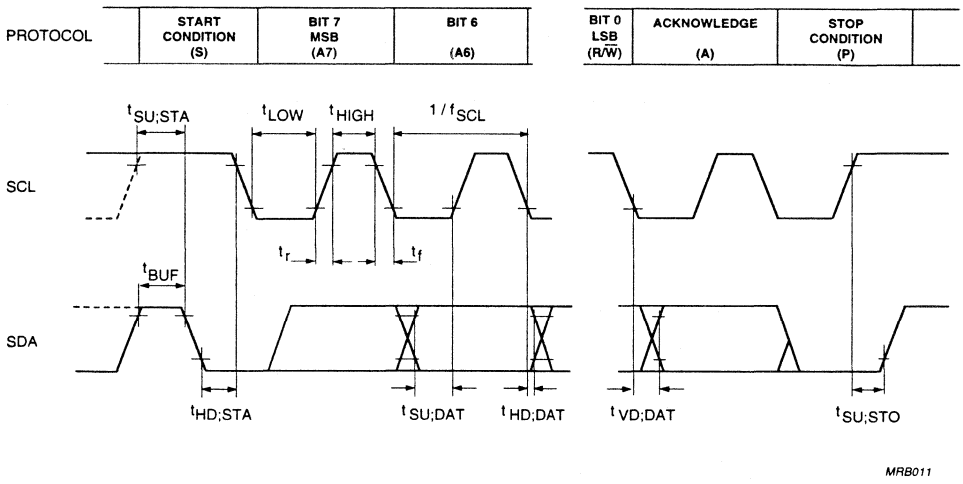


Fig.19 I²C-bus timing diagram; rise and fall times refer to V_{IL} and V_{IH}.

APPLICATION INFORMATION

Quartz frequency adjustment

METHOD 1: FIXED OSCI CAPACITOR

By evaluating the average capacitance necessary for the application layout a fixed capacitor can be used. The frequency is best measured via the 1 Hz signal available after power-on at the interrupt output (pin 7). The frequency tolerance depends on the quartz crystal tolerance, the capacitor tolerance and the device-to-device tolerance (on average ±5 x 10^{-6}). Average deviations of ±5 minutes per year can be achieved.

METHOD 2 : OSCI TRIMMER

Using the alarm function (via the I²C-bus) a signal faster than 1 Hz can be generated at the interrupt output for fast setting of a trimmer.

Procedure:

- Power-on
- Initialization (alarm functions).

Routine:

- Set clock to time T and set alarm to time T + dT
- At time T + dT (interrupt) repeat routine.

METHOD 3:

Direct measurement of OSC out (accounting for test probe capacitance).

The PCF8583 slave address has a fixed combination 1010 as group 1.

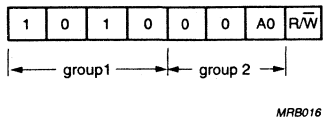


Fig.20 Slave address.

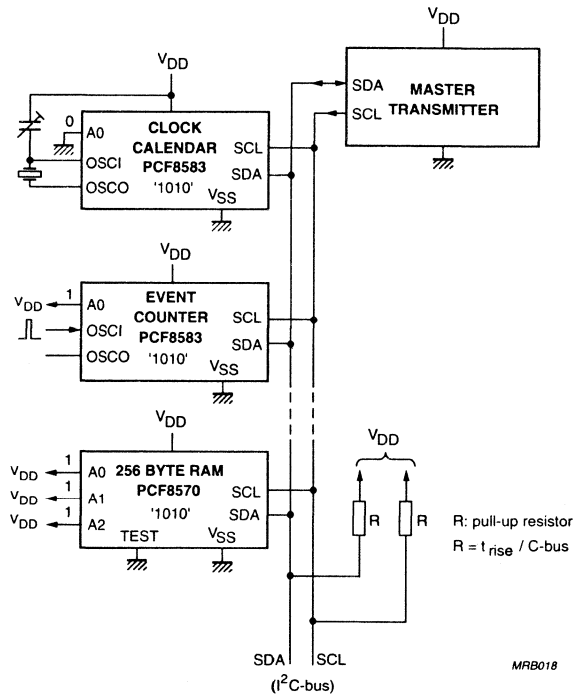


Fig.21 Application diagram.

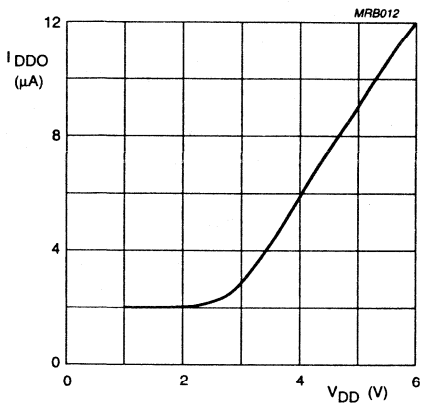


Fig.22 Typical supply current as a function of supply voltage (clock = 32 kHz; T_{amb} = −40 to +85 °C)

8-bit A/D and D/A converter PCF8591

GENERAL DESCRIPTION

The PCF8591 is a single chip, single supply low power 8-bit CMOS data acquisition device with four analogue inputs, one analogue output and a serial I²C bus interface. Three address pins A0, A1 and A2 are used for programming the hardware address, allowing the use of up to eight devices connected to the I²C bus without additional hardware. Address, control and data to and from the device are transferred serially via the two-line bidirectional bus (I²C).

The functions of the device include analogue input multiplexing, on-chip track and hold function, 8-bit analogue-to-digital conversion and an 8-bit digital-to-analogue conversion. The maximum conversion rate is given by the maximum speed of the I²C bus.

Features

- Single power supply
- Operating supply voltage 2,5 V to 6 V
- Low standby current
- Serial input/output via I²C bus
- Address by 3 hardware address pins
- Sampling rate given by I²C bus speed
- 4 analogue inputs programmable as single-ended or differential inputs
- Auto-incremented channel selection
- Analogue voltage range from V_{SS} to V_{DD}
- On-chip track and hold circuit
- 8-bit successive approximation A/D conversion
- Multiplying DAC with one analogue output

APPLICATIONS

Closed loop control systems; low power converter for remote data acquisition; battery operated equipment; acquisition of analogue values in automotive, audio and TV applications.

PACKAGE OUTLINES

PCF8591P:16-lead DIL; plastic (SOT38).
PCF8591T:16-lead mini-pack; plastic (SO16L; SOT162A).

8-bit A/D and D/A converter PCF8591

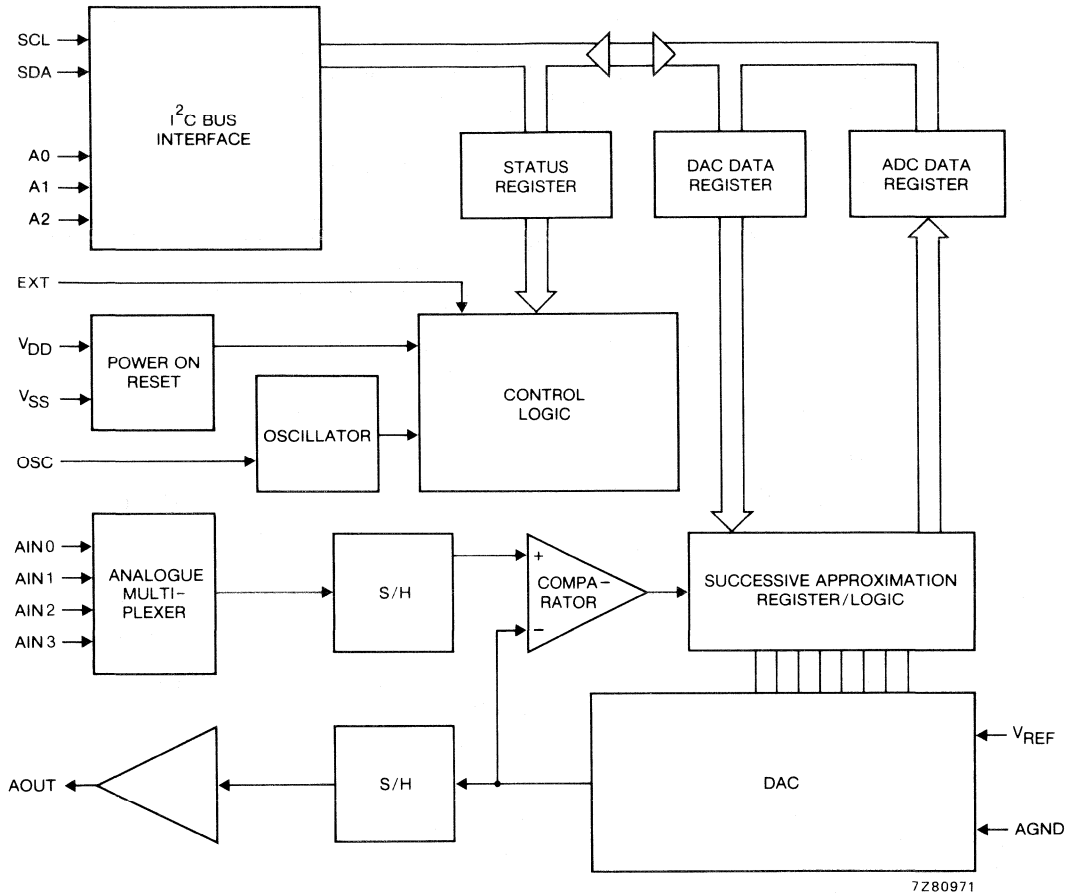


Fig. 1 Block diagram.

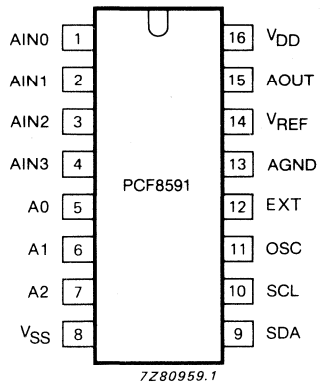


Fig. 2 Pinning diagram.

PINNING

1.	AIN0	analogue inputs (A/D converter)
2.	AIN1	
3.	AIN2	
4.	AIN3	
5.	A0	hardware address
6.	A1	
7.	A2	
8.	V_{SS}	negative supply voltage
9.	SDA	I²C bus data input/output
10.	SCL	I²C bus clock input/output
11.	OSC	oscillator input/output
12.	EXT	external/internal switch for oscillator input
13.	AGND	analogue ground
14.	V_{REF}	voltage reference input
15.	AOUT	analogue output (D/A converter)
16	V_{DD}	positive supply voltage

FUNCTIONAL DESCRIPTION

Adressing

Each PCF8591 device in an I²C bus system is activated by sending a valid address to the device. The address consists of a fixed part and a programmable part. The programmable part must be set according to the address pins A0, A1 and A2. The address always has to be sent as the first byte after the start condition in the I²C bus protocol. The last bit of the address byte is the read/write-bit which sets the direction of the following data transfer (see Figs 3 and 10).

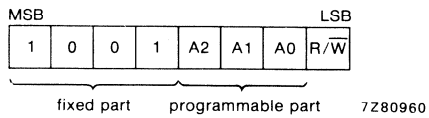


Fig. 3 Address byte.

Control byte

The second byte sent to a PCF8591 device will be stored in its control register and is required to control the device function.

The upper nibble of the control register is used for enabling the analogue output, and for programming the analogue inputs as single-ended or differential inputs. The lower nibble selects one of the analogue input channels defined by the upper nibble (see Fig. 4). If the auto-increment flag is set the channel number is incremented automatically after each A/D conversion.

The selection of a non-existing input channel results in the highest available channel number being allocated. Therefore, if the auto-increment flag is set, the next selected channel will be always channel 0. The most significant bits of both nibbles are reserved for future functions and have to be set to 0. After a power-on reset condition all bits of the control register are reset to 0. The D/A converter and the oscillator are disabled for power saving. The analogue output is switched to a high impedance state.

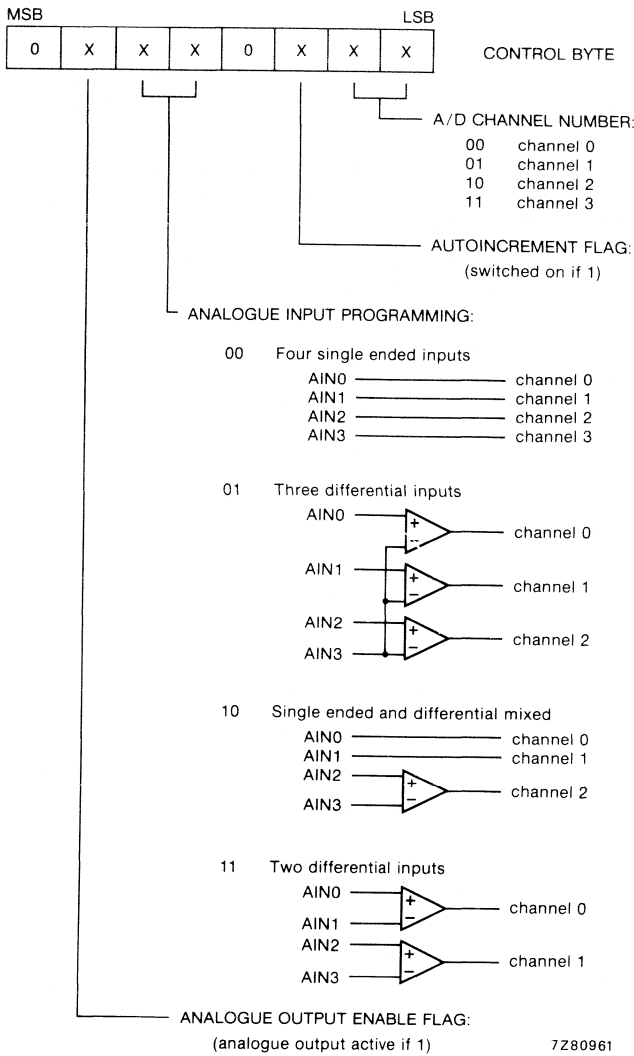


Fig. 4 Control byte.

D/A conversion

The third byte sent to a PCF8591 device is stored in the DAC data register and is converted to the corresponding analogue voltage using the on-chip D/A converter. This D/A converter consists of a resistor divider chain connected to the external reference voltage with 256 taps and selection switches. The tap-decoder switches one of these taps to the DAC output line (see Fig. 5).

The analogue output voltage is buffered by an auto-zeroed unity gain amplifier. This buffer amplifier may be switched on or off by setting the analogue output enable flag of the control register. In the active state the output voltage is held until a further data byte is sent.

The on-chip D/A converter is also used for successive approximation A/D conversion. In order to release the DAC for an A/D conversion cycle the unity gain amplifier is equipped with a track and hold circuit. This circuit holds the output voltage while executing the A/D conversion.

The output voltage supplied to the analogue output AOUT is given by the formula shown in Fig. 6. The waveforms of a D/A conversion sequence are shown in Fig. 7.

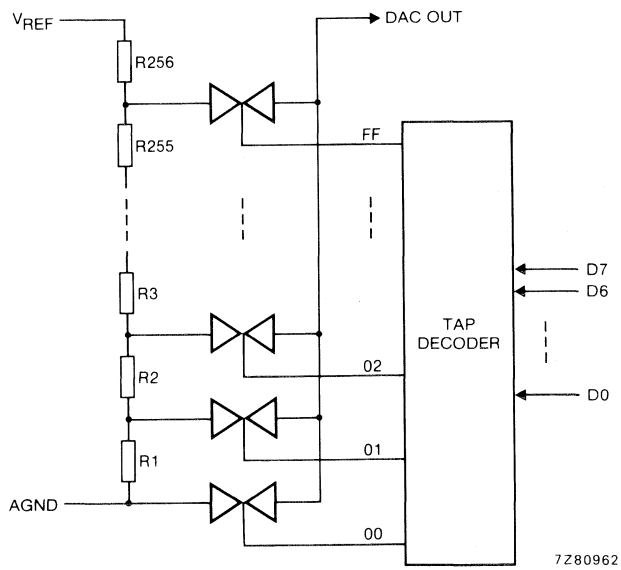


Fig. 5 DAC resistor divider chain.

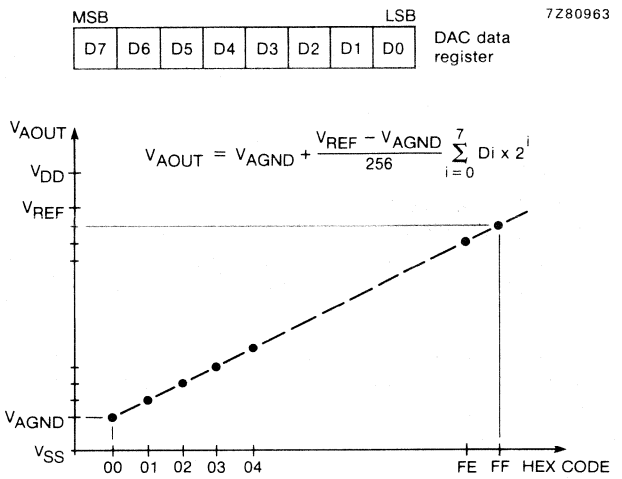


Fig. 6 DAC data and d.c. conversion characteristics.

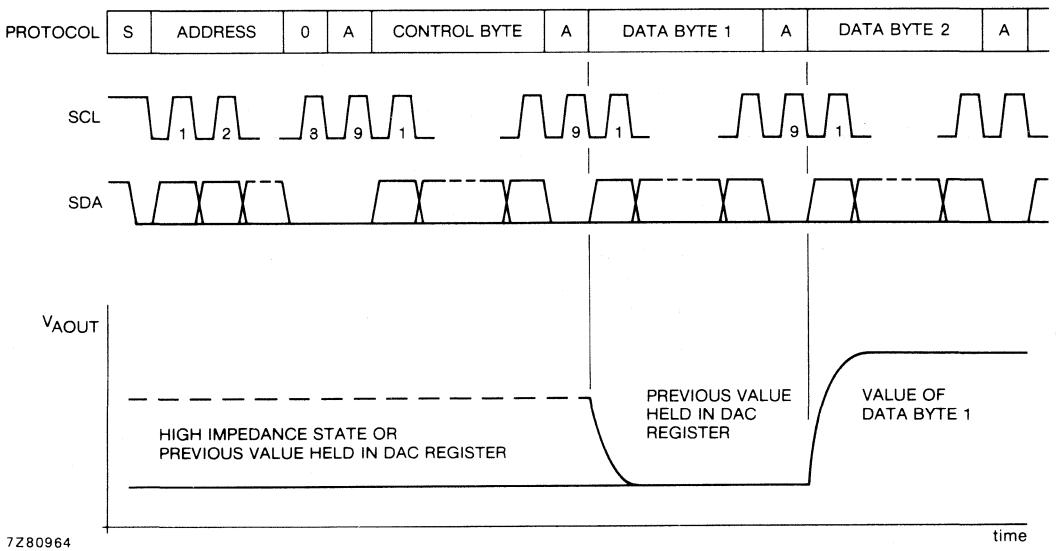


Fig. 7 D/A conversion sequence.

A/D conversion

The A/D converter makes use of the successive approximation conversion technique. The on-chip D/A converter and a high gain comparator are used temporarily during an A/D conversion cycle.

An A/D conversion cycle is always started after sending a valid read mode address to a PCF8591 device. The A/D conversion cycle is triggered at the trailing edge of the acknowledge clock pulse and is executed while transmitting the result of the previous conversion (see Fig. 8).

Once a conversion cycle is triggered an input voltage sample of the selected channel is stored on the chip and is converted to the corresponding 8-bit binary code. Samples picked up from differential inputs are converted to an 8-bit two's complement code (see Fig. 9). The conversion result is stored in the ADC data register and awaits transmission. If the auto-increment flag is set the next channel is selected.

The first byte transmitted in a read cycle contains the conversion result code of the previous read cycle. After a power-on reset condition the first byte read is a hexadecimal 80. The protocol of an I²C bus read cycle is shown in Fig. 10.

The maximum A/D conversion rate is given by the actual speed of the I²C bus.

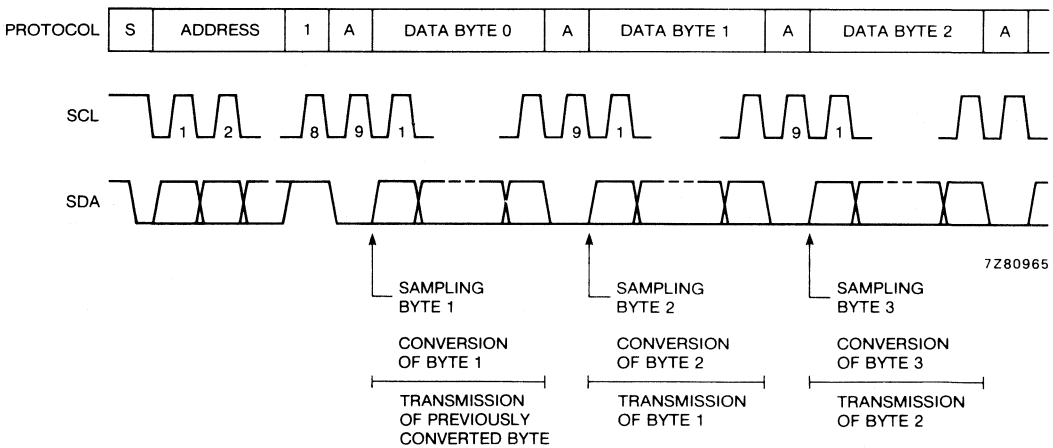


Fig. 8 A/D conversion sequence.

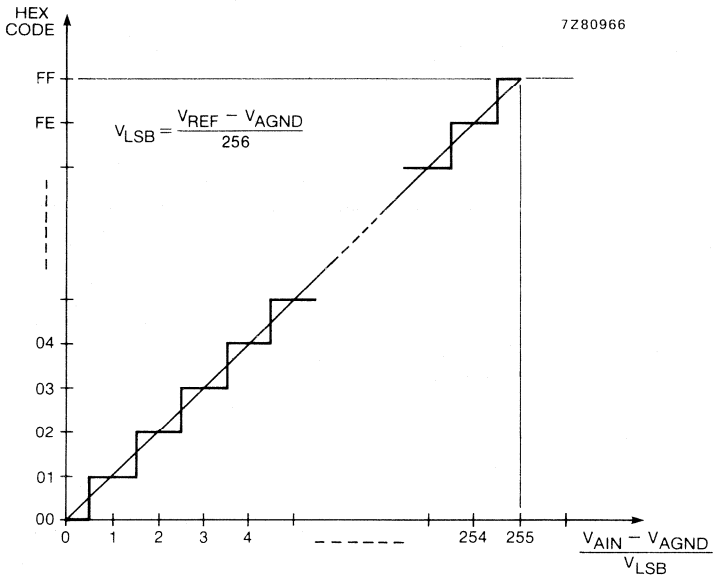


Fig. 9a A/D conversion characteristics of single-ended inputs.

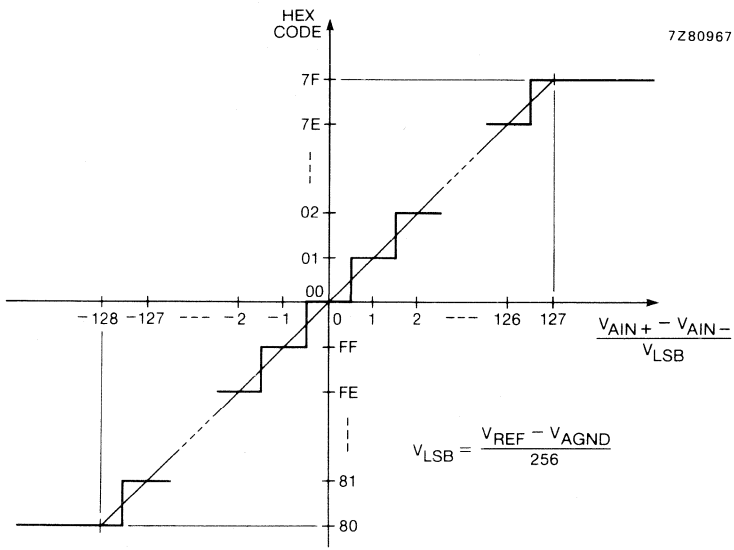


Fig. 9b A/D conversion characteristics of differential inputs.

Reference voltage

For the D/A and A/D conversion either a stable external voltage reference or the supply voltage has to be applied to the resistor divider chain (pins V_{REF} and AGND). The AGND pin has to be connected to the system analogue ground and may have a d.c. off-set with reference to V_{SS}.

A low frequency may be applied to the V_{REF} and AGND pins. This allows the use of the D/A converter as a one-quadrant multiplier; see Application Information and Fig. 6.

The A/D converter may also be used as a one or two quadrant analogue divider. The analogue input voltage is divided by the reference voltage. The result is converted to a binary code. In this application the user has to keep the reference voltage stable during the conversion cycle.

Oscillator

An on-chip oscillator generates the clock signal required for the A/D conversion cycle and for refreshing the auto-zeroed buffer amplifier. When using this oscillator the EXT pin has to be connected to V_{SS}. At the OSC pin the oscillator frequency is available.

If the EXT pin is connected to V_{DD} the oscillator output OSC is switched to a high impedance state allowing the user to feed an external clock signal to OSC.

Bus protocol

After a start condition a valid hardware address has to be sent to a PCF8591 device. The read/write bit defines the direction of the following single or multiple byte data transfer. For the format and the timing of the start condition (S), the stop condition (P) and the acknowledge bit (A) refer to the I²C bus characteristics. In the write mode a data transfer is terminated by sending either a stop condition or the start condition of the next data transfer.

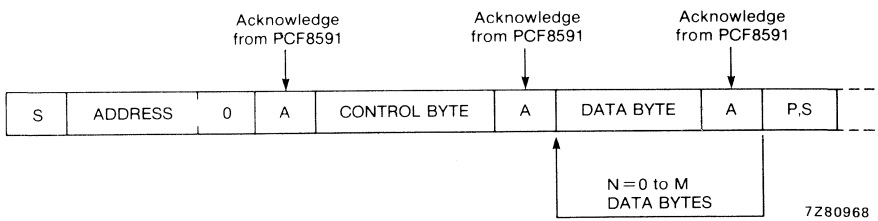


Fig. 10a Bus protocol for write mode, D/A conversion.

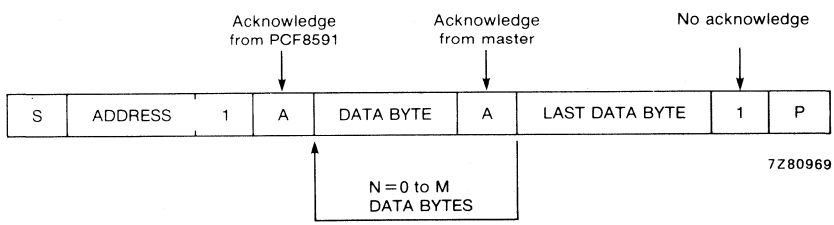


Fig. 10b Bus protocol for read mode, A/D conversion.

CHARACTERICS OF THE I²C BUS

The I²C bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transfered during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as a control signal.

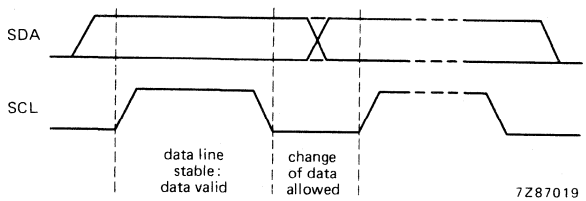


Fig. 11 Bit transfer.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH, is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH, is defined as the stop condition (P).

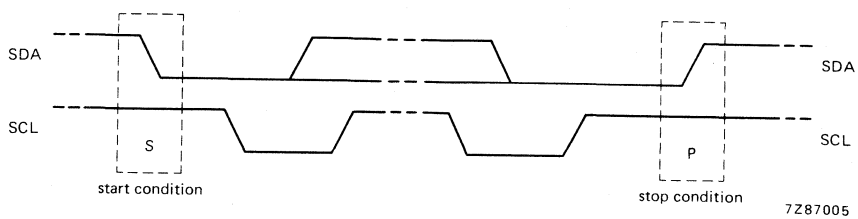


Fig. 12 Definition of start and stop condition.

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

System configuration

A device generating a message is a "transmitter", a device receiving a message is the "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

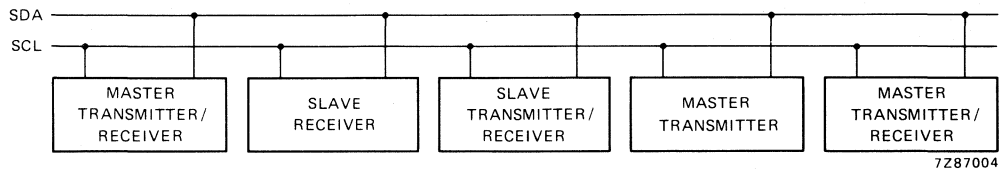


Fig. 13 System configuration.

Acknowledge.

The number of data bytes transfered between the start and stop conditions from transmitter to receiver is not limited. Each data byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master also generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

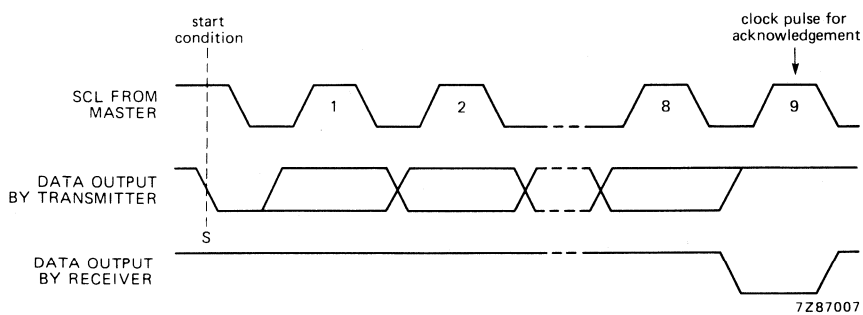


Fig. 14 Acknowledgement on the I²C bus.

Timing specifications

All the timing values are valid within the operating supply voltage and ambient temperature range and refer to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.

parameter	symbol	min.	typ.	max.	unit
SCL clock frequency	f_{SCL}	–	–	100	kHz
Tolerable spike width on bus	t_{SW}	–	–	100	ns
Bus free time	t_{BUF}	4,0	–	–	μs
Start condition set-up time	$t_{SU;STA}$	4,0	–	–	μs
Start condition hold time	$t_{HD;STA}$	4,7	–	–	μs
SCL LOW time	t_{LOW}	4,7	–	–	μs
SCL HIGH time	t_{HIGH}	4,0	–	–	μs
SCL and SDA rise time	t_R	–	–	1,0	μs
SCL and SDA fall time	t_F	–	–	0,3	μs
Data set-up time	$t_{SU;DAT}$	250	–	–	ns
Data hold time	$t_{HD;DAT}$	0	–	–	ns
SCL LOW to data out valid	$t_{VD;DAT}$	–	–	3,4	μs
Stop condition set-up time	$t_{SU;STO}$	4,0	–	–	μs

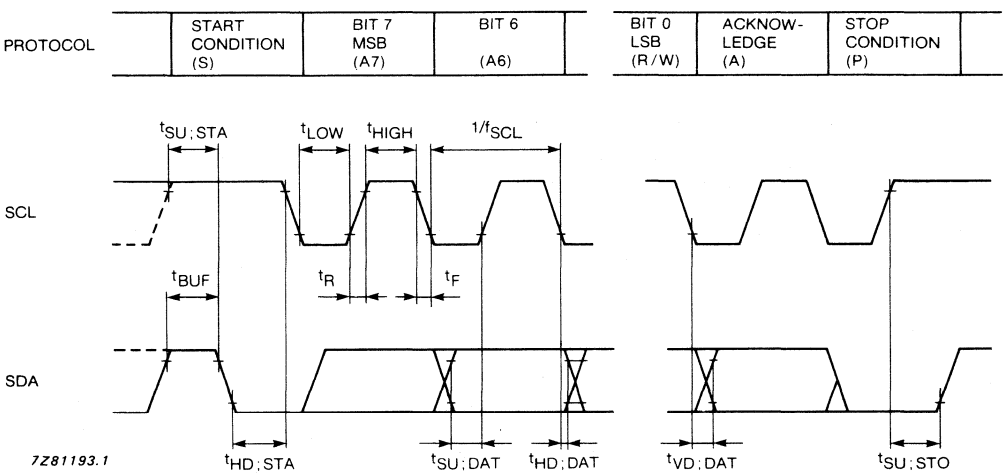


Fig. 15 I²C bus timing diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range	V_{DD}		−0,5 to +8,0 V
Voltage on any pin	V_I		−0,5 to V_{DD} +0,5 V
Input current d.c.	I_I	max.	10 mA
Output current d.c.	I_O	max.	20 mA
V_{DD} or V_{SS} current	I_{DD}, I_{SS}	max.	50 mA
Power dissipation per package	P_{tot}	max.	300 mW
Power dissipation per output	P	max.	100 mW
Storage temperature range	T_{stg}		−65 to +150 °C
Operating ambient temperature range	T_{amb}		−40 to +85 °C

Note:

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is advised to take handling precautions appropriate to handling MOS devices (see 'Handling MOS devices').

CHARACTERISTICS

V_{DD} = 2,5 V to 6 V; V_{SS} = 0 V; T_{amb} = −40 °C to +85 °C unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage	operating	V_{DD}	2,5	–	6,0	V
Supply current	standby $V_I = V_{SS}$ or V_{DD}; no load	I_{DD0}	–	1	15	μA
Supply current	operating; AOUT off; f_{SCL} = 100 kHz	I_{DD1}	–	125	250	μA
Supply current	AOUT active; f_{SCL} = 100 kHz	I_{DD2}	–	0,45	1,0	mA
Power-on reset level	note 1	V_{POR}	0,8	–	2,0	V
Digital inputs/output	SCL, SDA, A0, A1, A2					
Input voltage	LOW	V_{IL}	0	–	0,3 x V_{DD}	V
Input voltage	HIGH	V_{IH}	0,7 x V_{DD}	–	V_{DD}	V
Input current	leakage; $V_I = V_{SS}$ to V_{DD}	I_I	–	–	250	nA
Input capacitance		C_I	–	–	5	pF
SDA output current	leakage; HIGH at $V_{OH} = V_{DD}$	I_{OH}	–	–	250	nA
SDA output current	LOW at V_{OL} = 0,4 V	I_{OL}	3,0	–	–	mA

parameter	conditions	symbol	min.	typ.	max.	unit
Reference voltage inputs						
Voltage range*	$V_{REF} > V_{AGND}$	V_{REF}	$V_{SS}+1,6$	–	V_{DD}	V
Voltage range*	$V_{REF} > V_{AGND}$	V_{AGND}	V_{SS}	–	$V_{DD}-0,8$	V
Input current	leakage	I_I	–	–	250	nA
Input resistance	V_{REF} to AGND	R_{REF}	–	100	–	kΩ
Oscillator	OSC, EXT					
Input current	leakage	I_I	–	–	250	nA
Oscillator frequency		f_{OSC}	0,75	–	1,25	MHz

D/A CHARACTERISTICS

V_{DD} = 5,0 V; V_{SS} = 0 V; V_{REF} = 5,0 V; V_{AGND} = 0 V; R_{load} = 10 kΩ; C_{load} = 100 pF; T_{amb} = −40 °C to +85 °C unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Analogue output						
Output voltage range	no resistive load	V_{OA}	V_{SS}	–	V_{DD}	V
Output voltage range	R_{load} = 10 kΩ	V_{OA}	V_{SS}	–	$0,9 \times V_{DD}$	V
Output current	leakage; AOUT disabled	I_{LO}	–	–	250	nA
Accuracy						
Offset error	T_{amb} = 25 °C	OS_e	–	–	50	mV
Linearity error		L_e	–	–	±1,5	LSB
Gain error	no resistive load	G_e	–	–	1	%
Settling time	to ½ LSB full scale step	t_{DAC}	–	–	90	μs
Conversion rate		f_{DAC}	–	–	11,1	kHz
Supply noise rejection	at f = 100 Hz; V_{DD} = 0,1 V_{PP}	SNRR	–	40	–	dB

* A further extension of the range is possible, if the following conditions are fulfilled:

$$\frac{V_{REF} + V_{AGND}}{2} \geqslant 0,8\ V \text{ and } V_{DD} - \frac{V_{REF} + V_{AGND}}{2} \geqslant 0,4\ V.$$

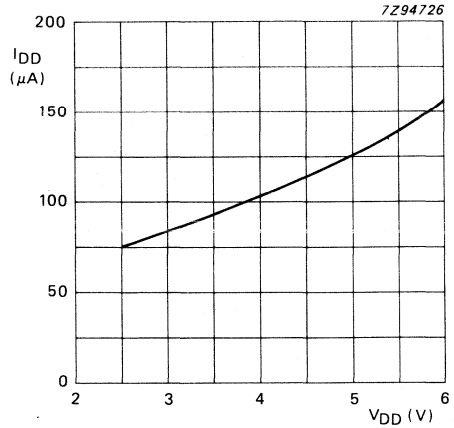
A/D CHARACTERISTICS

V_{DD} = 5,0 V; V_{SS} = 0 V; V_{REF} = 5,0 V; V_{AGND} = 0 V; R_{source} = 10 kΩ; T_{amb} = −40 °C to +85 °C unless otherwise specified

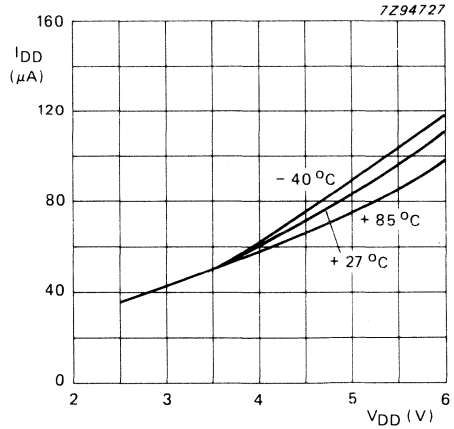
parameter	conditions	symbol	min.	typ.	max.	unit
Analogue inputs						
Input voltage range		V_{IA}	V_{SS}	–	V_{DD}	V
Input current	leakage	I_{IA}	–	–	100	nA
Input capacitance		C_{IA}	–	10	–	pF
Input capacitance	differential	C_{ID}	–	10	–	pF
Single-ended voltage	measuring range	V_{IS}	V_{AGND}	–	V_{REF}	V
Differential voltage	measuring range; $V_{FS} = V_{REF} - V_{AGND}$	V_{ID}	$\frac{-V_{FS}}{2}$	–	$\frac{+V_{FS}}{2}$	V
Accuracy						
Offset error	T_{amb} = 25 °C	OS_e	–	–	20	mV
Linearity error		L_e	–	–	±1,5	LSB
Gain error		G_e	–	–	1	%
Gain error	small-signal; ΔV_{IN} = 16 LSB	GS_e	–	–	5	%
Rejection ratio	common-mode	CMRR	–	60	–	dB
Supply noise rejection	at f = 100 Hz; V_{DDN} = 0,1xV_{PP}	SNRR	–	40	–	dB
Conversion time		t_{ADC}	–	–	90	μs
Sampling/conversion rate		f_{ADC}	–	–	11,1	kHz

Note

1. The power on reset circuit resets the I²C bus logic when V_{DD} is less than V_{POR}.

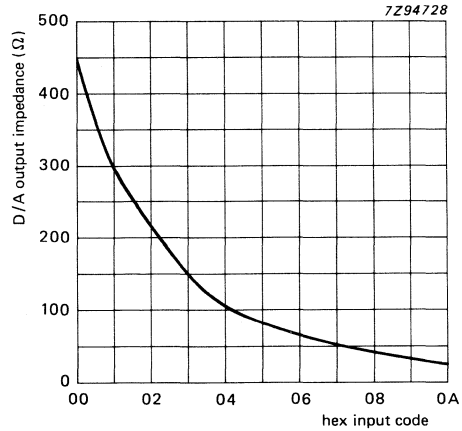


(a) internal oscillator; T_{amb} = + 27 °C.

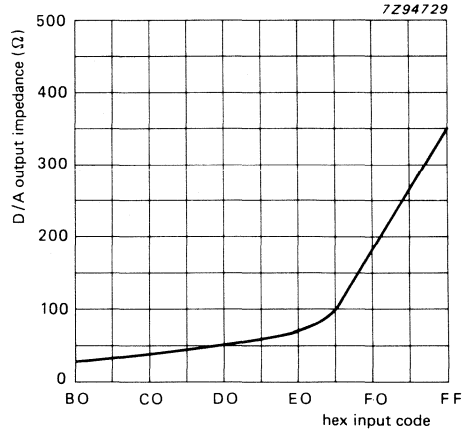


(b) external oscillator.

Fig. 16 Operating supply current against supply voltage (analogue output disabled).



(a) output impedance near negative power rail; T_{amb} = + 27 °C.



(b) output impedance near positive power rail; T_{amb} = + 27 °C.

Fig. 17 Output impedance of analogue output buffer (near power rails).

The x-axis represents the hex input-code equivalent of the output voltage.

APPLICATION INFORMATION

Inputs must be connected to V_{SS} or V_{DD} when not in use. Analogue inputs may also be connected to AGND or V_{REF}.

In order to prevent excessive ground and supply noise and to minimize cross-talk of the digital to analogue signal paths the user has to design the printed-circuit board layout very carefully. Supply lines common to a PCF8591 device and noisy digital circuits and ground loops should be avoided. Decoupling capacitors (> 10 μF) are recommended for power supply and reference voltage inputs.

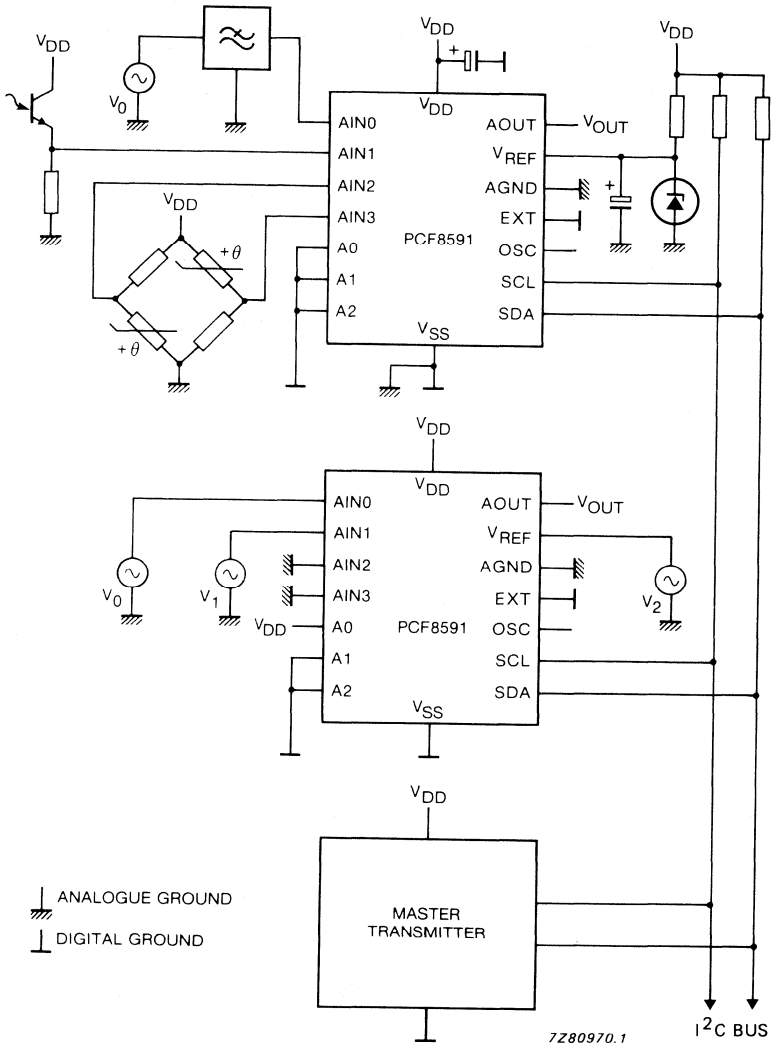


Fig. 18 Application diagram.

512 × 8-bit static CMOS EEPROM with I²C-bus interface

PCF8594

FEATURES

- Low Power CMOS
  maximum active current 2.5 mA
  maximum standby current 10 µA
- Non-volatile storage of 4-Kbits organized as two pages
  each 256 x 8-bits
- Only one power supply required
- On-chip voltage multiplier
- Serial input/output bus (I²C)
- Write operations
  byte write mode
  8-byte page write mode (minimizes total write time per byte)
- Write-protection input
- Read operations
  sequential read
  random read
- Extended supply voltage range (2.5 to 6.0 V)
- Internal timer for writing (no external components)
- Power-on reset
- High reliability by using a redundant storage code
  (single bit error correction)
- Endurance
  100 k; T_{amb} = 85 °C
- 10 years non-volatile data retention time
- Pin and Address compatible to
  PCF8570, PCF8571, PCF8572, PCF8581, PCF8582A, PCA8582B and PCF8582C

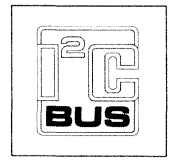
GENERAL DESCRIPTION

The PCF8594 is a 4-Kbit (512 x 8-bit) floating gate electrically erasable programmable read only memory (EEPROM). By using an internal redundant storage code it is fault tolerant to single bit errors. This feature dramatically increases reliability compared to conventional EEPROM memories.

Power consumption is low due to the full CMOS technology used. The programming voltage is generated on chip, using a voltage multiplier.

As data bytes are received and transmitted via the serial I²C-bus, a package using eight pins is sufficient. Up to four PCF8594 devices may be connected to the I²C-bus. Chip select is accomplished by two address inputs.

Timing of the Erase/Write cycle is done internally, thus no external components are required. Pin 7 must be connected to either V_{DD} or left open-circuit.



There is an option of using an external clock for timing the length of an Erase/Write cycle.

A write protection input (pin 1) allows disable of write-commands from the master by a hardware signal. When pin 1 is HIGH and one of the upper 256 EEPROM cells is addressed, then the data bytes will not be acknowledged by the PCF8594 and the EEPROM-contents are not changed.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage		2.5	6.0	V
I_{DDR}	supply current READ	f_{SCL} = 100 kHz			
		V_{DD} = 3 V	-	0.1	mA
		V_{DD} = 6 V	-	0.4	mA
I_{DDW}	supply current ERASE/WRITE	f_{SCL} = 100 kHz			
		V_{DD} = 3 V	-	0.35	mA
		V_{DD} = 6 V	-	2.5	mA
I_{DDO}	supply current STANDBY				
		V_{DD} = 3 V	-	3.5	µA
		V_{DD} = 6 V	-	10	µA

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
PCF8594P	8	DIL	plastic	SOT97
PCF8594T	8	mini-pack	plastic	SO8; SOT96A

512 × 8-bit static CMOS EEPROM with I²C-bus interface

PCF8594

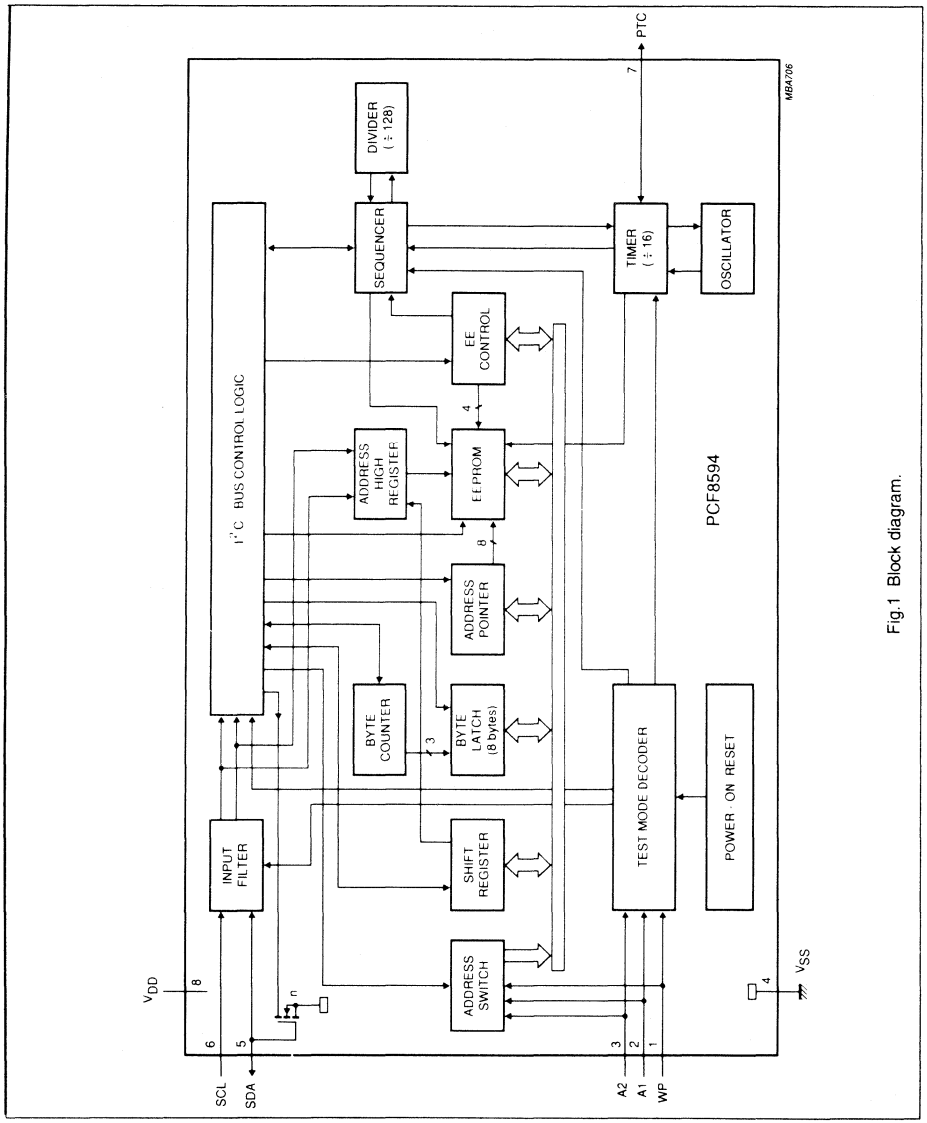


Fig.1 Block diagram.

512 × 8-bit static CMOS EEPROM with I²C-bus interface

PCF8594

PIN CONFIGURATION

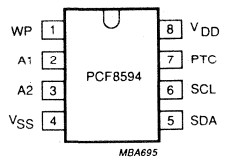


Fig.2 Pin configuration.

PINNING

SYMBOL	PIN	DESCRIPTION
WP	1	write-protect
A1	2	address input
A2	3	address input
V_{SS}	4	negative supply voltage
SDA	5	serial data line I²C-bus
SCL	6	serial clock line I²C-bus
PTC	7	programming time control
V_{DD}	8	positive supply voltage

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage		−0.3	+7.0	V
V_I	voltage on any input pin	$\|Z_I\| > 500\ \Omega$	V_{SS} −0.8	V_{DD} +0.8	V
I_I	current on any input pin		-	1	mA
I_O	output current		-	10	mA
T_{stg}	storage temperature range		−65	+150	°C
T_{amb}	operating ambient temperature range		−40	+85	°C

512 × 8-bit static CMOS EEPROM with I²C-bus interface

PCF8594

CHARACTERISTICS

V_{DD} = 2.5 to 6 V; V_{SS} = 0 V; T_{amb} = −40 to +85 °C; unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Supplies					
V_{DD}	supply voltage		2.5	6.0	V
I_{DDR}	supply current READ	f_{SCL} = 100 kHz			
		V_{DD} = 3 V	-	0.1	mA
		V_{DD} = 6 V	-	0.4	mA
I_{DDW}	supply current ERASE/WRITE	f_{SCL} = 100 kHz			
		V_{DD} = 3 V	-	0.35	mA
		V_{DD} = 6 V	-	2.5	mA
I_{DDO}	supply current STANDBY				
		V_{DD} = 3 V	-	3.5	µA
		V_{DD} = 6 V	-	10	µA
PTC input					
V_{IL}	input voltage LOW		−0.8	0.1 V_{DD}	V
V_{IH}	input voltage HIGH		0.9 V_{DD}	V_{DD} +0.8	V
SCL input					
V_{IL}	input voltage LOW		−0.8	0.3 V_{DD}	V
V_{IH}	input voltage HIGH		0.7 V_{DD}	V_{DD} +0.8	V
I_{LI}	input leakage current	V_I = V_{DD} or V_{SS}	-	± 1	µA
f_{SCL}	clock frequency		0	100	kHz
C	input capacitance	V_I = V_{SS}	-	7	pF
SDA input/output					
V_{IL}	input voltage LOW		−0.8	0.3 V_{DD}	V
V_{IH}	input voltage HIGH		0.7 V_{DD}	V_{DD} +0.8	V
V_{OL}	output voltage LOW	I_{OH} = 3 mA; V_{DD} = 2.5 V	-	0.4	V
I_{LO}	output leakage current	V_{OH} = V_{DD}	-	1	µA
C	input capacitance	V_I = V_{SS}	-	7	pF
Data retention time					
t_S	data retention time	T_{amb} = 55 °C	10	-	yrs

WRITE CYCLE LIMITS

The power-on reset circuit resets the I²C-bus logic with a set-up time ≤ 10 µs.

Selection of the chip address is achieved by connecting the A1 and A2 inputs to either V_{SS} or V_{DD}.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_{EW}	ERASE/WRITE cycle time					
		internal oscillator	5	10	25	ms
		external clock	5	-	25	ms
Endurance						
$N_{E/W}$	ERASE/WRITE cycles per byte	T_{amb} = 85 °C; $t_{E/W}$ = 5 to 25 ms	-	-	100 000	
Programming						
f_p	programming frequency		10	-	50	kHz
t_{LOW}	LOW time		5	-	-	µs
t_{HIGH}	HIGH time		5	-	-	µs
t_r	rise time		-	-	300	ns
t_f	fall time		-	-	300	ns
t_d	delay time		0	-	t_{LOW}	µs

512 × 8-bit static CMOS EEPROM with I²C-bus interface

PCF8594

I²C-bus PROTOCOL

The I²C-bus is for 2-way, 2-line communication between different ICs or modules. The serial bus consists of two bidirectional lines: one for data signals (SDA), and one for clock signals (SCL).
Both the SDA and SCL lines must be connected to a positive supply voltage via a pull-up resistor.

The following protocol has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as control signals.

The following bus conditions have been defined:

Bus not busy: both data and clock lines remain HIGH.

Start data transfer: a change in the state of the data line, from HIGH-to-LOW, while the clock is HIGH defines the start condition.

Stop data transfer: a change in the state of the data line, from LOW-to-HIGH, while the clock is HIGH, defines the stop condition.

Data valid: the state of the data line represents valid data when, after a start condition, the data line is stable for the duration of the HIGH period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a start condition and terminated with a stop condition; the number of the data bytes, transferred between the start and stop conditions is limited to seven bytes in the ERASE/WRITE mode and eight bytes in the PAGE ERASE/WRITE mode. Data transfer is unlimited in the READ mode. The information is transmitted in bytes and each receiver acknowledges with a ninth bit.

Within the I²C-bus specifications a low-speed mode (2 kHz clock rate) and a high speed mode (100 kHz clock rate) are defined.
The PCF8594 operates in both modes.

By definition a device that sends a signal is called a "transmitter", and the device which receives the signal is called a "receiver". The device which controls the signal is called the "master". The devices that are controlled by the master are called "slaves".

Each byte is followed by one acknowledge bit. This acknowledge bit is a HIGH level, put on the bus by the transmitter. The master generates an extra acknowledge related clock pulse. The slave receiver which is addressed is obliged to generate an acknowledge after the reception of each byte.

The master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.

The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse.

Set-up and hold times must be taken into account. A master receiver must signal an end of data to the slave transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master generation of the stop condition.

DEVICE ADDRESSING

Following a start condition the bus master must output the address of the slave it is accessing. The most significant four bits of the slave address are the device type identifier (see Fig. 3). For the PCF8594 this is fixed as 1010.

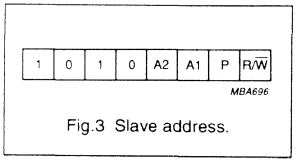


Fig.3 Slave address.

The next two significant bits address a particular device. A system could have up to four PCF8594 devices on the bus. The four addresses are defined by the state of the A1 and A2 inputs.

The next bit (bit 1) of the slave address field is the page selection bit. It is used by the host to select the upper/lower 256 bytes of memory. This is, in effect, the most significant bit for the word address.

The last bit of the slave address defines the operation to be performed. When set to logic 1 a read operation is selected.

WRITE OPERATIONS

Byte/word write

For a write operation the PCF8594 requires a second address field. This address field is a word address providing access to any one of the 256 words of memory. Upon receipt of the word address the PCF8594 responds with an acknowledge and awaits the next eight bits of data, again responding with an acknowledge. Word address is automatically incremented. The master can now terminate the transfer by generating a stop condition or transmit up to six more bytes of data and then terminate by generating a stop condition.

After this stop condition the ERASE/WRITE cycle starts and the bus is free for another transmission. Its duration is 10 ms per byte. During the ERASE/WRITE cycle the slave receiver does not send an acknowledge bit if addressed via the I²C-bus.

PAGE WRITE

The PCF8594 is capable of a eight-byte page write operation. It is initiated in the same manner as the byte write operation. The master can transmit eight data bytes within one transmission. After receipt of each byte the PCF8594 will respond with an acknowledge.

After the receipt of each data byte the three low order bits of the word address are internally incremented. The high order five bits of the address remain unchanged. If the master transmits more than eight bytes prior to generating the stop condition, no acknowledge will be given on the ninth (and following) data bytes and the whole transmission will be ignored. As in the byte write operation, all inputs are disabled until completion of the internal write cycles. The typical duration of a page write is 45 ms.

Note

A write to the EEPROM is always performed if the pin WP is LOW. If WP is HIGH, then the upper half of the EEPROM is write-protected and no acknowledge will be given by the PCF8594 when one of the upper 256 EEPROM cells is addressed. However, an acknowledge will be given after the slave address and the word address.

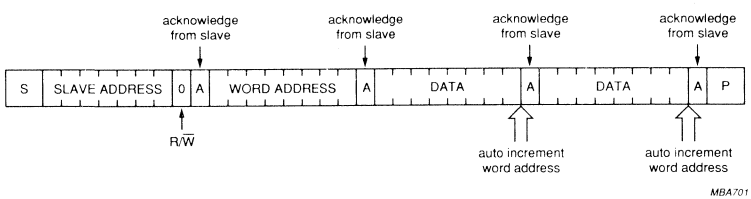


Fig.4 Auto increment memory word address; two byte write.

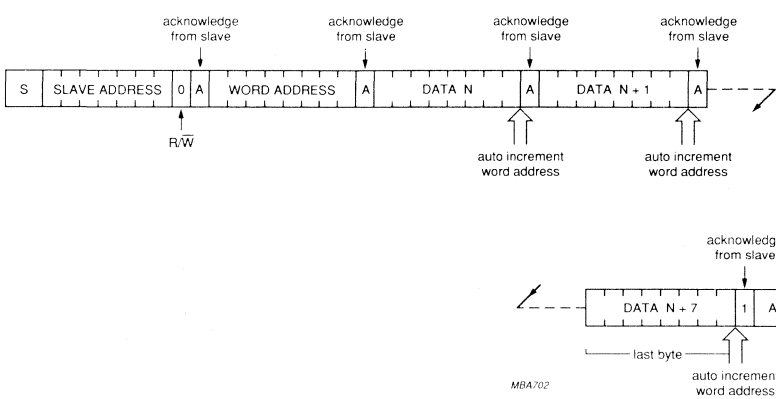


Fig.5 Page write operation; eight byte.

READ OPERATIONS

Read operations are initiated in the same manner as write operations with the exception that the LSB of the slave address is set to logic 1. There are three basic read operations; current address read, random read and sequential read.

Note

The lower 8-bits of the word address are incremented after each transmission of a data byte (read or write). The MSB of the word address, which is defined in the slave address, is not changed when the word address count overflows. Thus, the word address overflows from 255 to 0 and from 511 to 256.

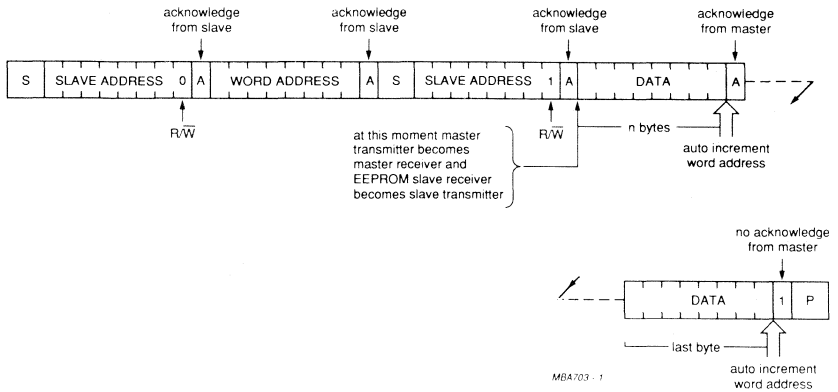


Fig.6 Master reads PCF8594 slave after setting word address (WRITE word address; READ data).

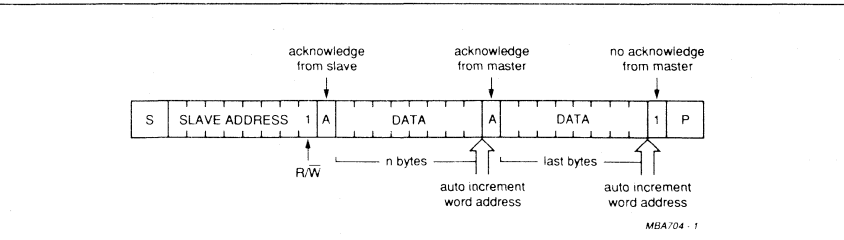


Fig.7 Master reads PCF8594 immediately after first byte (READ mode).

I²C-bus TIMING

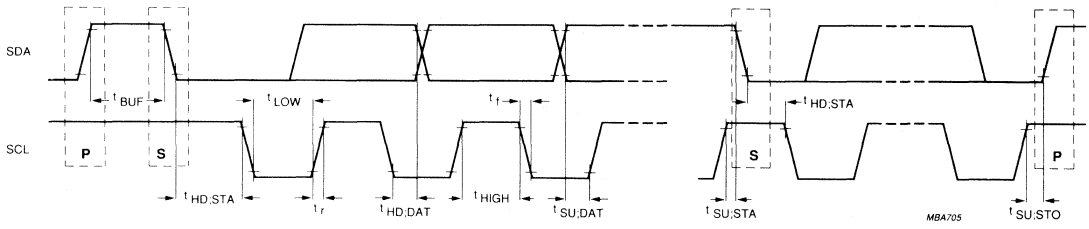


Fig.8 Timing requirements for the I²C-bus.

I²C-bus CHARACTERISTICS

(note 1)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
f_{SCL}	clock frequency		0	100	kHz
t_{BUF}	time the bus must be free before a new transmission can start		4.7	-	µs
$t_{HD;STA}$	start condition hold time after which first clock pulse is generated		4.0	-	µs
t_{LOW}	clock period LOW		4.7	-	µs
t_{HIGH}	clock period HIGH		4.0	-	µs
$t_{SU;STA}$	set-up time for start condition	repeated start	4.7	-	µs
$t_{HD;DAT}$	data hold time for bus compatible masters		5	-	µs
$t_{HD;DAT}$	data hold time for bus devices	note 2	0	-	ns
$t_{SU;DAT}$	data set-up time		250	-	ns
t_r	SDA and SCL rise time		-	1	µs
t_f	SDA and SCL fall time		-	300	ns
$t_{SU;STO}$	set-up time for stop condition		4.7	-	µs

Notes to the I²C-bus characteristics

1. All the timing values are valid within the operating supply voltage and ambient temperature range and refer to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.
2. The hold time required to bridge the undefined region of the falling edge of SCL must be internally provided by a transmitter. It is not greater than 300 ns.

EXTERNAL CLOCK TIMING

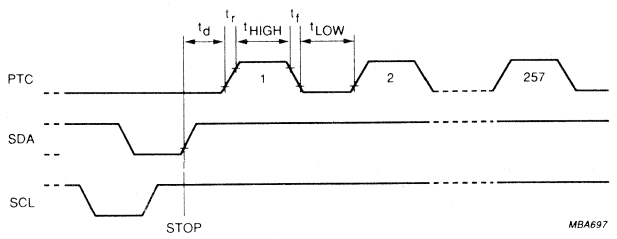


Fig.9 One byte ERASE/WRITE cycle.

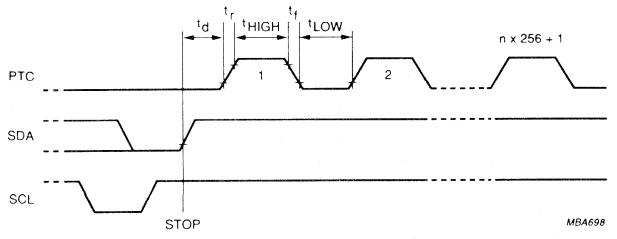


Fig.10 n byte ERASE/WRITE cycle (n = 2 to 7).

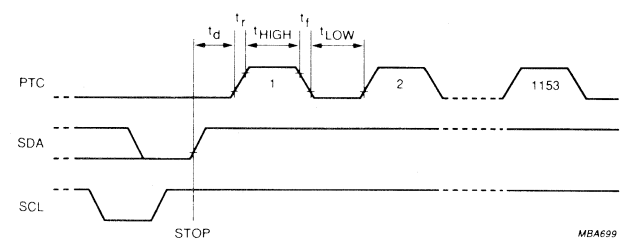
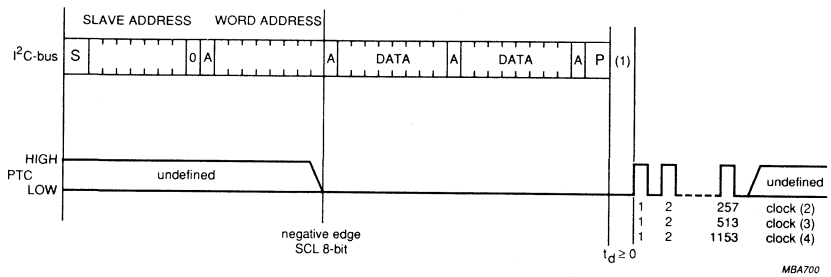


Fig.11 Page mode.



(1) If an external clock is chosen, this information is latched internally by setting pin 7 (PTC) LOW after transmission of the eight bit of the word address (negative edge of SCL). Thus the state of pin 7 may be previously undefined. Leaving pin 7 LOW causes a higher standby current.

(2) 1-byte programming.

(3) 2-byte programming.

(4) One page (8 byte) programming.

Fig.12 External clock.

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

1024 × 8-bit static CMOS EEPROM with I²C-bus interface

PCF8598

FEATURES

- Low Power CMOS
  - maximum active current 2.0 mA
  - maximum standby current 10 µA
- Non-volatile storage of 8 k bits organized as four pages
  - each 256 x 8 bits
- Only one power supply required
- On-chip voltage multiplier
- Serial input/output bus (I²C)
- Write operations
  - byte write mode
  - 8-byte page write mode (minimizes total write time per byte)
- Write-protection input
- Read operations
  - sequential read
  - random read
- Extended supply voltage range (2.5 to 6.0 V)
- Internal timer for writing (no external components)
- Power-on reset
- High reliability by using a redundant storage code
  - (single bit error correction)
- Endurance
  - 100 k; Tamb = 85 °C
- 10 years non-volatile data retention time
- Pin and Address compatible to
  - PCF8570, PCF8571, PCF8572, PCF8581, PCF8582A, PCA8582B, PCF8582C, PCF8582D, PCF8582E and PCF8594

GENERAL DESCRIPTION

The PCF8598 is a 8 Kbit (1024 x 8 bit) floating gate electrically erasable programmable read only memory (EEPROM). By using an internal redundant storage code it is fault tolerant to single bit errors. This feature dramatically increases reliability compared to conventional EEPROM memories.

Power consumption is low due to the full CMOS technology used. The programming voltage is generated on chip, using a voltage multiplier.

As data bytes are received and transmitted via the serial I²C-bus, a package using eight pins is sufficient. Up to two PCF8598 devices may be connected to the I²C-bus.

Chip select is accomplished by one address input.

Timing of the Erase/Write cycle is done internally, thus no external components are required. Pin 7 must be connected to either V_{DD} or left open-circuit.

There is an option of using an external clock for timing the length of an Erase/Write cycle.

A write protection input (pin 1) allows disable of write-commands from the master by a hardware signal. When pin 1 is HIGH and one of the upper 512 EEPROM cells is addressed, then the data bytes will not be acknowledged by the PCF8598 and the EEPROM-contents are not changed.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage	2.5	-	6.0	V
I_{DDR}	supply current READ	0.1	-	0.4	mA
I_{DDW}	supply current WRITE/ERASE	0.35	-	2.5	mA
I_{DDO}	standby supply current	3.5	-	10	µA

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
PCF8598P	8	DIL	plastic	SOT97
PCF8598T	16	mini-pack	plastic	SO16L; SOT162A

1024 × 8-bit static CMOS EEPROM with I²C-bus interface

PCF8598

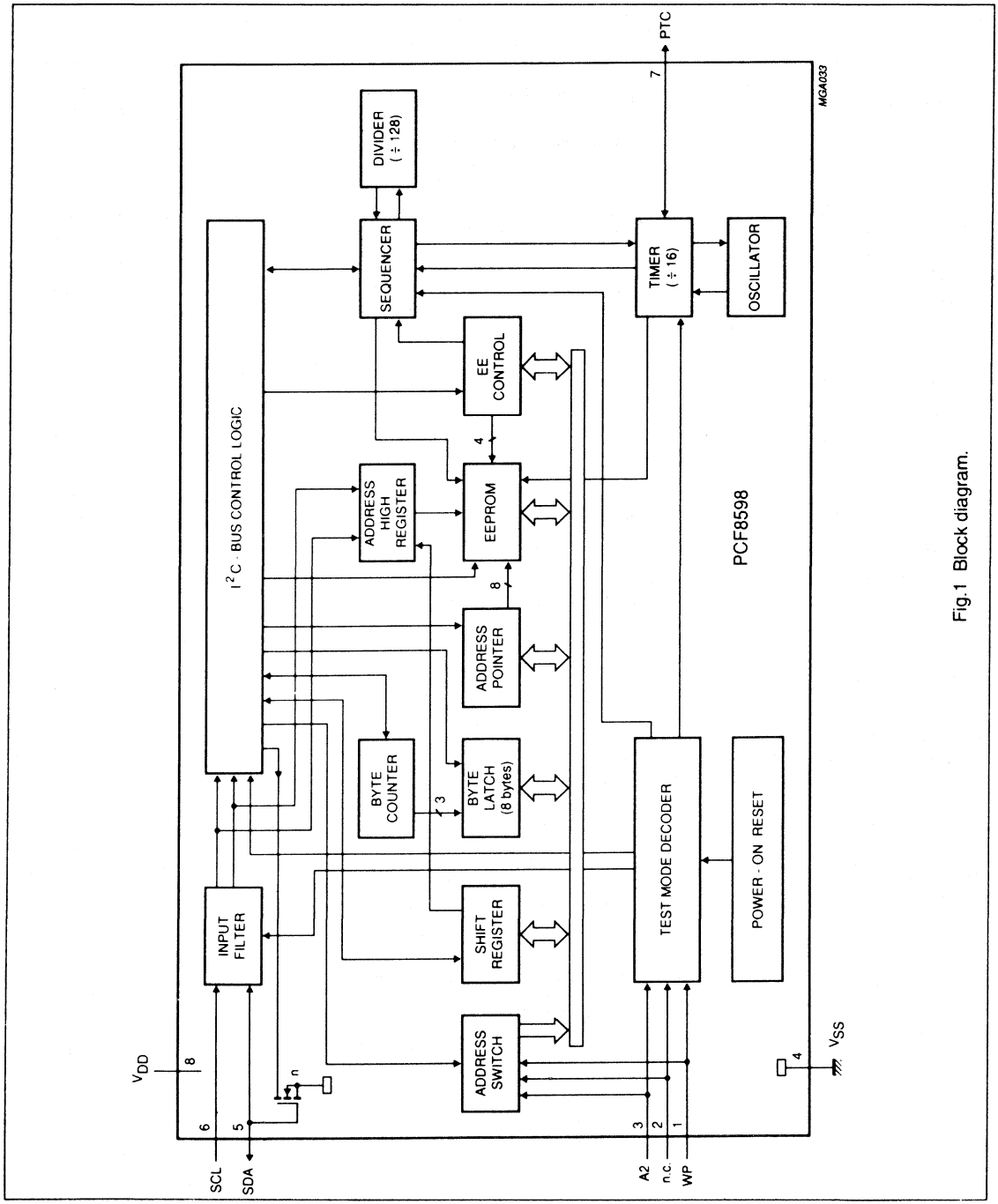


Fig.1 Block diagram.

1024 × 8-bit static CMOS EEPROM with I²C-bus interface

PCF8598

PIN CONFIGURATION

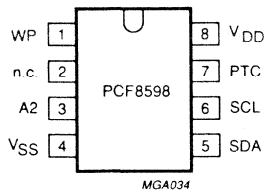


Fig.2 Pin configuration.

PINNING

SYMBOL	PIN	DESCRIPTION
WP	1	write-protect
n.c.	2	not used
A2	3	address input
V_{SS}	4	negative supply voltage
SDA	5	serial data line I²C-bus
SCL	6	serial clock line I²C-bus
PTC	7	programming time control
V_{DD}	8	positive supply voltage

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage		−0.3	+7.0	V
V_I	voltage on any input pin	$\|Z_I\| > 500\ \Omega$	V_{SS} −0.8	V_{DD} +0.8	V
I_I	current on any input pin		-	1	mA
I_O	output current		-	10	mA
T_{stg}	storage temperature range		−65	+150	°C
T_{amb}	operating ambient temperature range		−40	+85	°C

CHARACTERISTICS

V_{DD} = 2.5 to 6 V; V_{SS} = 0 V; T_{amb} = –40 to +85 °C; unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DD}	supply voltage		2.5	-	6.0	V
I_{DDR}	supply current READ	f_{SCL} = 100 kHz				
		V_{DD} = 3 V	-	-	0.1	mA
		V_{DD} = 6 V	-	-	0.4	mA
I_{DDW}	supply current ERASE/WRITE	f_{SCL} = 100 kHz				
		V_{DD} = 3 V	-	-	0.35	mA
		V_{DD} = 6 V	-	-	2.5	mA
I_{DDO}	supply current STANDBY					
		V_{DD} = 3 V	-	-	3.5	µA
		V_{DD} = 6 V	-	-	10	µA
PTC input						
V_{IL}	input voltage LOW		–0.8	-	0.1 V_{DD}	V
V_{IH}	input voltage HIGH		0.9 V_{DD}	-	V_{DD} +0.8	V
SCL input						
V_{IL}	input voltage LOW		–0.8	-	0.3 V_{DD}	V
V_{IH}	input voltage HIGH		0.7 V_{DD}	-	V_{DD} +0.8	V
I_{LI}	input leakage current	V_I = V_{DD} or V_{SS}	-	-	1	µA
f_{SCL}	clock frequency		0	-	100	kHz
C_I	input capacitance	V_I = V_{SS}	-	-	7	pF
SDA input/output						
V_{IL}	input voltage LOW		–0.8	-	0.3 V_{DD}	V
V_{IH}	input voltage HIGH		0.7 V_{DD}	-	V_{DD} +0.8	V
V_{OL}	output voltage LOW	I_{OH} = 3 mA; V_{DD} = 2.5 V	-	-	0.4	V
I_{LO}	output leakage current	V_{OH} = V_{DD}	-	-	1	µA
C_I	input capacitance	V_I = V_{SS}	-	-	7	pF
Data retention time						
t_S	data retention time	T_{amb} = 55 °C	10	-	-	yrs

WRITE CYCLE LIMITS

The power-on reset circuit resets the I²C-bus logic with a set-up time ≤ 10 µs. Selection of the chip address is achieved by connecting the A1 and A2 inputs to either V_{SS} or V_{DD}.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Endurance						
$N_{E/W}$	ERASE/WRITE cycles per byte	T_{amb} = 85 °C; $t_{E/W}$ = 5 to 25 ms	-	-	100 000	
Programming						
t_{EW}	ERASE/WRITE cycle time	internal oscillator external clock	5	10	25	ms
f_p	programming frequency		10	-	50	kHz
t_{LOW}	LOW time		5	-	-	µs
t_{HIGH}	HIGH time		5	-	-	µs
t_r	rise time		-	-	300	ns
t_f	fall time		-	-	300	ns
t_d	delay time		0	-	t_{LOW}	µs

1024 × 8-bit static CMOS EEPROM with I²C-bus interface

I²C-bus PROTOCOL

The I²C-bus is for 2-way, 2-line communication between different ICs or modules. The serial bus consists of two bidirectional lines: one for data signals (SDA), and one for clock signals (SCL).
Both the SDA and SCL lines must be connected to a positive supply voltage via a pull-up resistor.

The following protocol has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as control signals.

The following bus conditions have been defined:

Bus not busy: both data and clock lines remain HIGH.

Start data transfer: a change in the state of the data line, from HIGH-to-LOW, while the clock is HIGH, defines the start condition.

Stop data transfer: a change in the state of the data line, from LOW-to-HIGH, while the clock is HIGH, defines the stop condition.

Data valid: the state of the data line represents valid data when, after a start condition, the data line is stable for the duration of the HIGH period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a start condition and terminated with a stop condition; the number of the data bytes,
transferred between the start and stop conditions is limited to seven bytes in the ERASE/WRITE mode and eight bytes in the PAGE ERASE/WRITE mode. Data transfer is unlimited in the READ mode. The information is transmitted in bytes and each receiver acknowledges with a ninth bit.

Within the I²C-bus specifications a low-speed mode (2 kHz clock rate) and a high speed mode (100 kHz clock rate) are defined.
The PCF8598 operates in both modes.

By definition a device that sends a signal is called a "transmitter", and the device which receives the signal is called a "receiver". The device which controls the signal is called the "master". The devices that are controlled by the master are called "slaves".

Each byte is followed by one acknowledge bit. This acknowledge bit is a HIGH level, put on the bus by the transmitter. The master generates an extra acknowledge related clock pulse. The slave receiver which is addressed is obliged to generate an acknowledge after the reception of each byte.

The master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.

The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse.

Set-up and hold times must be taken into account. A master receiver must signal an end of data to the slave transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master generation of the stop condition.

DEVICE ADDRESSING

Following a start condition the bus master must output the address of the slave it is accessing. The most significant four bits of the slave address are the device type identifier (see Fig.3). For the PCF8598 this is fixed as 1010.

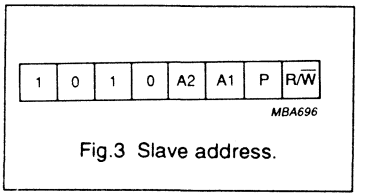


Fig.3 Slave address.

The next significant bit (A2) addresses a particular device.
A system could have up to two PCF8598 devices on the bus.
The two addresses are defined by the state of the A2 input.

The next two significant bits of the slave address field are the page selection bits. It is used by the host to select one out of four pages (page = 256 bytes of memory) These are, in effect, the two most significant bits of the word address.

The last bit of the slave address defines the operation to be performed. When set to logic 1 a read operation is selected.

WRITE OPERATIONS

Byte/word write

For a write operation the PCF8598 requires a second address field. This address field is a word address providing access to any one of the 256 words of memory. Upon receipt of the word address the PCF8598 responds with an acknowledge and awaits the next eight bits of data, again responding with an acknowledge. Word address is automatically incremented. The master can now terminate the transfer by generating a stop condition or transmit up to six more bytes of data and then terminate by generating a stop condition.

After this stop condition the ERASE/WRITE cycle starts and the bus is free for another transmission. Its duration is 10 ms per byte. During the ERASE WRITE cycle the slave receiver does not send an acknowledge bit if addressed via the I²C-bus.

PAGE WRITE

The PCF8598 is capable of an eight-byte page write operation. It is initiated in the same manner as the byte write operation. The master can transmit eight data bytes within one transmission.
After receipt of each byte the PCF8598 will respond with an acknowledge.

After the receipt of each data byte the three low order bits of the word address are internally incremented. The high order five bits of the address remain unchanged. If the master transmits more than eight bytes prior to generating the stop condition, no acknowledge will be given on the ninth (and following) data bytes and the whole transmission will be ignored. As in the byte write operation, all inputs are disabled until completion of the internal write cycles. The typical duration of a page write is 45 ms.

Note:

A write to the EEPROM is always performed if the pin WP is LOW. If WP is HIGH, then the upper half of the EEPROM is write-protected and no acknowledge will be given by the PCF8598 when one of the upper 512 EEPROM cells is addressed. However, an acknowledge will be given after the slave address and the word address.

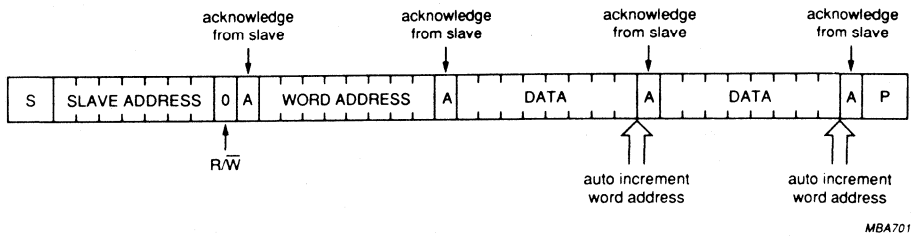


Fig.4 Auto increment memory word address; two byte write.

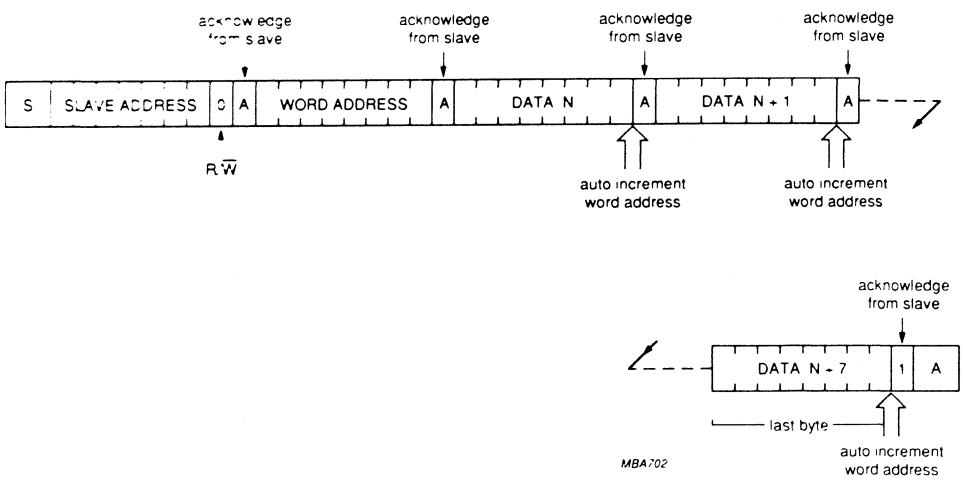


Fig.5 Page write operation; eight byte.

READ OPERATIONS

Read operations are initiated in the same manner as write operations with the exception that the LSB of the slave address is set to logic 1. There are three basic read operations; current address read, random read and sequential read.

Note:

The lower 8 bits of the word address are incremented after each transmission of a data byte (read or write). The two MSBs of the word address, which are defined in the slave address, are not changed when the word address count overflows. Thus, the word address overflows from 255 to 0, from 511 to 256, from 767 to 512 and from 1023 to 768.

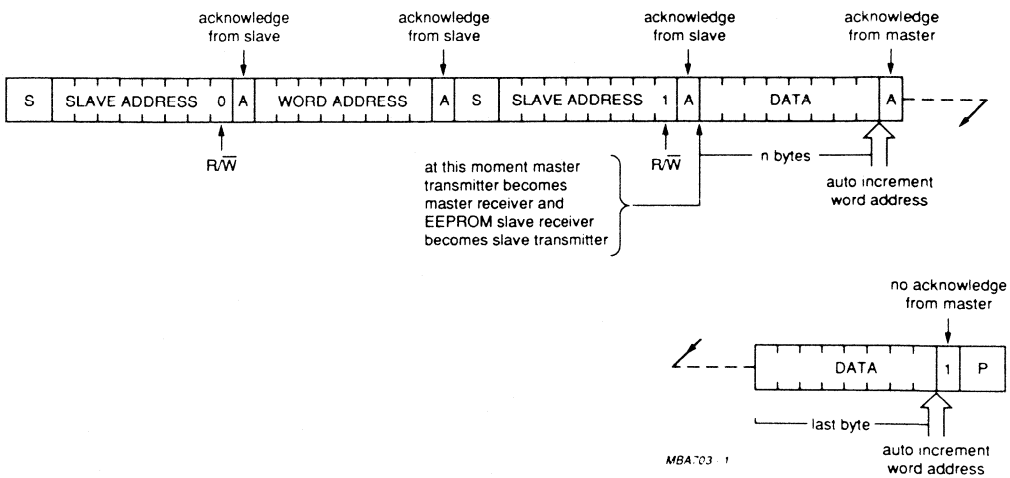


Fig.6 Master reads PCF8598 slave after setting word address; (WRITE word address; READ data).

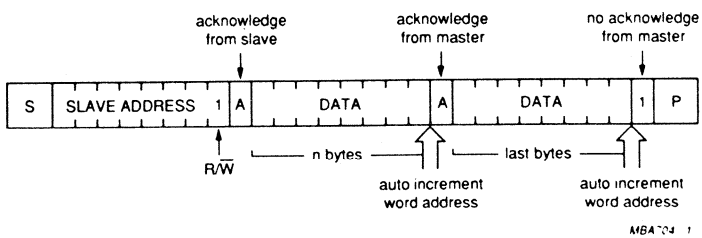


Fig.7 Master reads PCF8598 immediately after first byte (READ mode).

I²C-bus TIMING

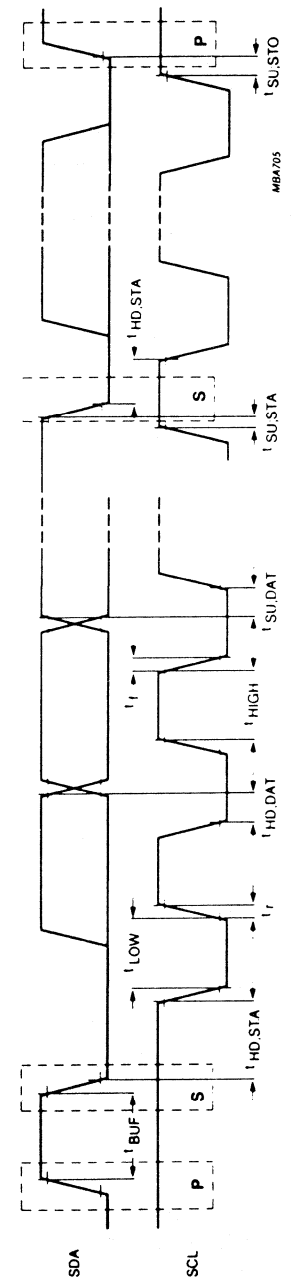


Fig.8 Timing requirements for the I²C-bus.

I²C-bus CHARACTERISTICS

(note 1)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
f_{SCL}	clock frequency		0	-	100	kHz
t_{BUF}	time the bus must be free before a new transmission can start		4.7	-	-	µs
$t_{HD;STA}$	start condition hold time after which first clock pulse is generated		4.0	-	-	µs
t_{LOW}	clock period LOW		4.7	-	-	µs
t_{HIGH}	clock period HIGH		4.0	-	-	µs
$t_{SU;STA}$	set-up time for start condition	repeated start	4.7	-	-	µs
$t_{HD;DAT}$	data hold time for bus compatible masters		5	-	-	µs
$t_{HD;DAT}$	data hold time for bus devices	note 2	0	-	-	ns
$t_{SU;DAT}$	data set-up time		250	-	-	ns
t_r	SDA and SCL rise time		-	-	1	µs
t_f	SDA and SCL fall time		-	-	300	ns
$t_{SU;STO}$	set-up time for stop condition		4.7	-	-	µs

Notes

1. All the timing values are valid within the operating supply voltage and ambient temperature range and refer to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.
2. The hold time required to bridge the undefined region of the falling edge of SCL must be internally provided by a transmitter. It is not greater than 300 ns.

EXTERNAL CLOCK TIMING

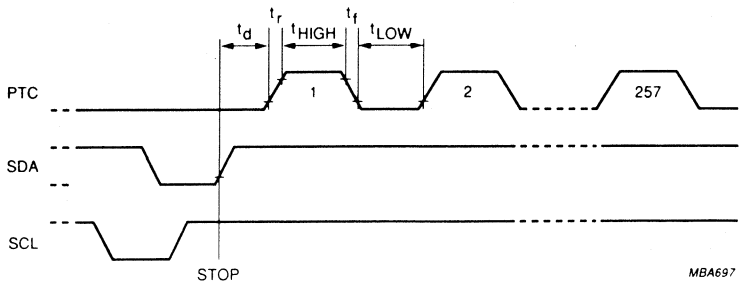


Fig.9 One byte ERASE/WRITE cycle.

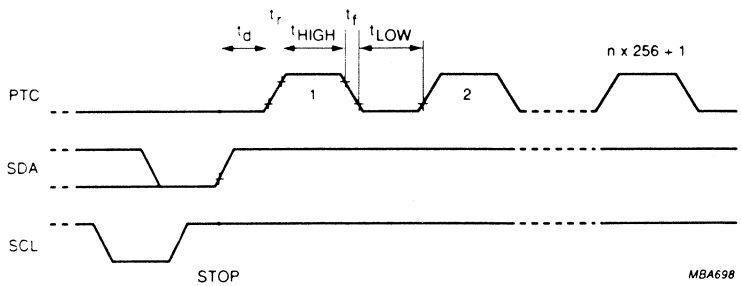


Fig.10 10 n byte ERASE/WRITE cycle (n = 2 to 7).

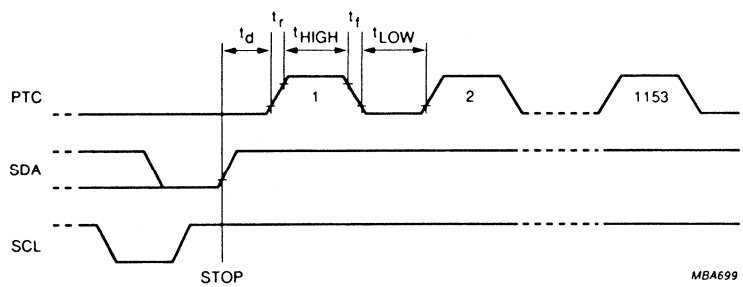
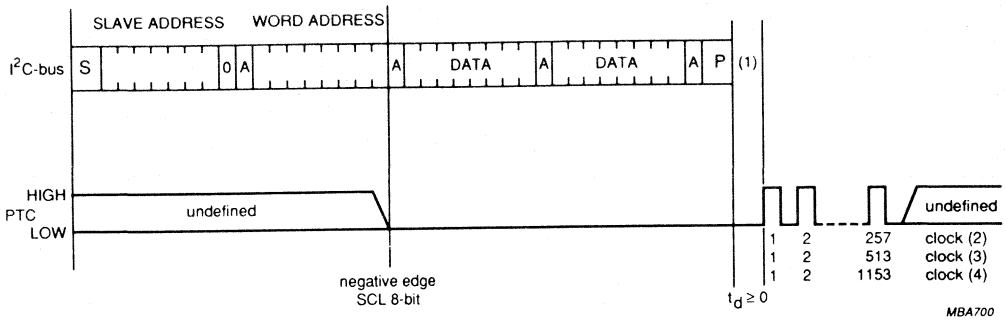


Fig.11 Page mode.



(1) If an external clock is chosen, this information is latched internally by setting pin 7 (PTC) LOW after transmission of the eight bit of the word address (negative edge of SCL). Thus the state of pin 7 may be previously undefined. Leaving pin 7 LOW causes a higher standby current.

(2) 1-byte programming.

(3) 2-byte programming.

(4) One page (8 byte) programming.

Fig.12 External clock.

4-digit LED driver with I²C-bus interface SAA1064

GENERAL DESCRIPTION

The LED-driver is a bipolar integrated circuit made in an I²L compatible 18 volts process. The circuit is especially designed to drive four 7-segment LED displays with decimal point by means of multiplexing between two pairs of digits. It features an I²C-Bus slave transceiver interface with the possibility to program four different SLAVE ADDRESSES, a POWER RESET flag, 16 current sink OUTPUTS, controllable by software up to 21 mA, two multiplex drive outputs for common anode segments, an on-chip multiplex oscillator, control bits to select static, dynamic and blank mode, and one bit for segment test.

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage	V_{EE} = 0 V	V_{CC}	4.5	5	15	V
Supply current all outputs OFF	V_{CC} = 5 V	I_{CC}*	7	9.5	14	mA
Total power dissipation						
24-lead DIL (SOT101B)		P_{tot}	–	–	1000	mW
24-lead DIL SO (SOT137A)		P_{tot}	–	–	500	mW
Operating ambient temperature range		T_{amb}	−40	–	+85	°C

* The positive current is defined as the conventional current flow into a device (sink current).

PACKAGE OUTLINE

SAA1064: 24-lead DIL; plastic with internal heat spreader (SOT101B).
SAA1064T: 24-lead mini-pack; plastic (SO-24; SOT137A).

4-digit LED driver with I²C-bus interface SAA1064

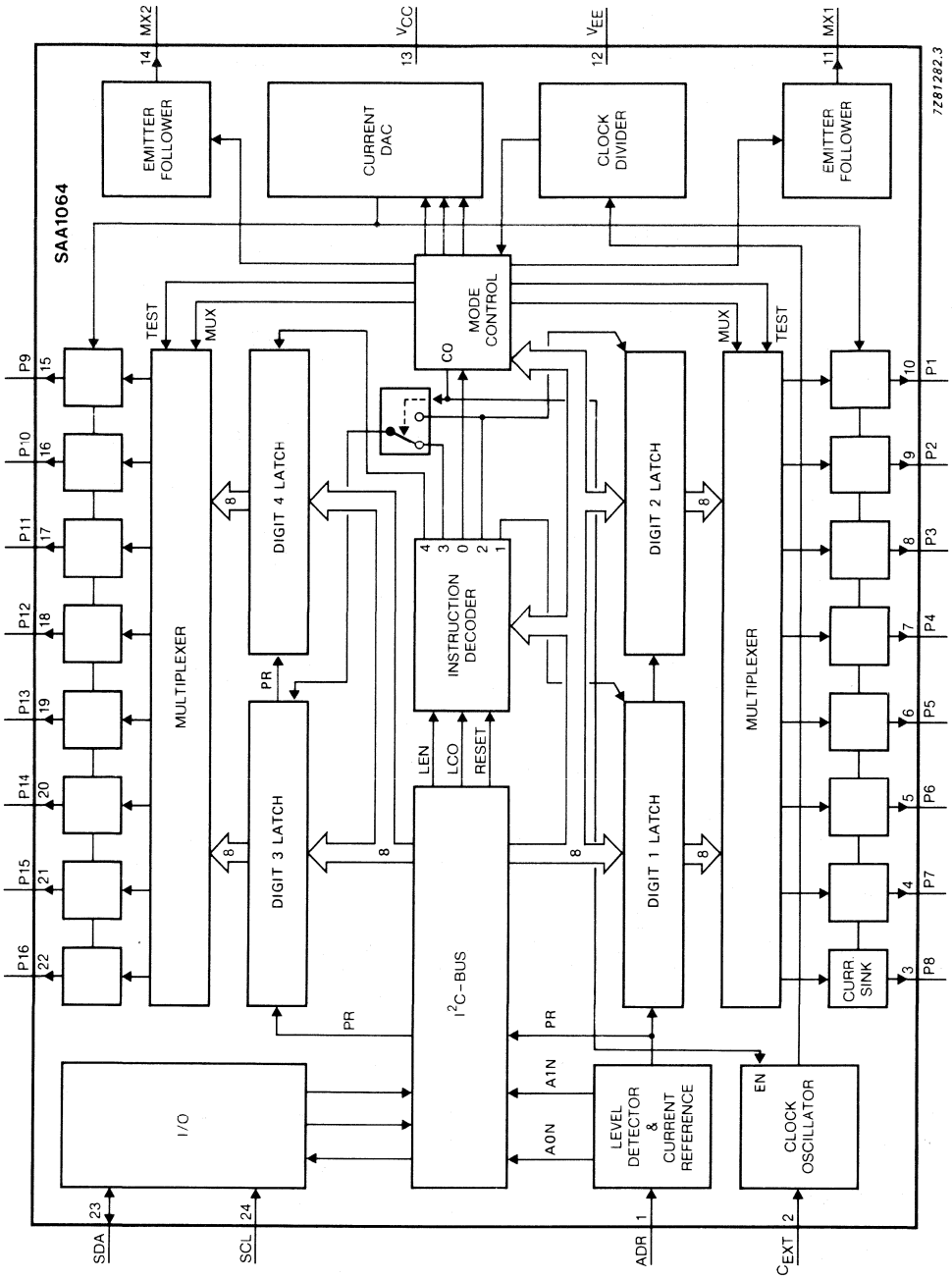


Fig.1 Block diagram.

4-digit LED driver with I²C-bus interface | SAA1064

PINNING

SYMBOL	PIN	DESCRIPTION
ADR	1	I²C-Bus slave address input
C_{EXT}	2	external control
P8 to P1	3-10	segment output
MX1	11	multiplex output
V_{EE}	12	ground
V_{CC}	13	positive supply
MX2	14	multiplex output
P9 to P16	15-22	segment output
SDA	23	I²C-Bus serial data line
SCL	24	I²C-Bus serial clock line

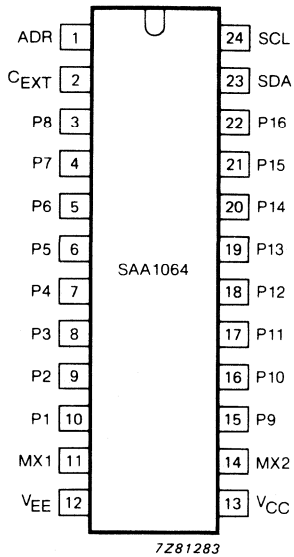
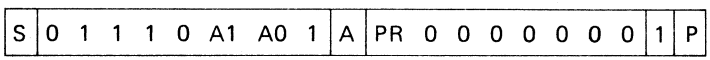


Fig.2 Pinning diagram.

FUNCTIONAL DESCRIPTION



slave address | status byte

Fig. 3a I²C-Bus format; READ mode.

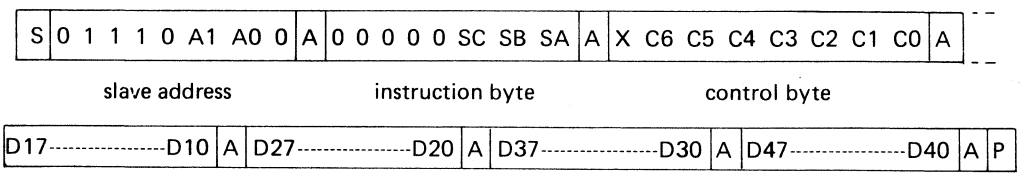


Fig. 3b I²C-Bus format; WRITE mode.

S = start condition
P = stop condition
A = acknowledge
X = don't care

A1, A0 = programmable address bits
SC SB SA = subaddress bits
C6 to C0 = control bits
PR = POWER RESET flag

Address pin ADR

Four different slave addresses can be chosen by connecting ADR either to V_{EE}, 3/8 V_{CC}, 5/8 V_{CC} or V_{CC}. This results in the corresponding valid addresses HEX 70, 72, 74 and 76 for writing and 71, 73, 75 and 77 for reading. All other addresses cannot be acknowledged by the circuit.

Status byte

Only one bit is present in the status byte, the POWER RESET flag. A logic 1 indicates the occurence of a power failure since the last time it was read out. After completion of the READ action this flag will be set to logic 0.

Subaddressing

The bits SC, SB and SA form a pointer and determine to which register the data byte following the instruction byte will be written. All other bytes will then be stored in the registers with consecutive subaddresses. This feature is called Auto-Increment (AI) of the subaddress and enables a quick initialization by the master.
The subaddress pointer will wrap around from 7 to 0.
The subaddresses are given as follows:

SC	SB	SA	sub-address	function
0	0	0	00	control register
0	0	1	01	digit 1
0	1	0	02	digit 2
0	1	1	03	digit 3
1	0	0	04	digit 4
1	0	1	05	reserved, not used
1	1	0	06	
1	1	1	07	

Control bits (see Fig. 4)

The control bits C0 to C6 have the following meaning:

C0 = 0 static mode, i.e. continuous display of digits 1 and 2
C0 = 1 dynamic mode, i.e. alternating display of digit 1 + 3 and 2 + 4
C1 = 0/1 digits 1 + 3 are blanked/not blanked
C2 = 0/1 digits 2 + 4 are blanked/not blanked
C3 = 1 all segment outputs are switched-on for segment test*
C4 = 1 adds 3 mA to segment output current
C5 = 1 adds 6 mA to segment output current
C6 = 1 adds 12 mA to segment output current

Data

A segment is switched ON if the corresponding data bit is logic 1. Data bits D17 to D10 correspond with digit 1, D27 to D20 with digit 2, D37 to D30 with digit 3 and D47 to D40 with digit 4.
The MSBs correspond with outputs P8 and P16, the LSBs with P1 and P9. Digit numbers 1 to 4 are equal to their subaddresses (hex) 1 to 4.

* At a current determined by C4, C5 and C6.

SDA, SCL

The SDA and SCL I/O meet the I²C-Bus specification. For protection against positive voltage pulses on these inputs voltage regulator diodes are connected to V_{EE}. This means that normal line voltage should not exceed 5,5 volt. Data will be latched on the positive-going edge of the acknowledge related clock pulse.

Power-on reset

The power-on reset signal is generated internally and sets all bits to zero, resulting in a completely blanked display. Only the POWER RESET flag is set.

External Control (C_{EXT})

With a capacitor connected to pin 2 the multiplex frequency can be set (see Fig. 5). When static this pin can be connected to V_{EE} or V_{CC} or left floating since the oscillator will be switched off.

Segment outputs

The segment outputs P1 to P16 are controllable current-sink sources. They are switched on by the corresponding data bits and their current is adjusted by control bits C4, C5 and C6.

Multiplex outputs

The multiplex outputs MX1 and MX2 are switched alternately in dynamic mode with a frequency derived from the clock-oscillator. In static mode MX1 is switched on. The outputs consist of an emitter-follower, which can be used to drive the common anodes of two displays directly provided that the total power dissipation of the circuit is not exceeded. If this occurs external transistors should be connected to pins 11 and 14 as shown in Fig. 5.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage (pin 13)	V_{EE} = 0 V	V_{CC}	−0.5	18	V
Supply current (pin 13)		I_{CC}	−50	200	mA
Total power dissipation					
24-lead DIL (SOT101B)		P_{tot}		1000	mW
24-lead SO (SO137A)		P_{tot}		500	mW
SDA, SCL voltages	V_{EE} = 0 V	$V_{23,24}$	−0.5	5.9	V
Voltages ADR-MX1 and MX2-P16	V_{EE} = 0 V	$V_{1\text{-}11}$, $V_{14\text{-}22}$	−0.5	V_{CC} + 0.5	V
Input/output current all pins	outputs OFF	$\pm I_{I/O}$	−	10	mA
Operating ambient temperature range		T_{amb}	−40	+ 85	°C
Storage temperature range		T_{stg}	−55	+ 150	°C

THERMAL RESISTANCE

From crystal to ambient

24-lead DIL	$R_{th\ j\text{-}a}$	35 K/W
24-lead SO (on ceramic substrate)	$R_{th\ j\text{-}a}$	75 K/W
24-lead SO (on printed circuit board)	$R_{th\ j\text{-}a}$	105 K/W

CHARACTERISTICS

V_{CC} = 5 V; T_{amb} = 25 °C; voltages are referenced to ground (V_{EE} = 0 V); unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage (pin 13)		V_{CC}	4,5	5,0	15	V
Supply current	all outputs OFF					
	V_{CC} = 5 V	I_{CC}	7,0	9,5	14,0	mA
Power dissipation	all outputs OFF	P_d	–	50	–	mW
SDA; SCL (pins 23 and 24)						
Input voltages		$V_{23,24}$	0	–	5,5	V
Logic input voltage LOW		$V_{IL(L)}$	–	–	1,5	V
Logic input voltage HIGH		$V_{IH(L)}$	3,0	–	–	V
Input current LOW	$V_{23,24} = V_{EE}$	$-I_{IL}$	–	–	10	μA
Input current HIGH	$V_{23,24} = V_{CC}$	I_{IH}	–	–	10	μA
SDA						
Logic output voltage LOW	I_O = 3 mA	$V_{OL(L)}$	–	–	0,4	V
Output sink current		I_{SDA}	3	–	–	mA
Address input (pin 1)						
Input voltage programmable address bits:						
A0 = 0; A1 = 0		V_1	V_{EE}	–	$3/16V_{CC}$	V
A0 = 1; A1 = 0		V_1	$5/16V_{CC}$	$3/8V_{CC}$	$7/16V_{CC}$	V
A0 = 0; A1 = 1		V_1	$9/16V_{CC}$	$5/8V_{CC}$	$11/16V_{CC}$	V
A0 = 1; A1 = 1		V_1	$13/16V_{CC}$	–	V_{CC}	V
Input current LOW	$V_1 = V_{EE}$	$-I_1$	–	–	10	μA
Input current HIGH	$V_1 = V_{CC}$	I_1	–	–	10	μA
External control (C_{EXT}) pin 2						
Switching level input						
Input voltage LOW		V_{IL}	–	–	$V_{CC}-3,3$	V
Input voltage HIGH		V_{IH}	$V_{CC}-1,5$	–	–	V
Input current	V_2 = 2 V	I_2	−140	−160	−180	μA
	V_2 = 4 V	I_2	140	160	180	μA

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Segment outputs (P8 to P1; pins 3 to 10) P9 to P16; pins 15 to 22)						
Output voltages	I_O = 15 mA	V_O	–	–	0.5	V
Output leakage current HIGH	$V_O = V_{CC}$ = 15 V	I_{LO}	–	–	± 10	μA
Output current LOW						
All control bits (C4, C5 and C6) are HIGH	V_{OL} = 5 V	I_{OL}	17.85	21	25.2	mA
Contribution of:						
control bit C4		I_O	2.55	3.0	3.6	mA
control bit C5		I_O	5.1	6.0	7.2	mA
control bit C6		I_O	10.2	12.0	14.4	mA
Relative segment output current accuracy						
with respect to highest value		ΔI_O	–	–	7.5	%
Multiplex 1 and 2 (pins 11 and 14)						
Maximum output voltage (when ON)	$-I_{MPX}$ = 50 mA	V_{MPX}	V_{CC}−1.5	–	–	V
Maximum output current HIGH (when ON)	V_{MPX} = 2 V	$-I_{MPX}$	50	–	110	mA
Maximum output current LOW (when OFF)	V_O = 2 V	$+I_{MPX}$	50	70	110	μA
Multiplex output period	C_{EXT} = 2.7 nF	T_{MPX}	5	–	10	ms
Multiplexed duty factor			–	48.4	–	%

* Value to be fixed.

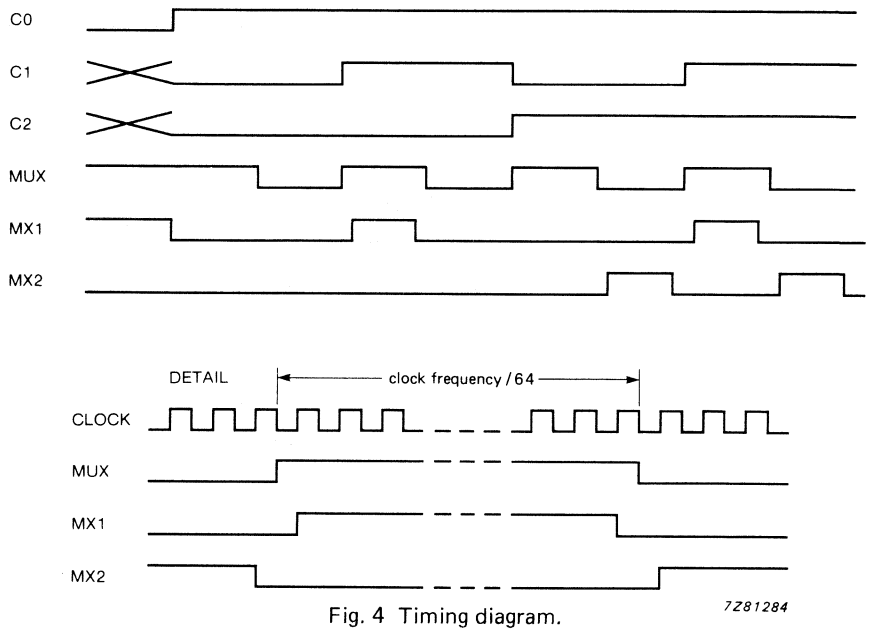


Fig. 4 Timing diagram.

APPLICATION INFORMATION

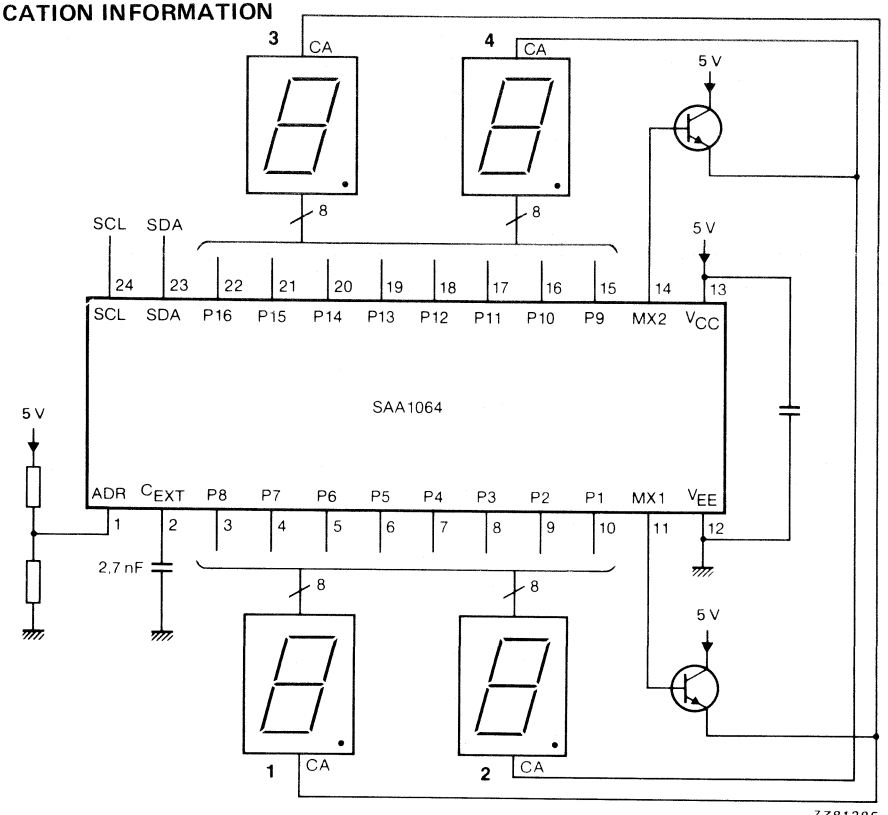


Fig. 5 Dynamic mode application diagram.

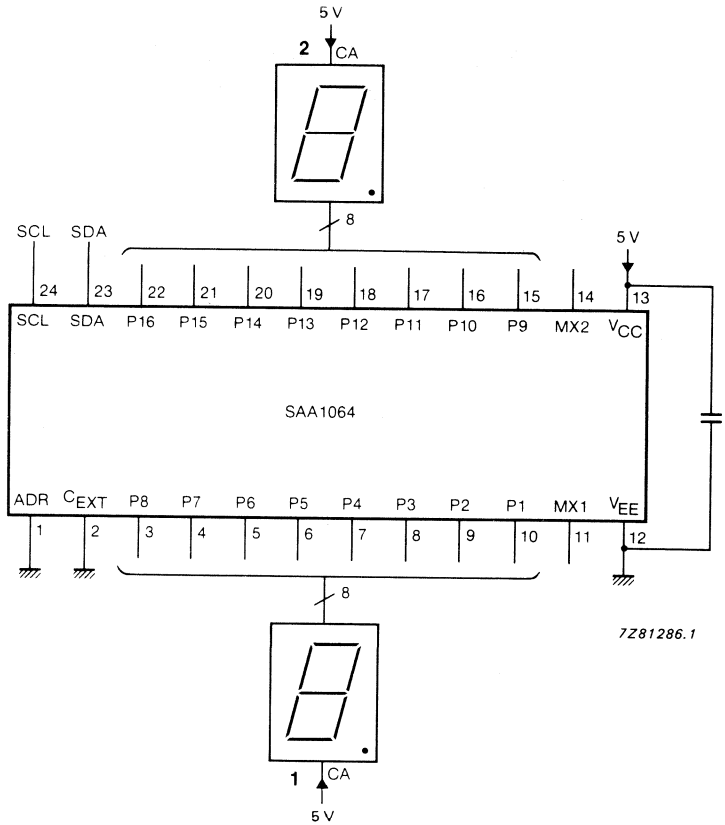


Fig. 6 Static mode application diagram.

POWER DISSIPATION

The total maximum power dissipation of the SAA1064 is made up by the following parts:

1. Maximum dissipation when none of the outputs are programmed (continuous line in Fig.7).
2. Maximum dissipation of each programmed output. The dashed line in Fig.7 visualises the dissipation when **all** the segments are programmed (max. 16 in the static, and max. 32 in the dynamic mode). When less segments are programmed one should take a proportional part of the maximum value.
3. Maximum dissipation of the programmed segment drivers which can be expressed as: $P_{add} = V_O \times I_O \times N$.

Where:
- P_{add} = The additional power dissipation of the segment drivers
- V_O = The low state segment driver output voltage
- I_O = The programmed segment output current
- N = The number of programmed segments in the static mode, or half the number of programmed segment drivers in the dynamic mode.

Under no conditions the total maximum dissipation (500 mW for the SO and 1000 mW for the DIL package) should be exceeded.

Example: V_{CC} = 5 V

V_O = 0.25 V

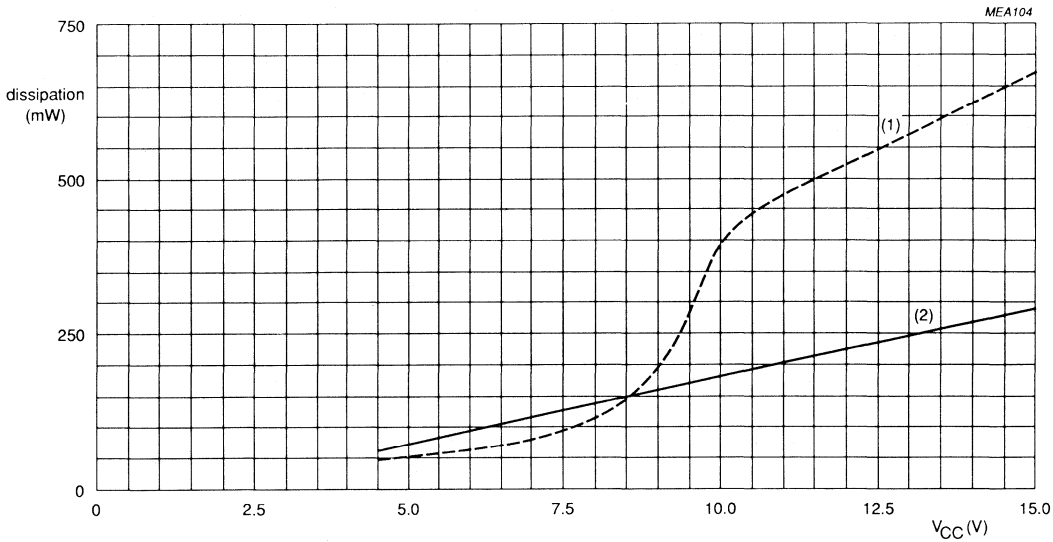
I_O = 12 mA

24 programmed segments in dynamic mode

$P_{tot} = P_1 + P_2 + P_3$

$= 75\ mW + (50 * 24/32)\ mW + (0.25 * 12.10^{-3} * 12)\ mW$

$= 148.5\ mW$



(1) All outputs programmed (no segment current sink).

(2) Outputs not programmed.

Fig.7 SAA1064 power dissipation as a function of supply voltage.

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

Octuple 6-bit DAC with I²C-bus — TDA8444/AT/T

GENERAL DESCRIPTION

The TDA8444 comprises eight digital-to-analogue converters (DACs) each controlled via the two-wire I²C-bus. The DACs are individually programmed using a 6-bit word to select an output from one of 64 voltage steps. The maximum output voltage of all DACs is set by the input V_{max} and the resolution is approximately $V_{max}/64$. At power-on all DAC outputs are set to their lowest value. The I²C-bus slave receiver has a 7-bit address of which 3 bits are programmable via pins A0, A1 and A2.

Features

- Eight discrete DACs
- I²C-bus slave receiver
- 16-pin DIL package

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage		V_P	10.8	12.0	13.2	V
Supply current	no loads; $V_{max} = V_P$; all data = 00	I_{CC}	8	12	15	mA
Total power dissipation	no loads; $V_{max} = V_P$; all data = 00	P_{tot}	–	150	–	mW
Effective range of V_{max} input	V_P = 12 V	V_{max}	1	–	10.5	V
DAC output voltage range		V_O	0.1	–	V_P–0.5	V
Step value of 1 LSB	$V_{max} = V_P$; I_O = –2 mA	V_{LSB}	70	160	250	mV

PACKAGE OUTLINE

16-lead DIL; plastic (SOT38).

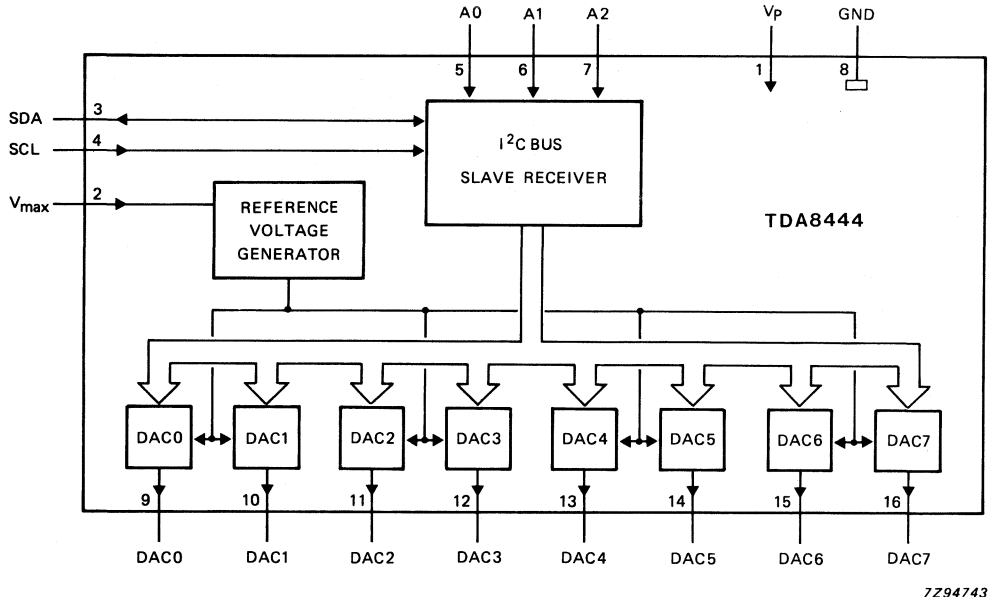


Fig. 1 Block diagram.

PINNING

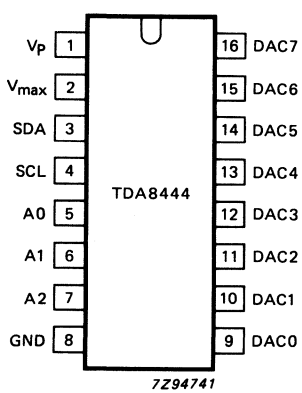
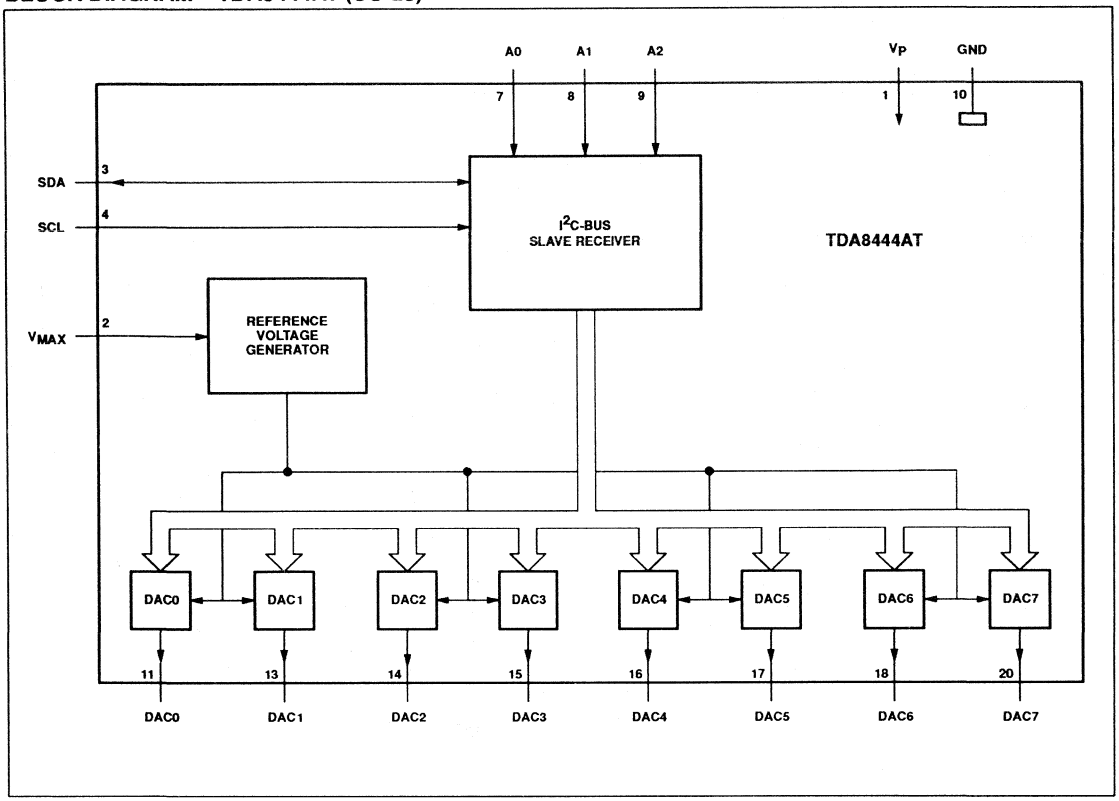


Fig. 2 Pinning diagram.

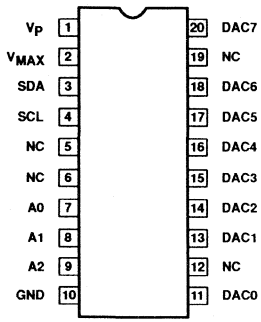
1	V_P	positive supply voltage
2	V_{max}	control input for DAC maximum output voltage
3	SDA	I²C-bus serial data input/output
4	SCL	I²C-bus serial data clock
5	A0	programmable address bits for I²C-bus slave receiver
6	A1	
7	A2	
8	GND	ground
9-16	DAC0-7	analogue voltage outputs

Octuple 6-bit DAC with I²C-bus TDA8444/AT/T

BLOCK DIAGRAM – TDA8444AT (SO-20)



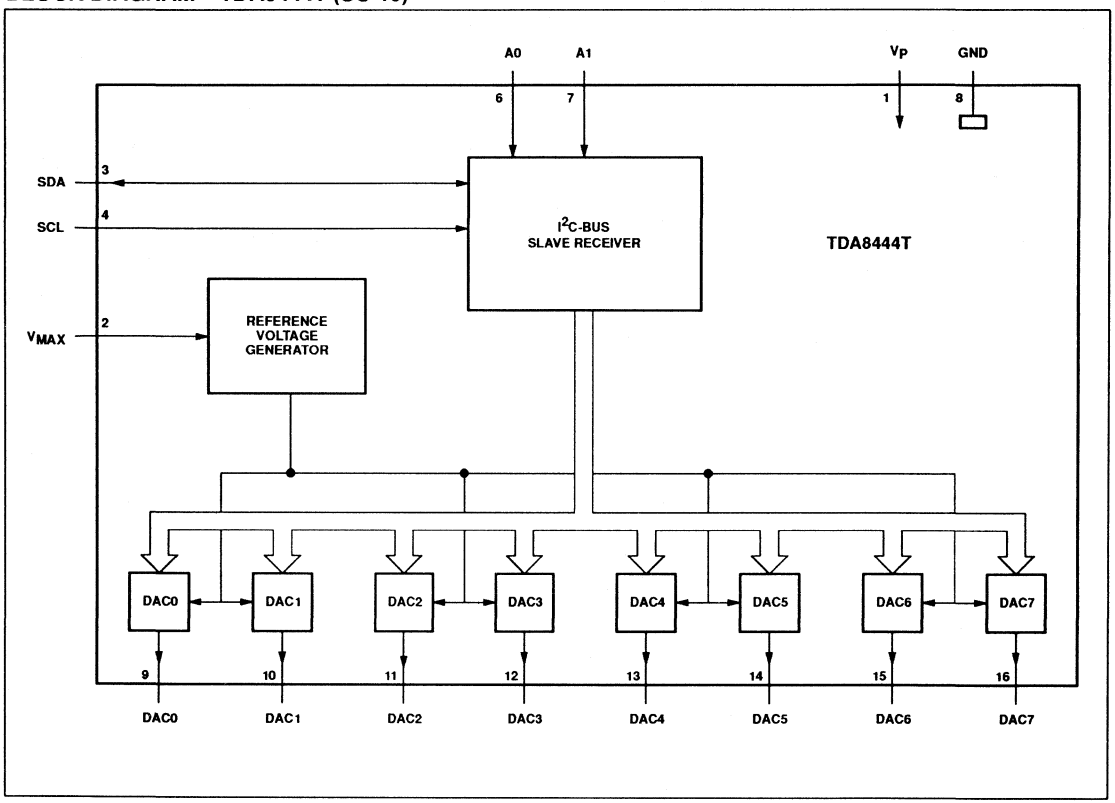
PIN CONFIGURATION AND DESCRIPTION – TDA8444AT (SO-20, SOT-163)



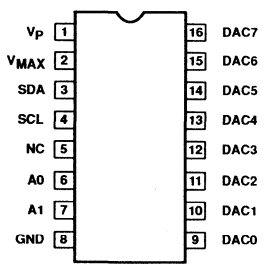
1	V_p	Positive supply voltage
2	V_{MAX}	Control input for DAC maximum output voltage
3	SDA	I²C bus serial data input/output
4	SCL	I²C bus serial data clock
7	A0	Programmable address bits for I²C bus slave receiver
8	A1	Programmable address bits for I²C bus slave receiver
9	A2	Programmable address bits for I²C bus slave receiver
10	GND	Ground
11, 13-18, 20	DAC0-7	Analog voltage outputs

Octuple 6-bit DAC with I²C-bus TDA8444/AT/T

BLOCK DIAGRAM – TDA8444T (SO-16)



PIN CONFIGURATION AND DESCRIPTION – TDA8444T (SO-16, SOT-162)

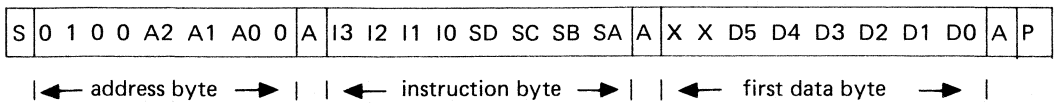


1	V_P	Positive supply voltage
2	V_{MAX}	Control input for DAC maximum output voltage
3	SDA	I²C bus serial data input/output
4	SCL	I²C bus serial data clock
6	A0	Programmable address bits for I²C bus slave receiver
7	A1	Programmable address bits for I²C bus slave receiver
8	GND	Ground
9-16	DAC0-7	Analog voltage outputs

FUNCTIONAL DESCRIPTION

I²C-bus

The TDA8444 I²C-bus interface is a receive-only slave. Data is accepted from the I²C-bus in the following format:



Where:

S = start condition
P = stop condition
A = acknowledge
X = don't care
A2, A1, A0 = programmable address bits
I3, I2, I1, I0 = instruction bits
SD, SC, SB, SA = subaddress bits
D5, D4, D3, D2, D1, D0 = data bits

Fig. 3 Data format.

Address byte

Valid addresses are 40, 42, 44, 46, 48, 4A, 4C, 4E (hexadec), depending on the programming of bits A2, A1 and A0. With these addresses, up to eight TDA8444 ICs can be operated independently from one I²C-bus. No other addresses are acknowledged by the TDA8444.

Instruction and data bytes

Valid instructions are 00 to 0F and F0 to FF (hexadec); the TDA8444 will not respond to other instruction values.

Instructions 00 to 0F cause auto-incrementing of the subaddress (bits SD to SA) when more than one data byte is sent within one transmission. With auto-incrementing, the first data byte is written into the DAC addressed by bits SD to SA and then the subaddress is automatically incremented by one position for the next data byte in the series.

Auto-incrementation does not occur with instructions F0 to FF. Other than auto-incrementation there is no difference between instructions 00 to 0F and F0 to FF. When only one data byte per transmission is present, the DAC addressed by the subaddress will always receive the data.

Valid subaddresses (bits SD to SA) are 0 to 7 (hexadec) relating numerically to DAC0 to DAC7. When the auto-incrementing function is used, the subaddress will sequence through all possible values (0 to F, 0 to F, etc.).

I²C-bus

Input SCL (pin 3) and input/output SDA (pin 4) conform to I²C-bus specifications.* Pins 3 and 4 are protected against positive voltage pulses by internal zener diodes connected to the ground plane and therefore the normal bus line voltage should not exceed 5.5 V.

The address inputs A0, A1, A2 are programmed by a connection to GND for An = 0 or to V_P for An = 1. If the inputs are left floating, An = 1 will result.

FUNCTIONAL DESCRIPTION (continued)

Input V_{max}

Input V_{max} (pin 2) provides a means of compressing the output voltage swing of the DACs. The maximum DAC output voltage is restricted to approximately V_{max} while the 6-bit resolution is maintained, so giving a finer voltage resolution of smaller output swings.

Digital-to-analogue converters

Each DAC comprises a 6-bit data latch, current switches and an output driver. Current sources with values weighted by 2^0 up to 2^5 are switched according to the data input so that the sum of the selected currents gives the required analogue voltage from the output driver. The range of the output voltage is approximately 0.5 to 10.5 V when $V_{max} = V_P$.

The DAC outputs are protected against short-circuits to V_P and GND.

To avoid the possibility of oscillations, capacitive loading at the DAC outputs should not exceed 2 nF.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage		$V_P = V_1$	−0.5	18	V
Supply current (source)		$I_p = I_1$	–	−10	mA
		$I_P = I_I$	–	40	mA
I²C-bus line voltage		$V_{3,4}$	−0.5	5.9	V
Input voltage		V_I	−0.5	V_P + 0.5	V
Output voltage		V_O	−0.5	V_P + 0.5	V
Maximum current on any pin (except pins 1 and 8)		$\pm I_{max}$	–	10	mA
Total power dissipation		P_{tot}	–	500	mW
Operating ambient temperature range		T_{amb}	−20	+ 70	°C
Storage temperature range		T_{stg}	−65	+ 150	°C

THERMAL RESISTANCE

From junction to ambient $R_{th\ j\text{-}a}$ 75 K/W

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

CHARACTERISTICS

All voltages are with respect to GND; T_{amb} = 25 °C; V_P = 12 V unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage		V_P	10.8	12.0	13.2	V
Voltage level for power-on reset		V_1	1	–	4.8	V
Supply current	no loads; $V_{max} = V_P$; all data = 00	$I_P = I_1$	8	12	15	mA
Total power dissipation	no loads; $V_{max} = V_P$; all data = 00	P_{tot}	–	150	–	mW
Effective range of V_{max} input (pin 2)	V_P = 12 V	$V_{max} = V_2$	1.0	–	10.5	V
Pin 2 current	V_2 = 1 V	I_2	–	–	−10	μA
	$V_2 = V_P$	I_2	–	–	10	μA
SDA, SCL inputs (pins 3 and 4)						
Input voltage range		V_I	0	–	5.5	V
Input voltage LOW		V_{IL}	–	–	1.5	V
Input voltage HIGH		V_{IH}	3.0	–	–	V
Input current LOW	$V_{3;4}$ = 0.3 V	I_{IL}	–	–	−10	μA
Input current HIGH	$V_{3;4}$ = 6 V	I_{IH}	–	–	±10	μA
SDA output (pin 3)						
Output voltage LOW	I_3 = 3 mA	V_{OL}	–	–	0.4	V
Sink current		I_O	3	8	–	mA
Address inputs (pins 5 to 7)						
Input voltage range		V_I	0	–	V_P	V
Input voltage LOW		V_{IL}	–	–	1	V
Input voltage HIGH		V_{IH}	2.1	–	–	V
Input current LOW		I_{IL}	–	−7	−12	μA
Input current HIGH		I_{IH}	–	–	1	μA

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
DAC outputs (pins 9 to 16)						
Output voltage range		V_O	0.1	–	V_P–0.5	V
Minimum output voltage	data = 00; I_O = –2 mA	V_{Omin}	0.1	0.4	0.8	V
Maximum output voltage	data = 3F; I_O = –2 mA					
at $V_{max} = V_P$		V_{Omax}	10	10.5	11.5	V
at $1 < V_{max} < 10.5$ V		V_{Omax}	see note			V
Output sink current	V = V_P; data = 1F	I_O	2	8	15	mA
Output source current	V = 0V; data = 1F	I_O	–2	–	–6	mA
Output impedance	data = 1F; $-2 < I_O < +2$ mA	Z_O	–	4	50	Ω
Step value of 1 LSB	$V_{max} = V_P$; I_O = –2 mA	V_{LSB}	70	160	250	mV
Deviation from linearity	I_O = –2 mA; N ≠ 32		0	–	50	mV
Deviation from linearity	I_O = –2 mA; N = 32		0	–	70	mV

Note to the characteristics

$V_O = 0.95\ V_{max} + V_{Omin}$.

APPLICATION INFORMATION

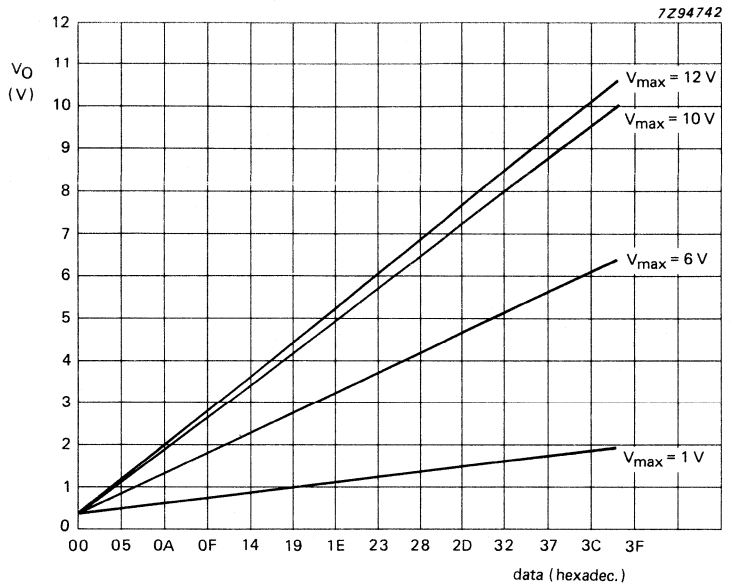


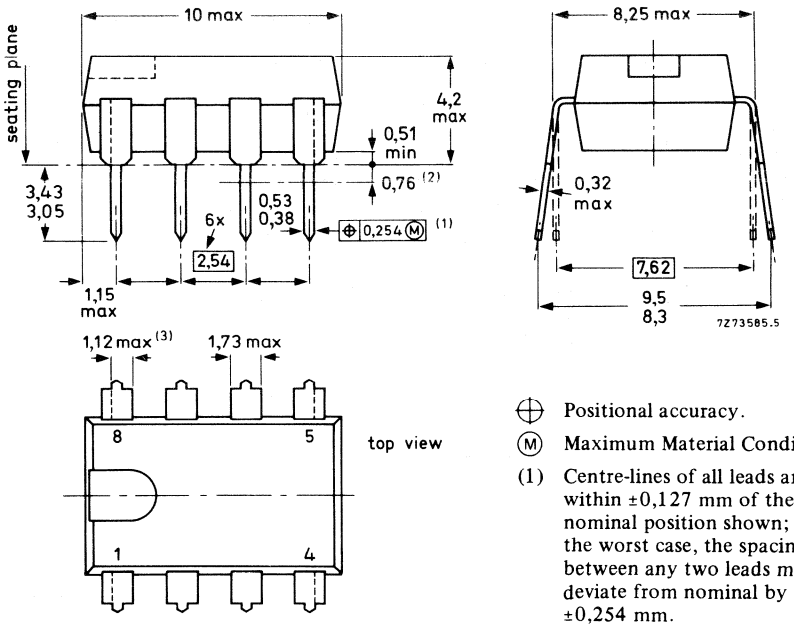
Fig. 4 Graph showing output voltage as a function of the input data value for V_{max} values of 1, 6, 10 and 12 V; V_P = 12 V.

Section 3
Package Outlines

INDEX

Package Outlines

SOT97 8-PIN PLASTIC DUAL IN-LINE (N/P) PACKAGE



⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

(3) Only for devices with asymmetrical end-leads.

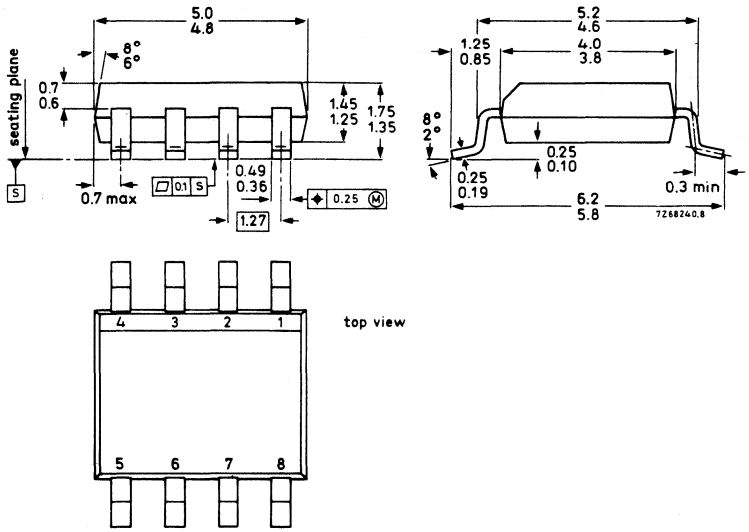
Dimensions in mm

SOT 97

7Z73585.5

Package Outlines

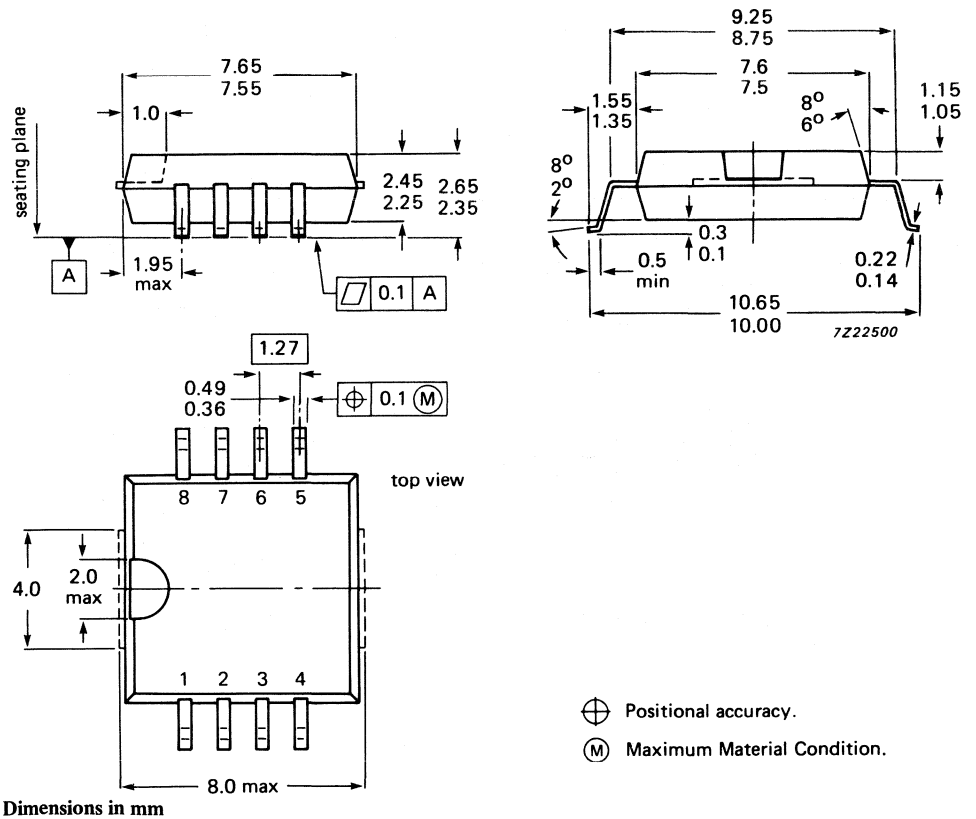
SOT96A 8-PIN PLASTIC SOL (SMALL OUTLINE LARGE) DUAL IN-LINE (D/T) PACKAGE



SOT96A 7Z68240.8

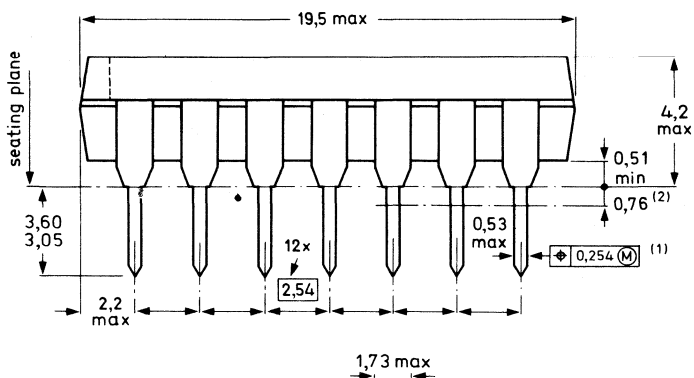
Package Outlines

SOT176C 8-PIN PLASTIC SOL (SMALL OUTLINE LARGE) DUAL IN-LINE (D/T) PACKAGE



Package Outlines

SOT27 14-PIN PLASTIC DUAL IN-LINE (N/P) PACKAGE



Dimensions in mm

⊕ Positional accuracy.

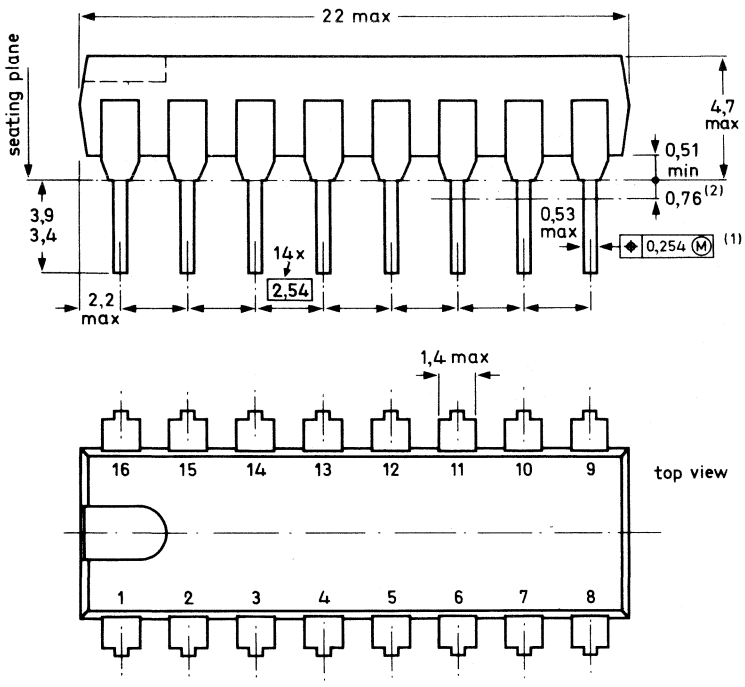
Ⓜ Maximum Material Condition.

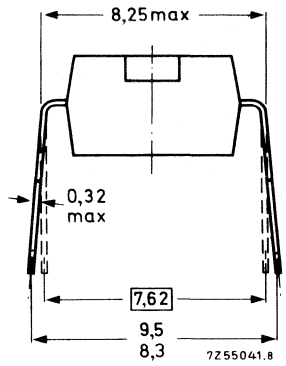
(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Package Outlines

SOT38 16-PIN PLASTIC DUAL IN-LINE (N/P) PACKAGE





(1) Centre-lines of all leads are within ±0.127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0.254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

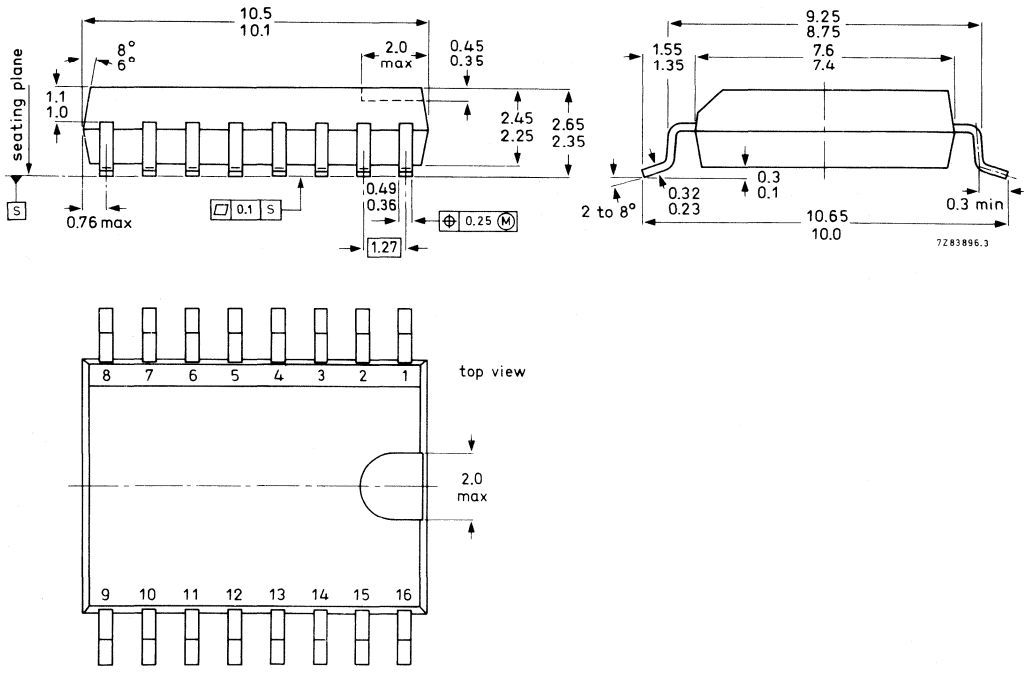
(3) Dimensions in mm.

SOT 38

7Z55041.8

Package Outlines

SOT162A 16-PIN PLASTIC SOL (SMALL OUTLINE LARGE) DUAL IN-LINE (D/T) PACKAGE

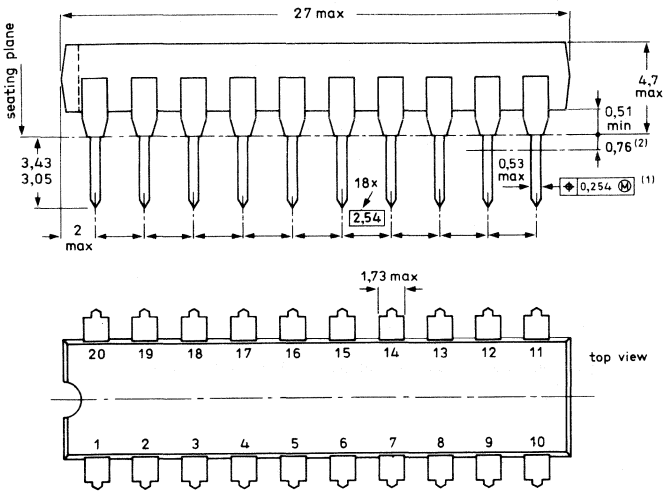


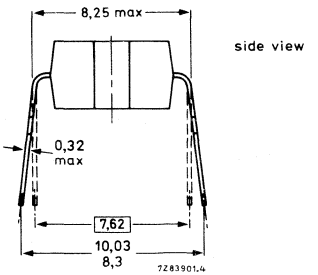
(1) Dimensions in mm.

SOT 162A 7Z83896.3

Package Outlines

SOT146 20-PIN PLASTIC DUAL IN-LINE (N/P) PACKAGE





(1) Centre-lines of all leads are within ±0.127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0.254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

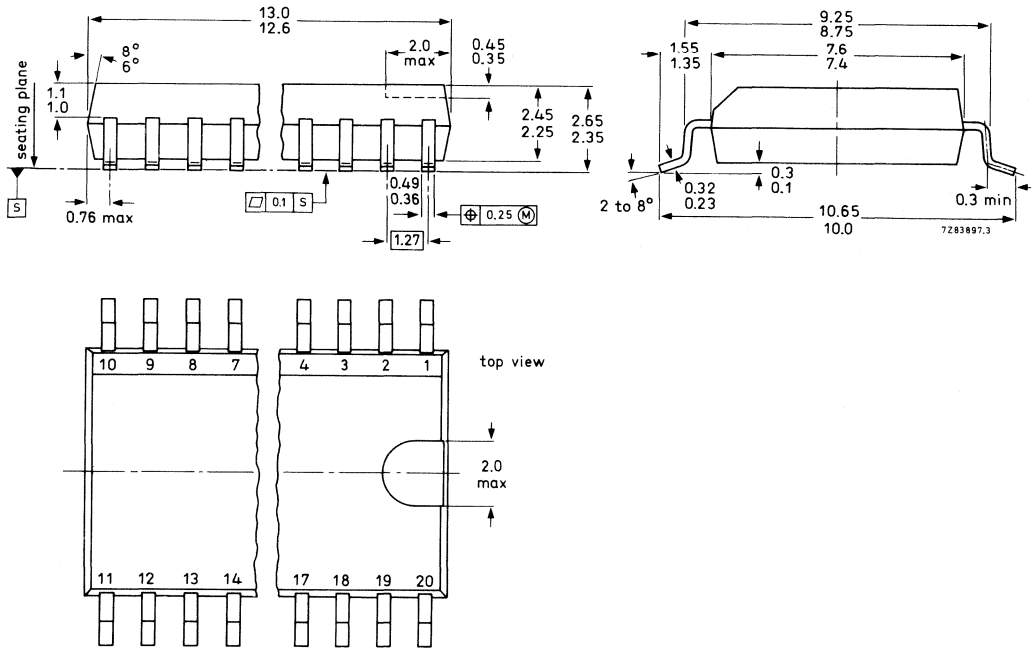
(3) Dimensions in mm.

SOT 146

7Z83901.4

Package Outlines

SOT163A 20-PIN PLASTIC SO (SMALL OUTLINE) DUAL IN-LINE (D/T) PACKAGE



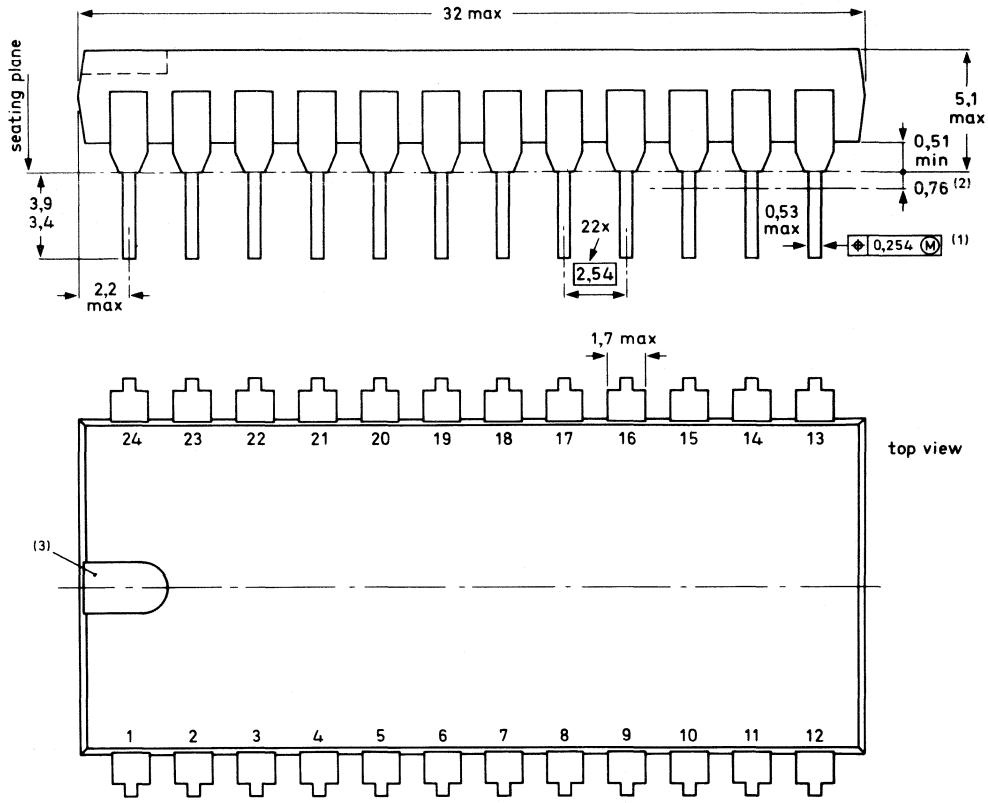
(1) Dimensions in mm.

SOT 163A

7Z83897.3

Package Outlines

SOT101B 24-PIN PLASTIC DUAL IN-LINE (N/P) PACKAGE (W/INTERNAL HEAT SPREADER)



Dimensions in mm

⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

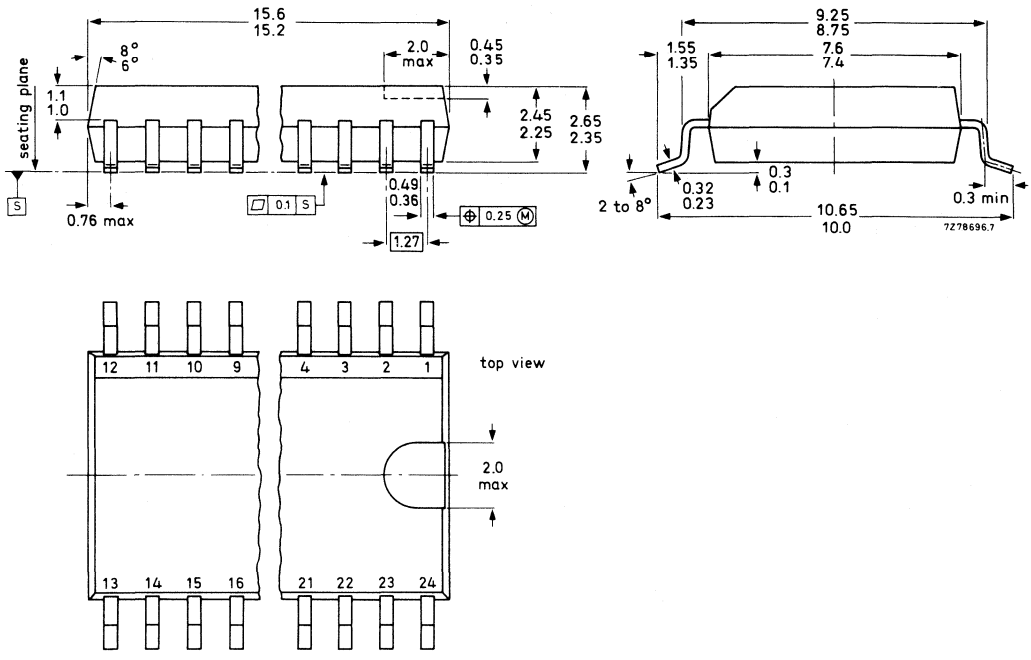
(3) Index may be horizontal as shown, or vertical.

SOT101A, B, F, G, L

7Z73670.5

Package Outlines

SOT137A 24-PIN PLASTIC SO (SMALL OUTLINE) DUAL IN-LINE (D/T) PACKAGE

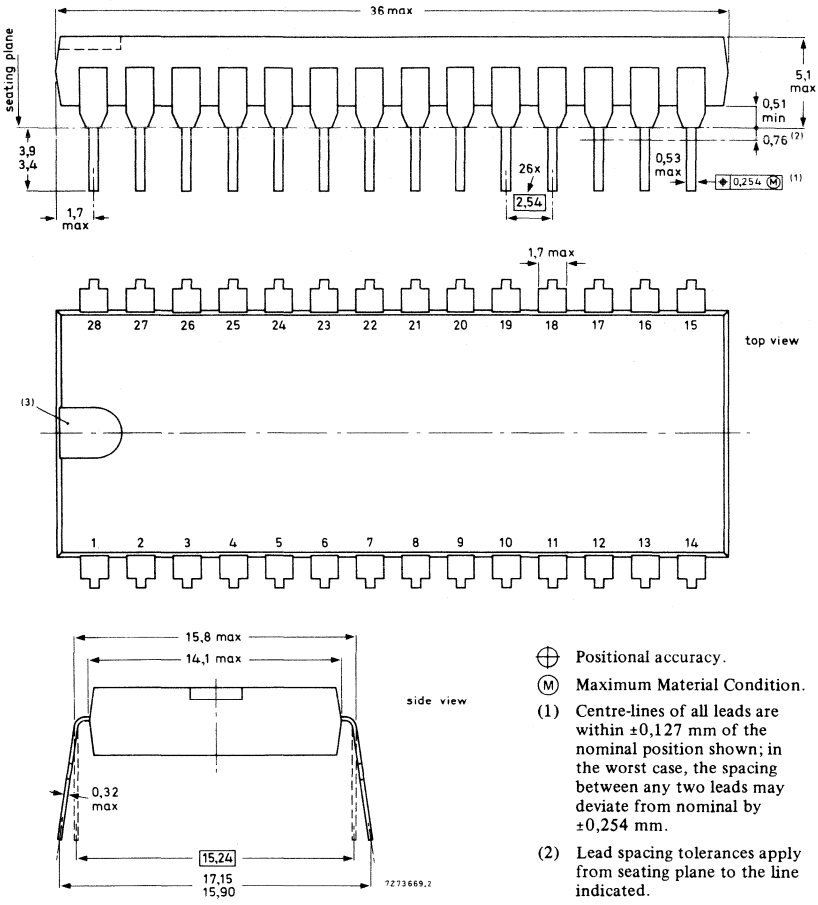


(1) Dimensions in mm.

SOT 137A 7Z78696.7

Package Outlines

SOT117 28-PIN PLASTIC DUAL IN-LINE (N/P) PACKAGE



⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

(3) Index may be horizontal as shown, or vertical.

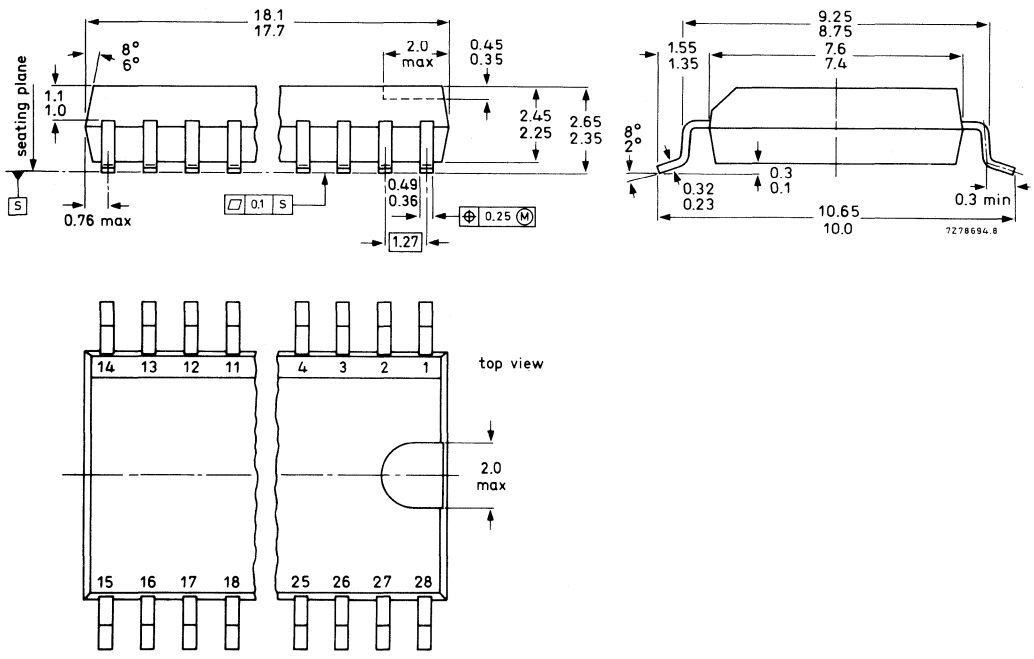
Dimensions in mm

SOT 117

7Z73669.2

Package Outlines

SOT136A 28-PIN PLASTIC SOL (SMALL OUTLINE LARGE) DUAL IN-LINE (D/T) PACKAGE



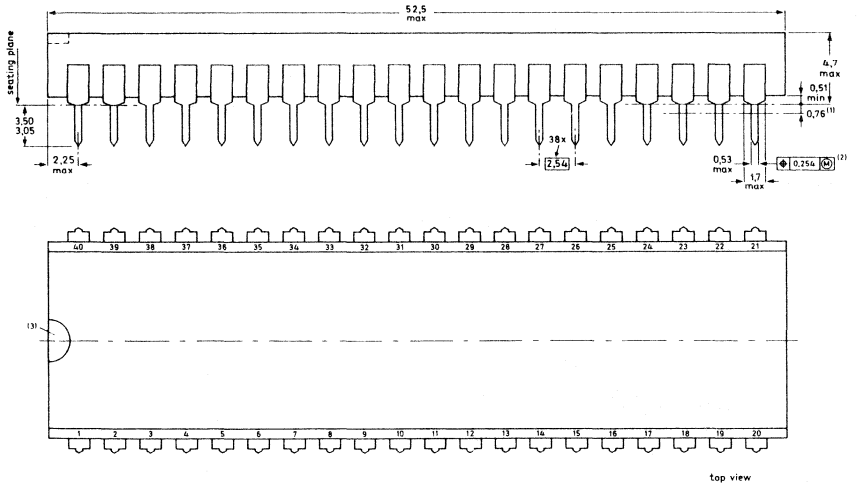
(1) Dimensions in mm.

SOT 136A

7Z78694.8

Package Outlines

SOT129 40-PIN PLASTIC DUAL IN-LINE (N/P) PACKAGE



(1) Centre-lines of all leads are within ±0.127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0.254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

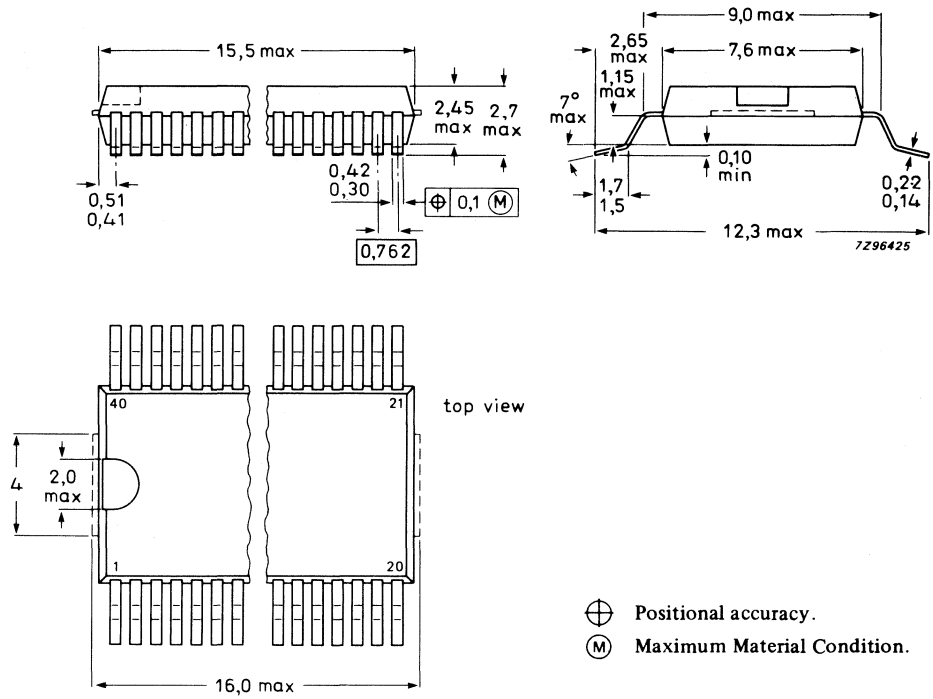
(3) Index may be horizontal as shown, or vertical

(4) Dimensions in mm.

SOT 129 7Z70128.5

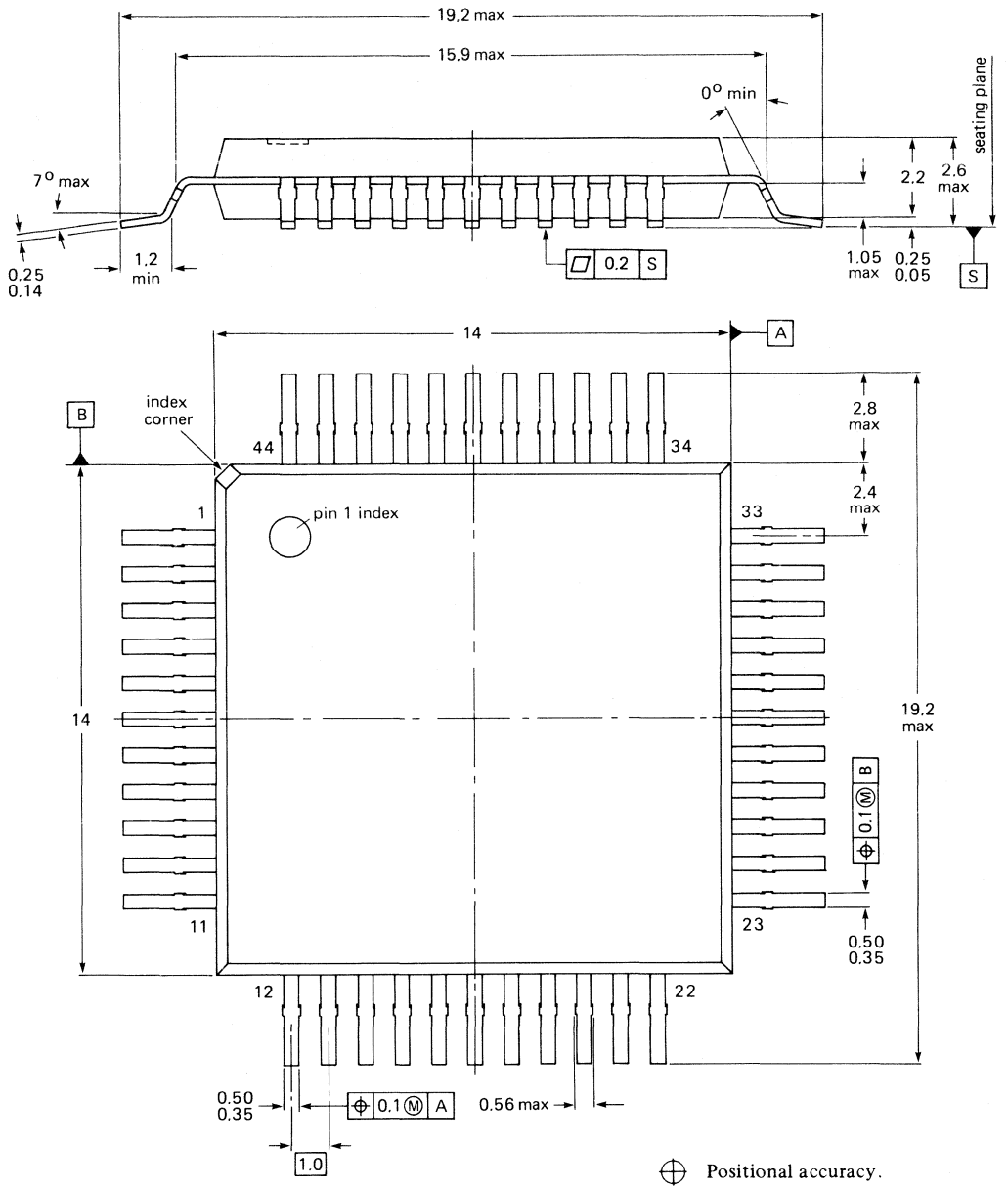
Package Outlines

SOT158A 40-PIN PLASTIC VSO (VERY SMALL OUTLINE) DUAL IN-LINE PACKAGE



Package Outlines

SOT205AG 44-PIN PLASTIC QUAD FLAT PACKAGE (B) PACKAGE



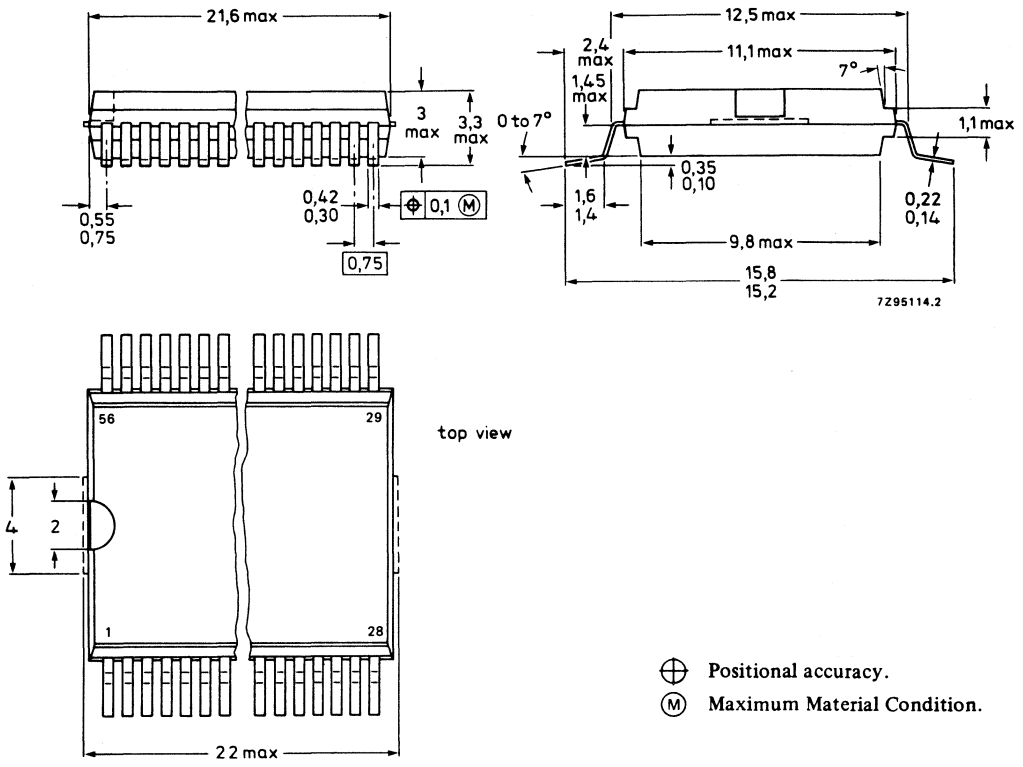
Dimensions in mm

SOT205A

7Z95754.3

Package Outlines

SOT190 **56-PIN PLASTIC VSO (VERY SMALL OUTLINE) DUAL IN-LINE PACKAGE**



Dimensions in mm

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